RFSoC Development Kit
Getting Started Guide

Version 1.8

Feb 24, 2023

Contents

Introduction

This tutorial serves as an introduction to the Avnet Zynq® UltraScale+™ RFSoC Development Kit with Qorvo RF Front End. Using the Avnet RFSoC Explorer® graphical user-interface in MATLAB, you will control the ZCU111 development board, generate and acquire signals through the Qorvo front-end card.

Avnet RFSoC Development Kit Overview

The Avnet Zynq UltraScale+ RFSoC Development Kit with Qorvo RF Front End enables system architects to explore the entire signal chain from antenna to digital using tools from MathWorks and industry-leading RF components from Qorvo. We extend the functionality of the Xilinx Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit by adding the Qorvo 2-Channel RF Front-end 1.8 GHz Card, plus native connection to MATLAB® & Simulink® with Avnet's RFSoC Explorer® application.

Please consult www.avnet.com/rfsockit or contact your local Avnet FAE for further details.

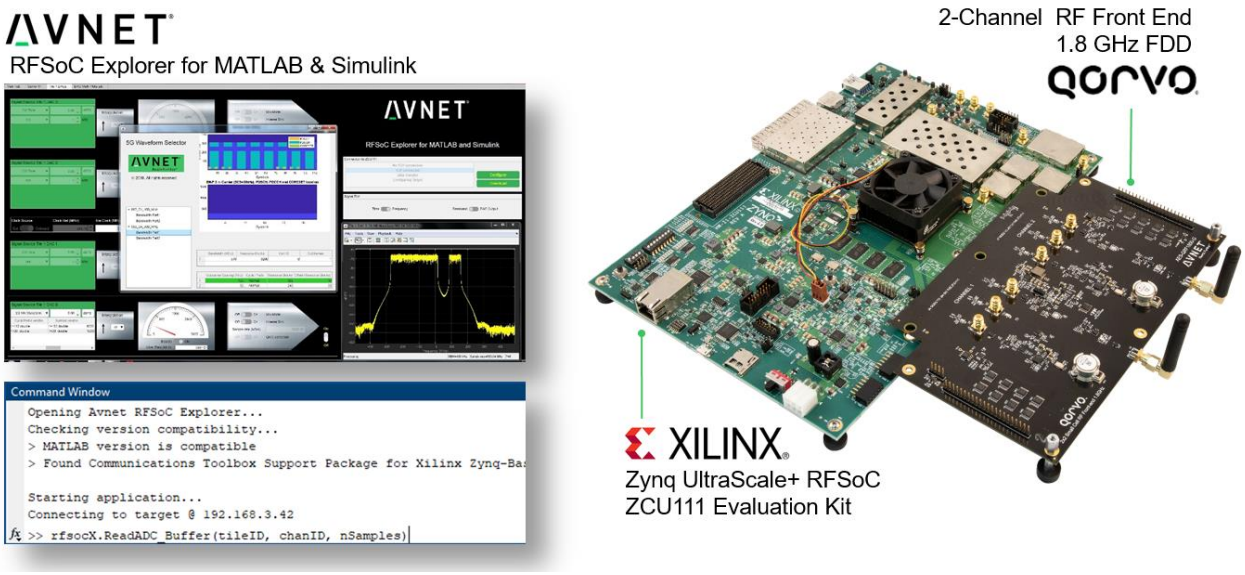


Figure 1 - Avnet Zynq UltraScale+ RFSoC Development Kit with Qorvo RF Front End

Regulatory Compliance Information

DISCLAIMER: This tutorial is provided for reference/educational purposes only and may not reflect results observed with other test equipment.

REGULATORY COMPLIANCE INFORMATION

FCC WARNING

This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Use of the kit should be limited to a development lab environment only.

CE WARNING

This evaluation kit is for use by professionals for their research and development purposes. The kit may not be put into service for use on a regular basis, or integrated into an end product (Annex I.4 of the RED). This kit is does not bare the CE mark of certification. As such, this kit may be operated only within the requirements of RED section 1.6.2.5, Custom-built evaluation kits.

Objectives

This tutorial is intended to help you:

- Gain familiarity with the Avnet RFSoC Development Kit with Qorvo RF Front End
- Use the Avnet RFSoC Explorer GUI to control the hardware, generate and acquire signals into MATLAB through the RF signal chains of the Qorvo card
- Explore the Avnet RFSoC Explorer user API for automated scripting and interface to MATLAB

Requirements

Laptop or PC with the following software installed:

- MATLAB
    - DSP System Toolbox
    - Fixed-Point Designer
    - Communications Toolbox
    - Communications Toolbox Support Package for Xilinx Zynq-Based Radio
    - Signal Processing Toolbox
    - LTE Toolbox (optional)
    - 5G Toolbox (optional)

Avnet Zynq UltraScale+ RFSoC Development Kit with Qorvo RF Front End

USB cable (Type A to Micro-USB Type B)

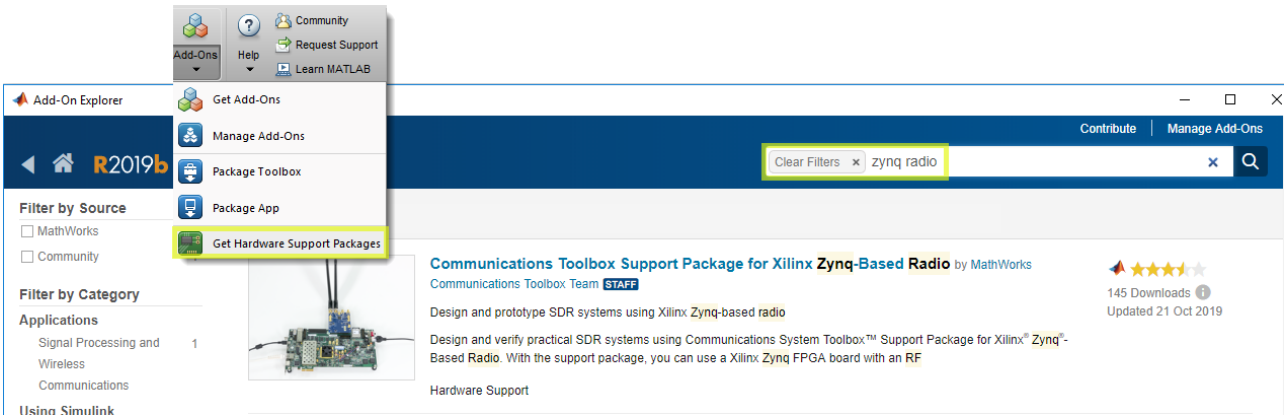
CAT5 Ethernet cable

Xilinx Vivado software is ***not required.***

Tools Setup

RFSoC Explorer installs easily in the MATLAB APPS tab without modifying your registry or other applications.

1. From MATLAB → Add-Ons, search for **Avnet RFSoC Explorer** and click install.
2. From MATLAB → Add-Ons, search for **Communications Toolbox Support Package for Xilinx Zynq-Based Radio** and click install.
    - ➢ After installation of this toolbox click **Setup Later** if prompted.



Hardware Setup

The Avnet RFSoC Development Kit includes the Xilinx Zynq ZCU111 Evaluation Kit. There are many jumpers and switches on the board, shipped with default states, which do not need to change for this tutorial. In the following steps we describe the minimal configuration. For a comprehensive setup guide, refer to the online ZCU111 Xilinx Wiki (*ZCU111 RFSoC RF Data Converter Evaluation Tool Getting Started Guide*).

1. Set the ZCU111 DIP switches (SW6) as shown in the figure below, which allows the ZCU111 board to boot from the SD card.

Figure 2 - ZCU111 SD boot switch settings

2. Remove the SD card from the ZCU111 and insert into your PC. Use an SD formatter tool format the card as FAT, https://www.sdcard.org/downloads/formatter_4/

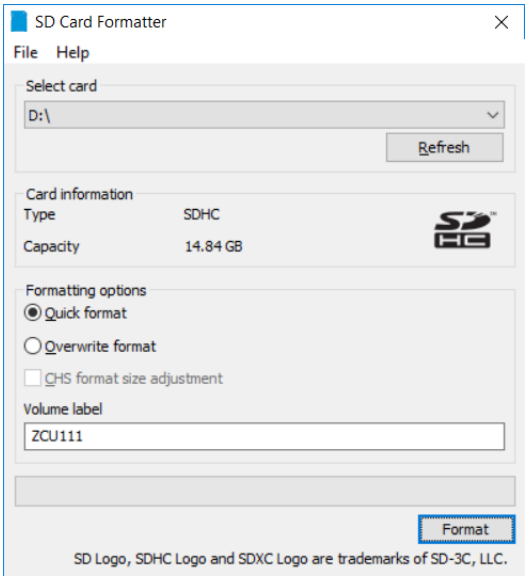


Figure 3 - SD card formatter

3. Use one of the links below to download the SD boot image archive.

   Avnet RFSoC Explorer v1.1.0 and earlier - avnet_rfsocX_zcu111_boot_20182_v1_0.zip

   Avnet RFSoC Explorer v2.0.0 and later - avnet_rfsocX_zcu111_boot_20183_v2_0.zip

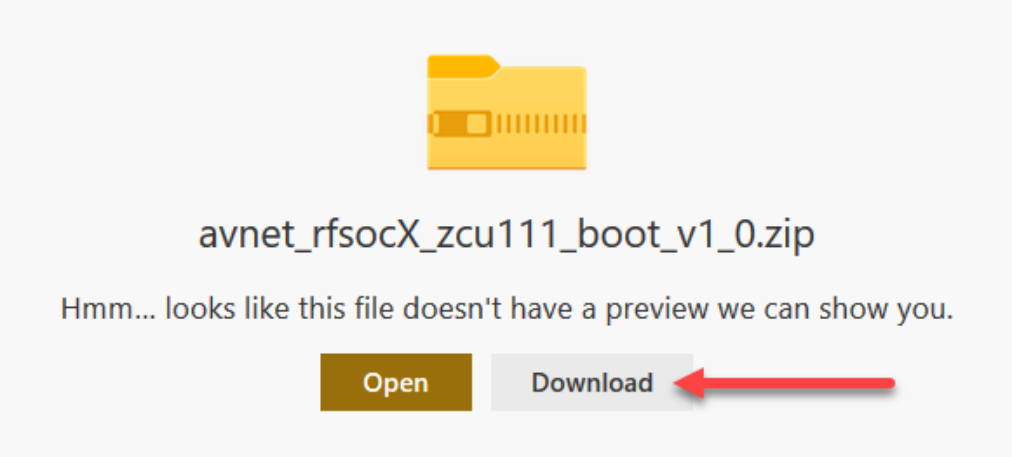


Figure 4 - SD Card Download

This archive contains the software for the ZCU111 evaluation board.

Unzip the archive to a convenient location on your hard disk, then copy the files to the root level of the SD card. Safely eject the SD card from the PC and replace into ZCU111.

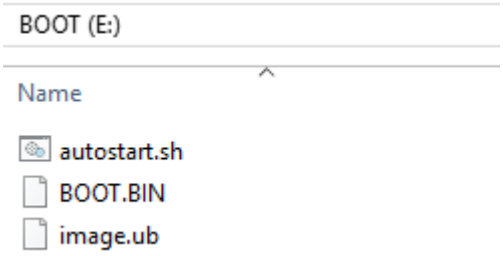


Figure 5 - SD Card Root Directory with Boot Files

4. To enable your PC to make a serial connection to the ZCU111 USB-UART, you must install the **Silicon Labs CP210x USB to UART Bridge VCP Drivers**. For step-by-step instructions see Appendix A: Installation of USB UART Driver.

5. Connect the Qorvo RF card, ZCU111, antennae, and cables as shown in Figure 6. Although no over-the-air transmission and reception is involved in this tutorial, the antennae provide convenient 50-Ohm termination to the PA.[1]

[1] Our original Qorvo 2-Channel RF Front-end 1.8 GHz Card (AES-LPA-QRF1800-G) is designed for small cell LTE Band-3 applications in FDD mode. Transmission for both channels in the downlink is centered at 1842 MHz; reception in the uplink at 1747 MHz. A later version of the Qorvo card (AES-LPA-QRF1800-RVS-G) is configured with channel 1 TX @ 1842.5MHz and RX @ 1747.5MHz; channel 2 TX @ 1747.5MHz, RX @ 1842.5MHz. This allows over-the-air loopback between channels. This tutorial uses the on-board TX observation path, therefore either version of the Qorvo card may be used.

6. Plug Ethernet and USB cables into your host PC

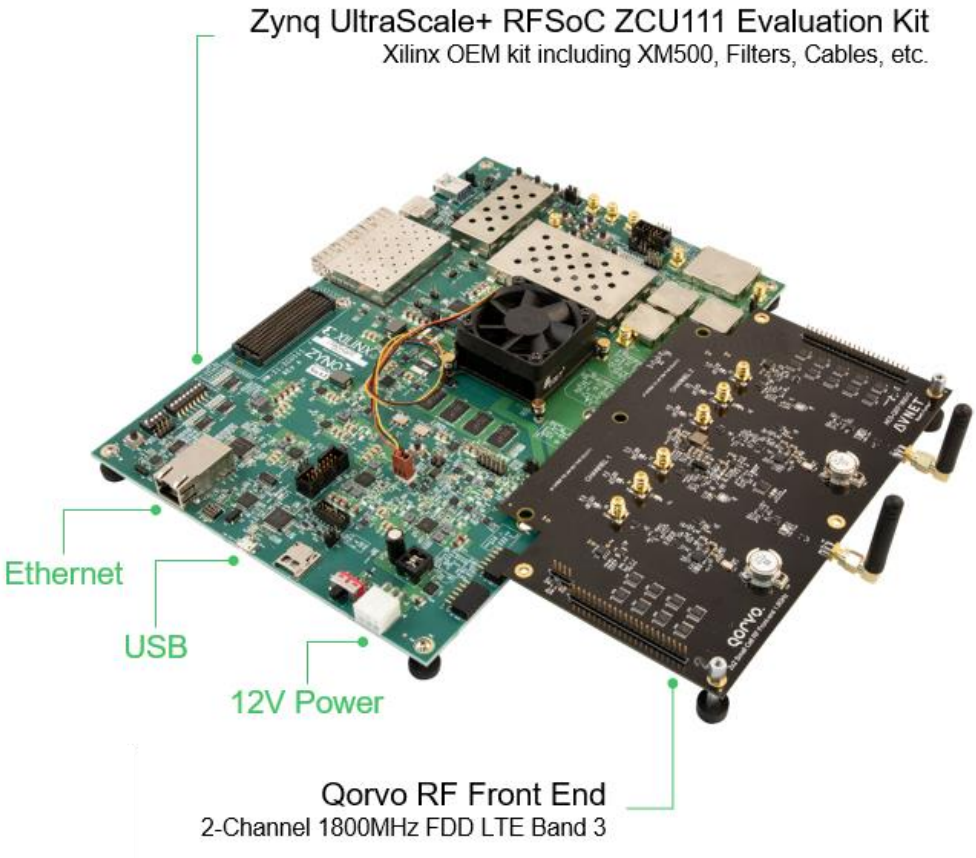


Figure 6 – Qorvo card mounted on ZCU111

For a comprehensive description of the functionality of the RF front-end, see *Qorvo 2-Channel RF Front-end 1.8 GHz Card Hardware User Guide* at www.avnet.com/rfsockit

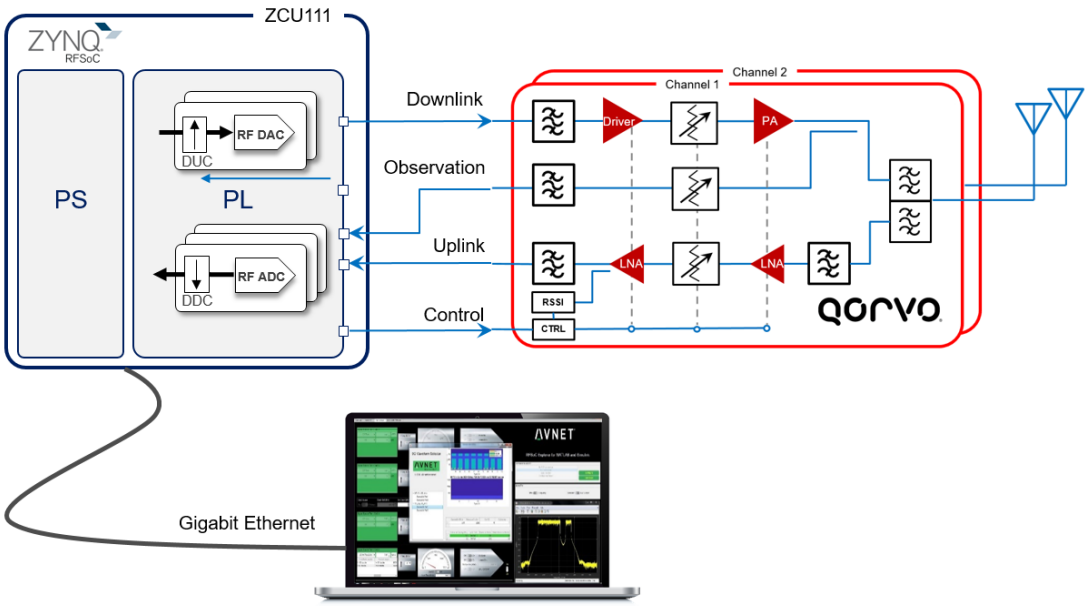
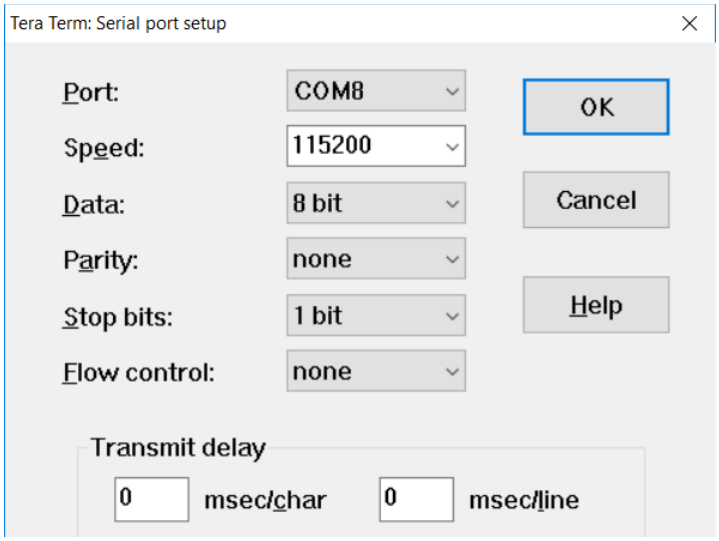


Figure 7 - Block diagram of Avnet RFSoC Development Kit

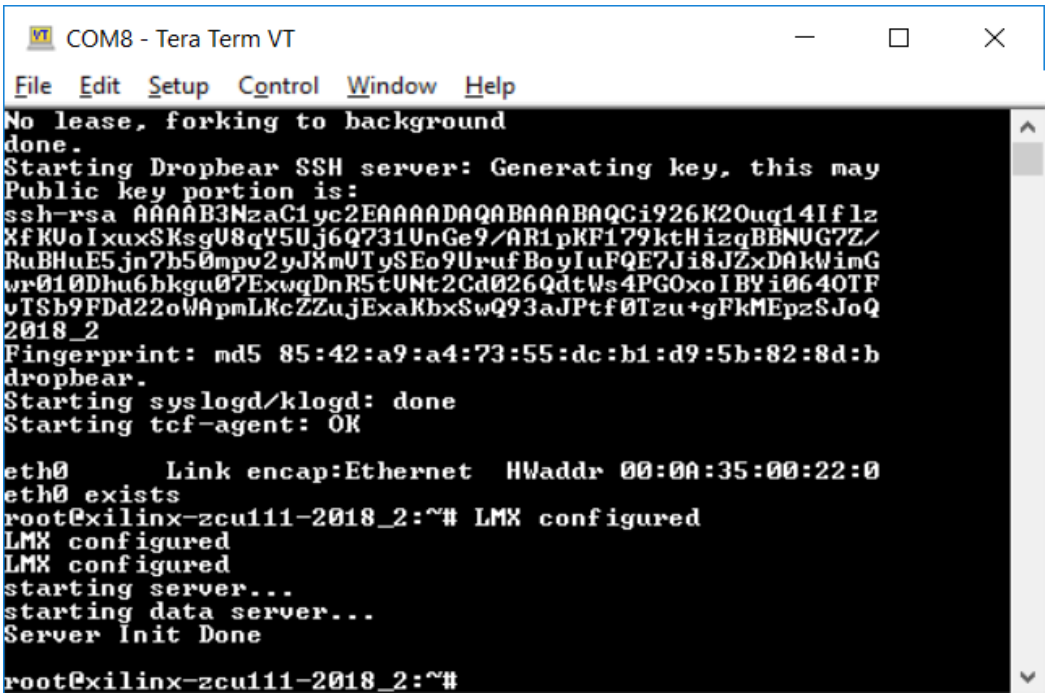
Booting ZCU111

1. Turn the ZCU111 power switch ON (near the 12V connector)

From your PC launch a terminal program with 115200/8/n/1/n settings. For the example output shown here, Tera Term was used. For information on setting up Tera Term to use with the ZCU111 USB-UART port, see Appendix A: Installation of USB UART Driver.

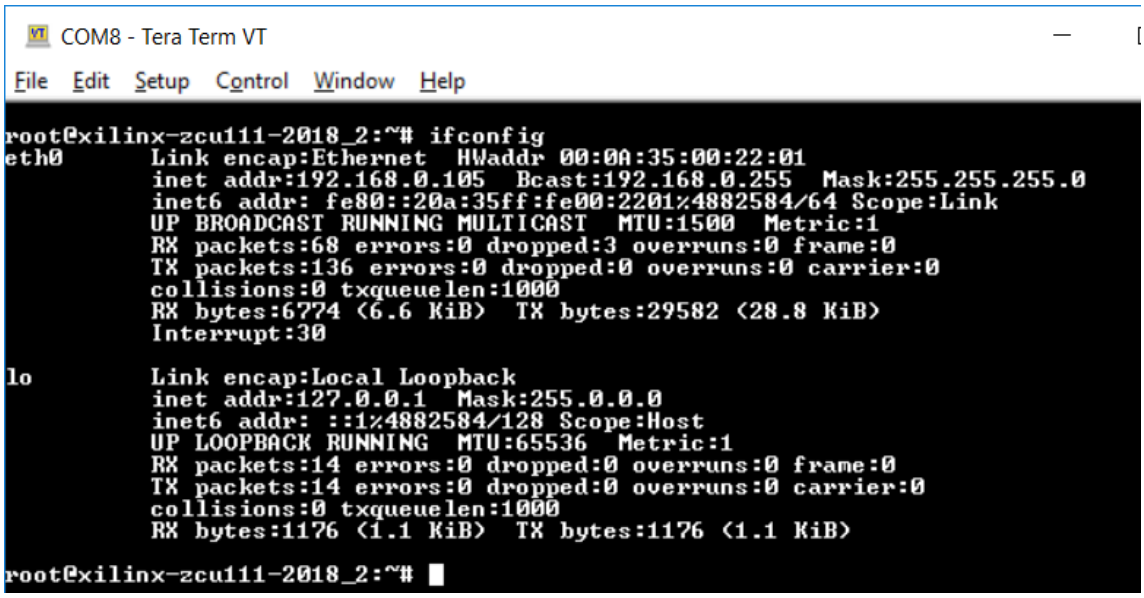


2. You should observe terminal output from U-Boot and then Linux output appear in the Tera Term window. After the final boot message '**`Server Init Done`**', press enter to generate a carriage return and command-line prompt from ZCU111.



Ethernet TCP/IP Connection to ZCU111

Upon booting to Linux the ZCU111 Ethernet port should have an IP address. Discover it by running the **`ifconfig`** command.



The ZCU111 Ethernet IP in this example is `192.168.0.105`

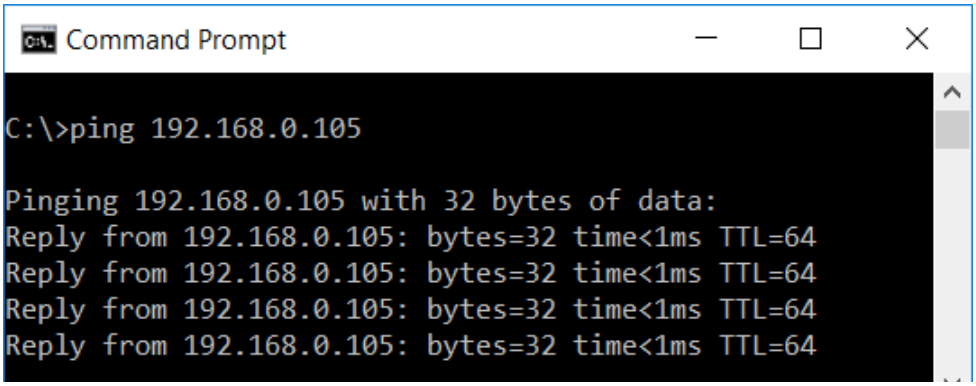
Set a static IP for your host PC's Local Ethernet adapter. Make sure your PC and the board are on the same subnet, gateway, etc.

Laptop Ethernet IP: `IP 192.168.0.106`

```
Subnet 255.255.255.0
```

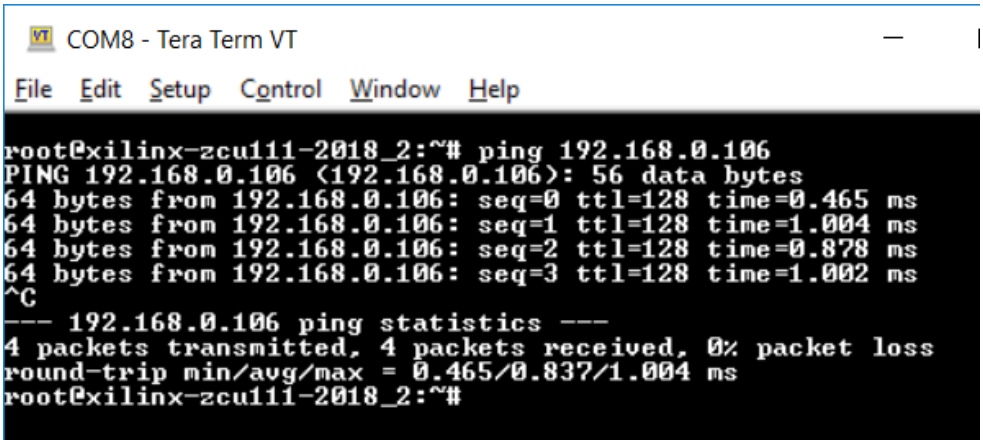
From the host PC, open a Windows command prompt and ping the ZCU111 board to verify Ethernet connectivity.

```
C:\> ping 192.168.0.105
```



From the host PC serial terminal connection to Linux running on the ZCU111, verify Ethernet connectivity by pinging your host PC.

```
root@xilinx-zcu111-2018_2:~# ping 192.168.0.106
```



Qorvo Card Control

1. The Qorvo 2-Channel RF Front-end 1.8 GHz Card is controlled from a Linux application running on the Processing System (PS) APU of the RFSoC. Commands sent from the PC through the USB_UART of ZCU111 are subsequently transferred to control registers on the Qorvo card via an SPI BUS. Refer to the Avnet Qorvo 2-Channel RF Front-end 1.8 GHz Card Hardware User Guide for more information.[i]

   At the terminal command-line, type '**`qorvo`**' to launch the control menu for the Qorvo card.

   Note: If you make a mistake while typing commands in the Qorvo control menu, use the keyboard 'Delete' key to backspace at the command line.

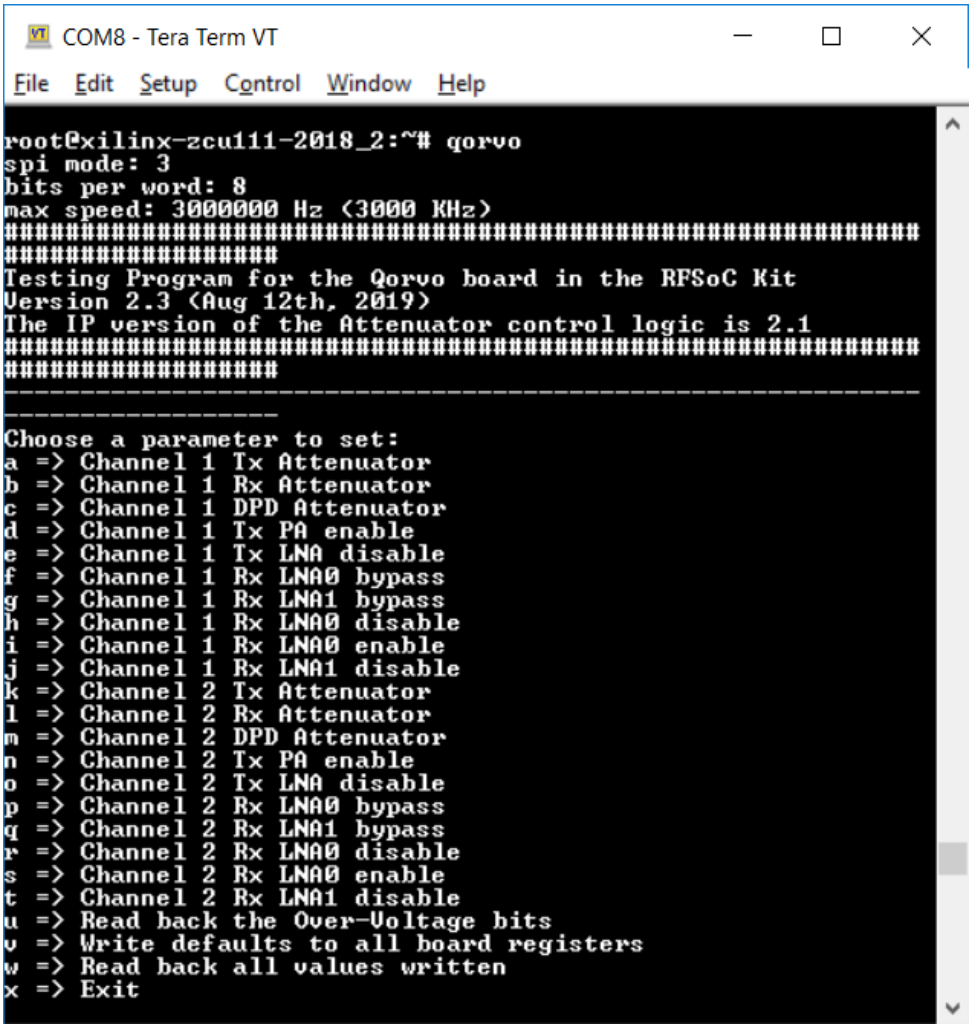


Figure 8 - Qorvo card command menu

2. Type '**`v`**' at the terminal command line, followed by a carriage return, to write default values to all control registers in the programmable devices of the Qorvo card.

3. Type '**w**' at the terminal command line, followed by a carriage return to display all current values. Note that these are the last values written to the Qorvo registers, not a read back of the device registers.

4. In preparation for next steps, we shall ensure that no RF output power emerges from the QPA9903 power amplifier (PA) in the TX signal chain of the Qorvo card.

   Type '**e**' at the terminal command line followed by a carriage return, then type '**1**' to disable the TX TQL9092 driver amplifier.

   Type '**d**' at the terminal command line followed by a carriage return, then type '**0**' to disable the QPA9903 power amplifier.

   With the digital attenuators at maximum attenuation, the previous steps have ensured that no signal power is coupled back from the PA through the DPD observation path on channel 1 of the Qorvo card to the RF-ADC of RFSoC on ZCU111. This is done for the purpose of calibrating the DPD observation path RF-ADC in next steps.

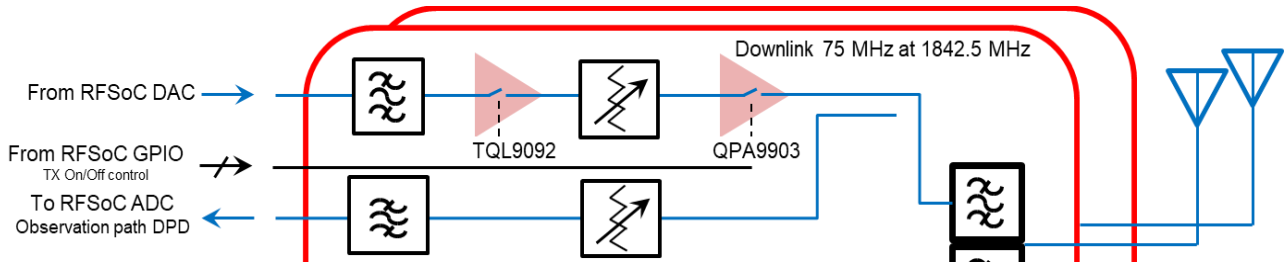


Figure 9 – Qorvo card TX signal chain disabled

Experiment 1: Generating a CW Tone through the TX Path

The power amplifier (PA) output in each channel of the Qorvo RF card is routed back to an RF-ADC through a directional coupler, providing an observation path typically used for digital pre-distortion of the PA. In this experiment we shall generate a CW tone in the digital domain from the RFSoC Explorer graphical user interface (GUI) running under MATLAB on the host PC. The digital signal data will be downloaded to the ZCU111 over TCP/IP and stored in DDR4 memory dedicated to the RF-DACs.

Once download is complete, the signal data will be read out of the memory buffer through DMA and routed to the digital up-converter (DUC) within the RF_DAC tile, interpolated to a higher sampling rate, frequency-shifted to 1842 MHz through the complex mixer and converted to the analog domain by the RF-DAC. This process repeats indefinitely, constantly looping back to the start of the data in the memory buffer after reaching the end to generate a CW tone at the output of the DAC. To avoid discontinuity between the start and end loop-points of the CW tone, RFSoC Explorer automatically adjusts the signal length to an integer number of cycles, thereby ensuring a smooth zero-crossing upon looping back to the start of data.

The directional coupler at the output of the PA routes the RF signal back towards an RF-ADC on the ZCU111, with 20 dB of attenuation. Normally intended as an observation path for digital pre-distortion and PA linearization, this provides a convenient means of re-acquiring the PA output signal into the digital domain without any external connections. Our objective here is simply to demonstrate usage of RFSoC Explorer to generate and acquire signals and control the RF signal chain; we shall leave PA linearization for another day.

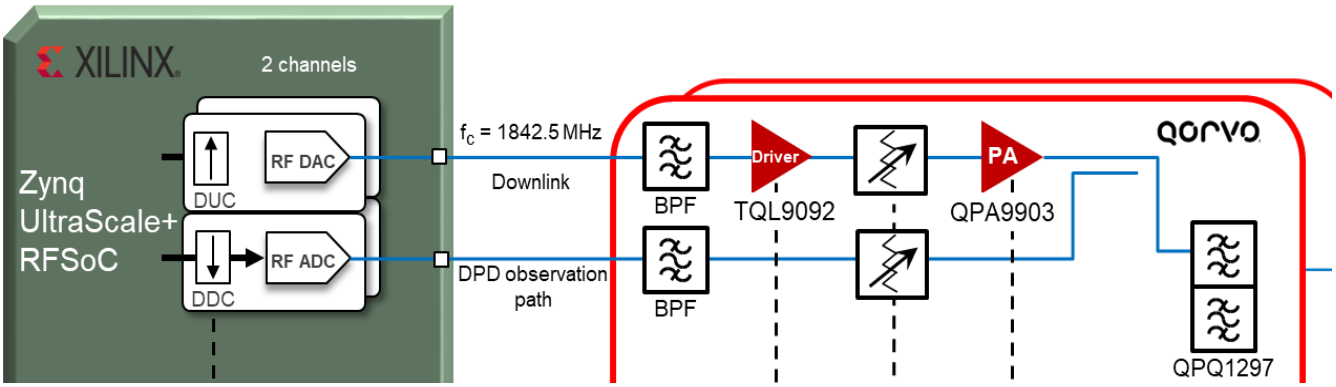


Figure 10 - TX signal chain and DPD observation path

1. Start MATLAB R2019b

2. In MATLAB, go to the APPS tab and click the  icon for **Avnet RFSoC Explorer**.

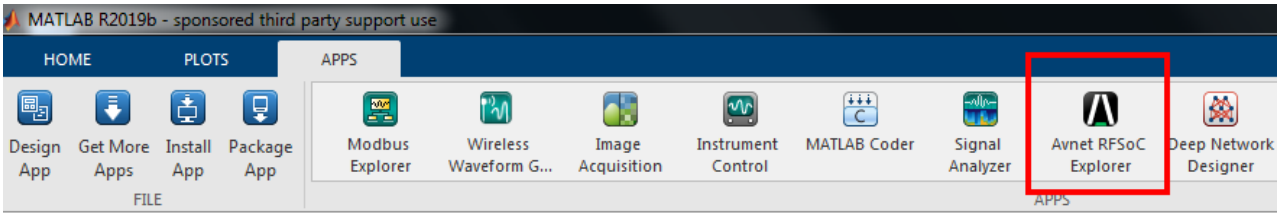


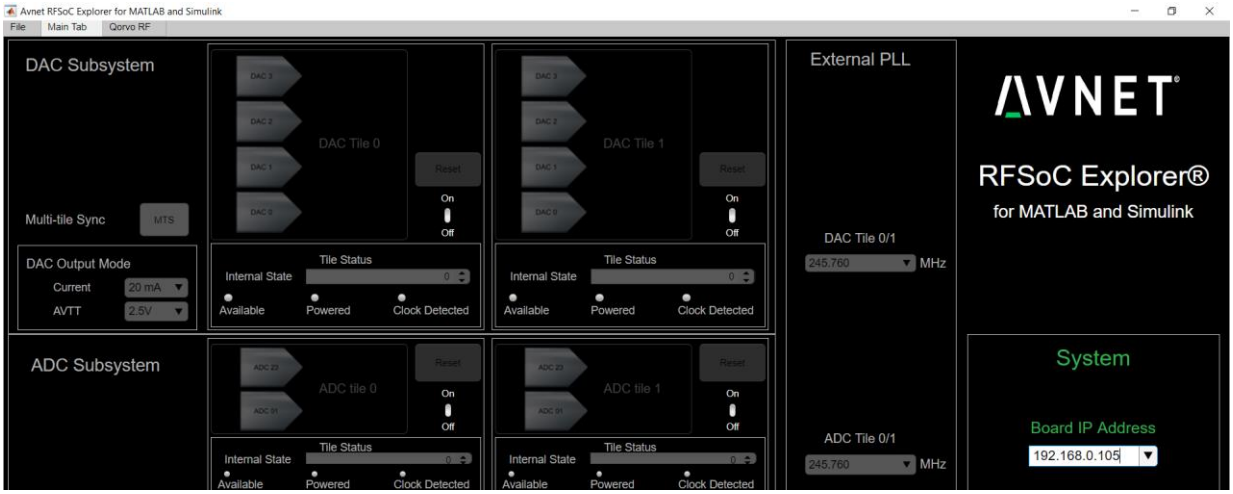
Figure 11 - Launching RFSoC Explorer

Shown in Figure 12 is the mapping of RFSoC data converters on ZCU111 that connect to signal paths of the Qorvo RF card. 'Tile' and 'Block' indices are zero-based. For ADCs, Block (0 => 01; 1 = >23).

Qorvo Signal	CH2_RX	CH2_DPD	CH1_RX	CH1_DPD	CH2_TX	CH1_TX
AMC/Schem.	ADC_01	ADC_03	ADC_05	ADC_07	DAC_00	DAC_06
Tile	0	1	2	3	0	1
Block	1	1	1	1	0	2

Figure 12 - Channel map of ZCU111 data converters

From the main tab of RFSoC Explorer set the Board IP Address that was previously found using the **`ifconfig`** command from the host PC serial terminal connection to Linux running on the ZCU111.



Frequency Planning

Frequency planning involves selecting appropriate sampling rates, Nyquist zone of operation and digital signal processing according to signal bandwidth, I/F frequency and board-level filtering. In this case the bandwidth of LTE-band-3 is 75 MHz, centered at 1842 MHz in the downlink.

While the bandwidth of the RF-ADC could easily support direct-RF conversion of the 1842 MHz I/F in the first-Nyquist zone, the relatively small instantaneous signal bandwidth of 75 MHz would make such an approach wasteful of resources and power. We shall instead aim to match the response of the digital halfband filters in the decimation stage of the digital downconverter (DDC) to the bandwidth of the LTE Band-3 signal.

The decimation filters are flat out to 80% Nyquist passband or 0.4*Fs.[2] Based on 75 MHz bandwidth of the LTE Band-3 signal, we derive a suitable sampling rate at the RF- ADC as shown below.

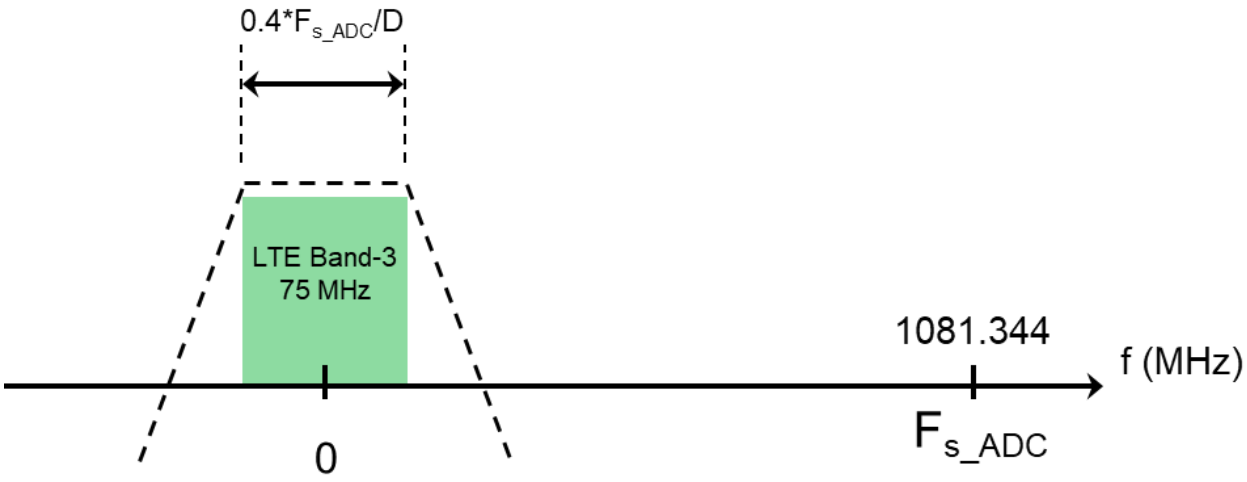


Figure 13 - ADC sampling rate and decimation factor for LTE-band 3

$0.4*F_{s\_ADC}/D \geq 75/2$ (MHz)

Solving for F_{s_ADC} and decimation factor D yields a suitable sampling rate for the RF-ADC.

$D = 8$

$F_{s\_ADC} \geq 750$ MHz

[2] Ref: *Table 41:* **Decimation Filter Operating Modes, Xilinx PG269 (v2.1) May 22, 2019**

Referring to Figure 14, a 1.00 MHz CW tone *x(n)* generated in the digital domain by RFSoC Explorer is sent through the interpolation filters and shifted in frequency by the complex mixer in the digital up-converter to form an analytic signal tone at 1843 MHz. Once converted to the analog domain the signal connects to the transmit path of the Qorvo card to reach the PA, where it is routed back through a directional coupler to an RF-ADC within the observation path normally used for PA linearization.

Note that the conversion from the digital to the analog domain produces a real signal with negative frequency component. The bandpass BAW filter serves as a re-construction filter to attenuate undesired images that are normally generated at multiples of the DAC sampling rate.

At the RF-ADC the sampling process produces virtual copies in the digital domain of the baseband signal centered at multiples of the sampling frequency. Careful frequency planning can exploit this phenomenon to retrieve the signal of interest without need of a high sampling rate that is greater than the highest frequency component of the analog signal, which in this case is 1843 MHz. By purposely sampling at a lower rate to create aliasing, copies of the signal can be made to appear at convenient frequency locations outside of the 1st Nyquist zone (0 – Fs/2 Hz). This is known as under-sampling or bandpass sampling. From there, the signal of interest can be shifted in frequency back to baseband by the complex mixer within the digital down-converter.

We shall shift to baseband the high-side image appearing at -319.688 MHz due to the alias centered at -2*Fs_ADC. Mixing with an effective NCO frequency of 320.688 MHz through the complex mixer brings our original CW tone back to 1 MHz. The signal then passes through three stages of decimation filters to attenuate any unwanted out-of-band frequency components and noise, reducing the effective sampling rate to 135.168 MSPS, amply satisfying Nyquist for an LTE Band-3 signal bandwidth of 75 MHz.

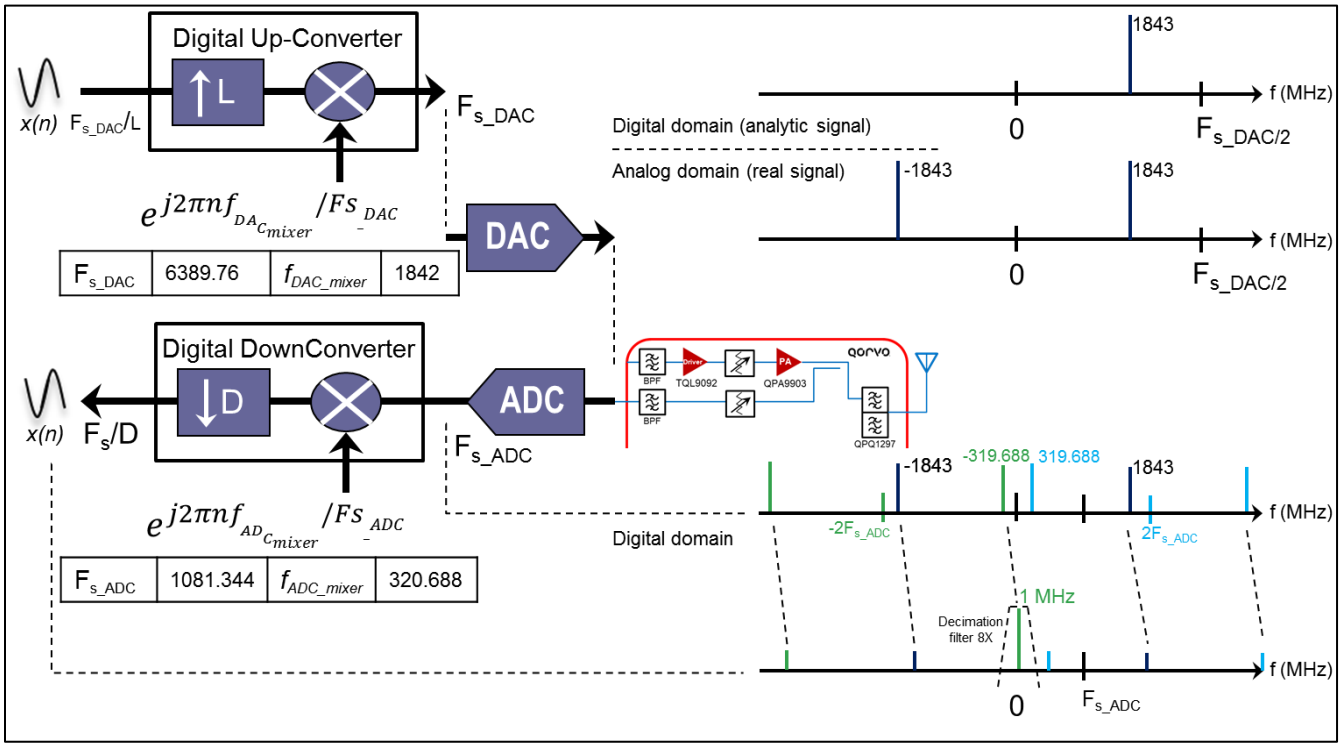


Figure 14 - Frequency planning for PA observation path for LTE-band 3

Configuring the RF-ADC in the DPD observation path

We start by enabling the ADC block for the DPD observation path in channel 1 of the Qorvo RF card, which connects to ADC07 (Tile 3, Block 1) of the RFSoC device on ZCU111.

1. Enable ADC Tile 3 in RFSoC Explorer. Click to enter the tile.

Figure 15 - RFSoC Explorer Enabling ADC Tile 3

2. Enable ADC23. This is the ADC block that connects to the channel 1 observation path of the Qorvo RF card. Click OK on the warning box; you will perform ADC calibration in a later step.

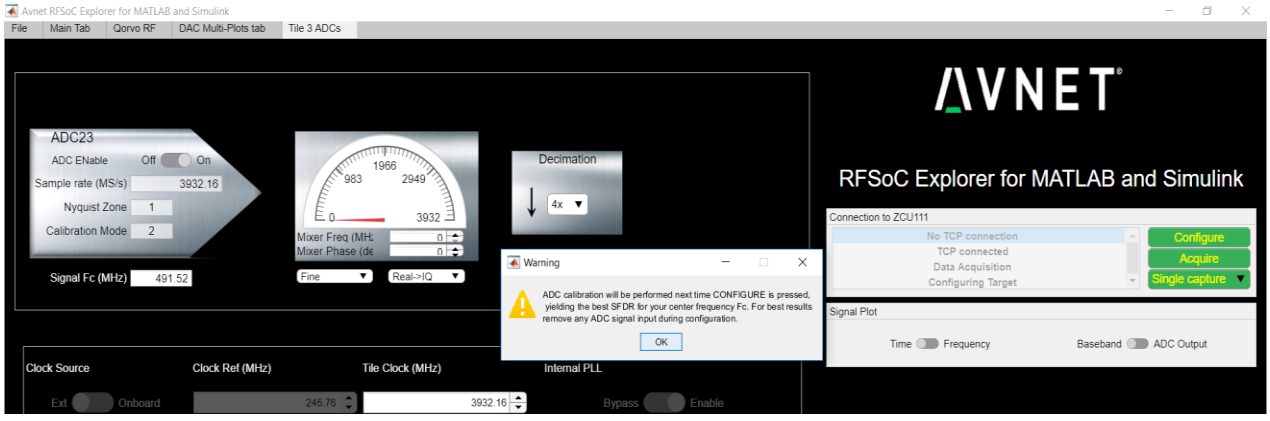


Figure 16 – Enabling ADC23 in Tile 3

3. Adjust the ADC tile clock to 1081.344 MHz. This controls the sampling rate for both RF-ADCs in the tile.

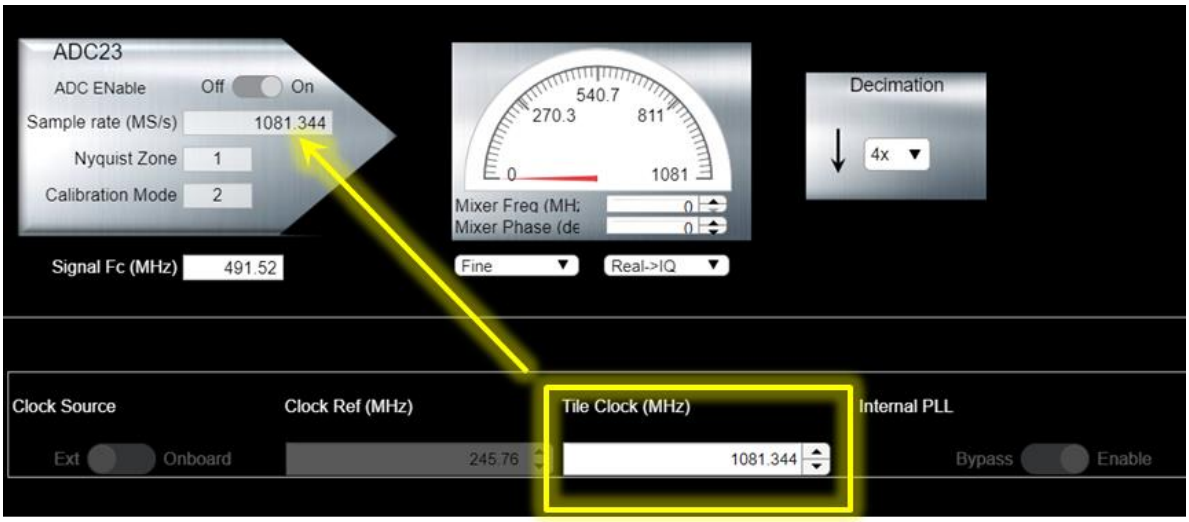


Figure 17 - Setting RF-ADC sampling rate

4. The NCO frequency for the complex mixer within the digital downconverter represents the shift in frequency to apply to the signal of interest at the ADC input, centered at F_c in the analog domain. In this case F_c = 1842 MHz for LTE Band-3. We wish to shift the CW tone at 1843 Mhz back to 1 MHz.

   The complex mixer operates in the digital domain; NCO frequency settings in the range of -10 GHz to 10 GHz translate to an 'effective' NCO frequency in the digital domain (from -Fs/2 ... Fs/2). If the analog signal centered at F_c is in a higher Nyquist zone relative to the ADC sampling rate, a digital alias will be shifted back to DC. This is sometimes referred to as sub-sampling, as described on page 48 of *Zynq UltraScale+ RFSoC RF Data Converter 2.1 PG269*; see endnote **Error! Bookmark not defined.**.

   Set the ADC complex mixer to -1842 MHz.

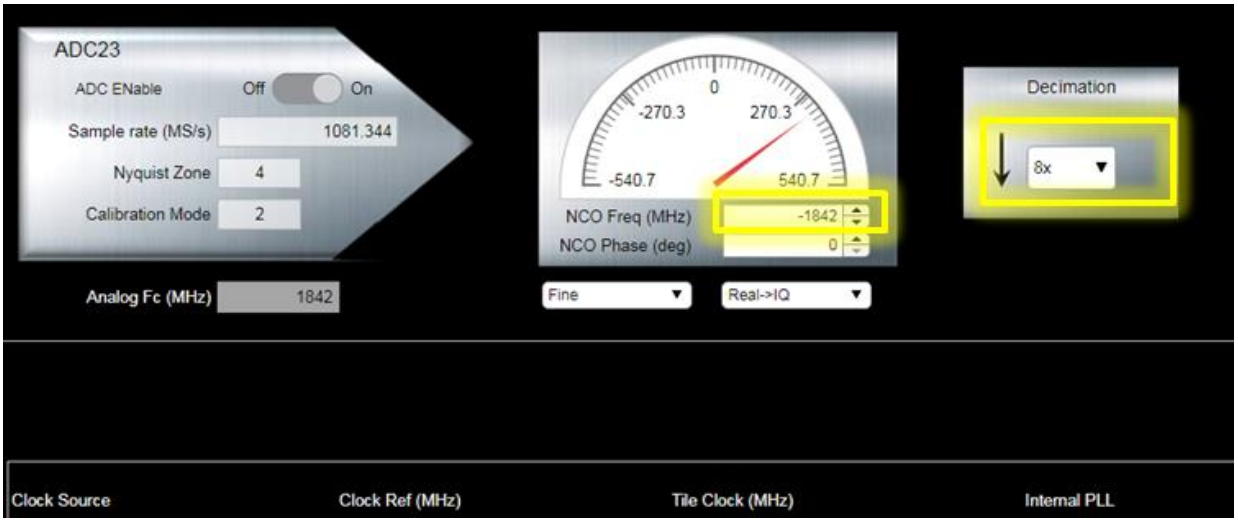
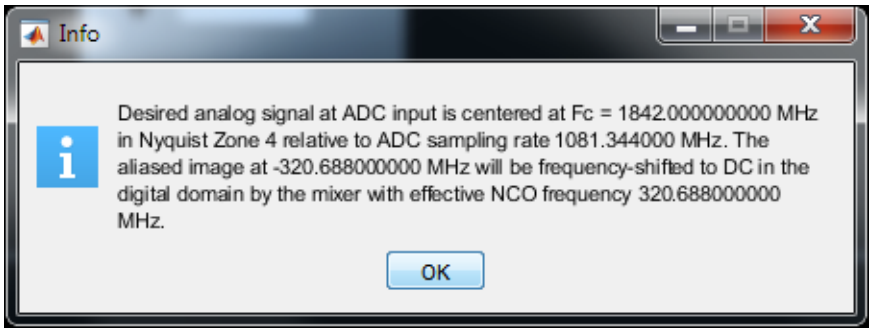


Figure 18 - Setting ADC complex mixer frequency

Observe the information dialog confirming the 'effective' NCO frequency. Refer also to Figure 14.



Each of the RF-ADCs in the Zynq UltraScale+ RFSoC is built on multiple sub-ADCs in an interleaving architecture. The nature of the interleaving process requires that an intricate calibration algorithm be carried out to obtain the best dynamic range performance from the RF-ADC. It is recommended to remove all signal power at the input of the RF-ADC during the calibration process; this was accomplished by disabling the TX signal chain in previous steps. Further details are provided in section '*RF-ADC Nyquist Zone Operation*' *Zynq UltraScale+ RFSoC RF Data Converter 2.1 PG269* [ii].

RFSoC Explorer automatically calculates and displays Nyquist Zone and Calibration Mode as a function of the input signal center frequency Analog Fc, and the ADC tile sampling rate.

Finally set decimation to 8X. This will enable the cascade of 3 half-band decimation filters within the RF-ADC tile to attenuate unwanted frequency components above 67 MHz (at baseband) and reduce the sampling rate to 135.168 MSPS.[3]

Activate the 'Configure' pushbutton to perform ADC calibration and download settings to the RF-ADC tile.

[3] This sampling rate is sufficient for the purpose of demonstrating acquisition on a CW tone. In a true PA linearization application it would be necessary to conserve greater excess bandwidth through the observation path to capture any non-linear distortion products from the PA beyond the signal bandwidth. The useable bandwidth through the BAW filter in the DPD observation path is approximately 180 MHz, from 1750 to 1930 MHz.

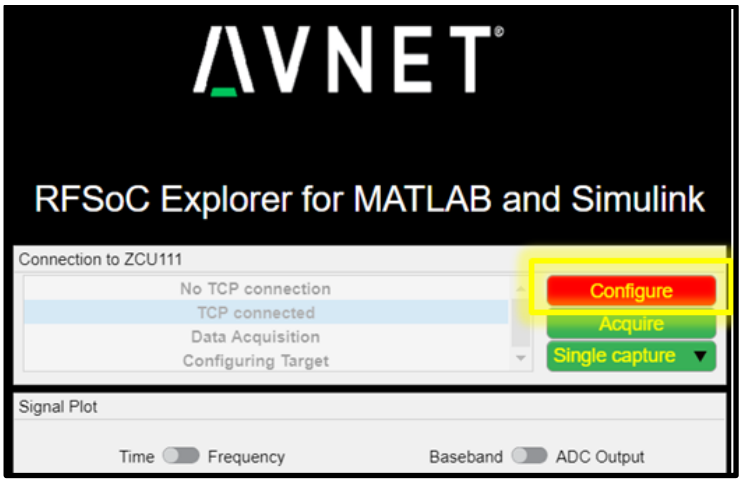


Figure 19 - Configuring the RF-ADC

5. The configuration process communicates with the Xilinx RFdc Linux driver API running on the Processing System (PS) APU of the RFSoC, providing runtime interaction and monitoring of the data converters. For reference, the Xilinx RFdc source files are publicly available on GitHub[iii].

   RFdc responds with the actual ADC tile sampling frequency that was programmed in the internal PLL. Click OK to dismiss the dialog box.

   The RF-ADC block for the DPD observation path of the Qorvo RF card has been activated.

6. We can now re-enable the TX driver and PA of the Qorvo card.

   Type '**d**' at the terminal command line followed by a carriage return, then type '**1**' to enable the QPA9903 power amplifier in channel 1 of the Qorvo card.

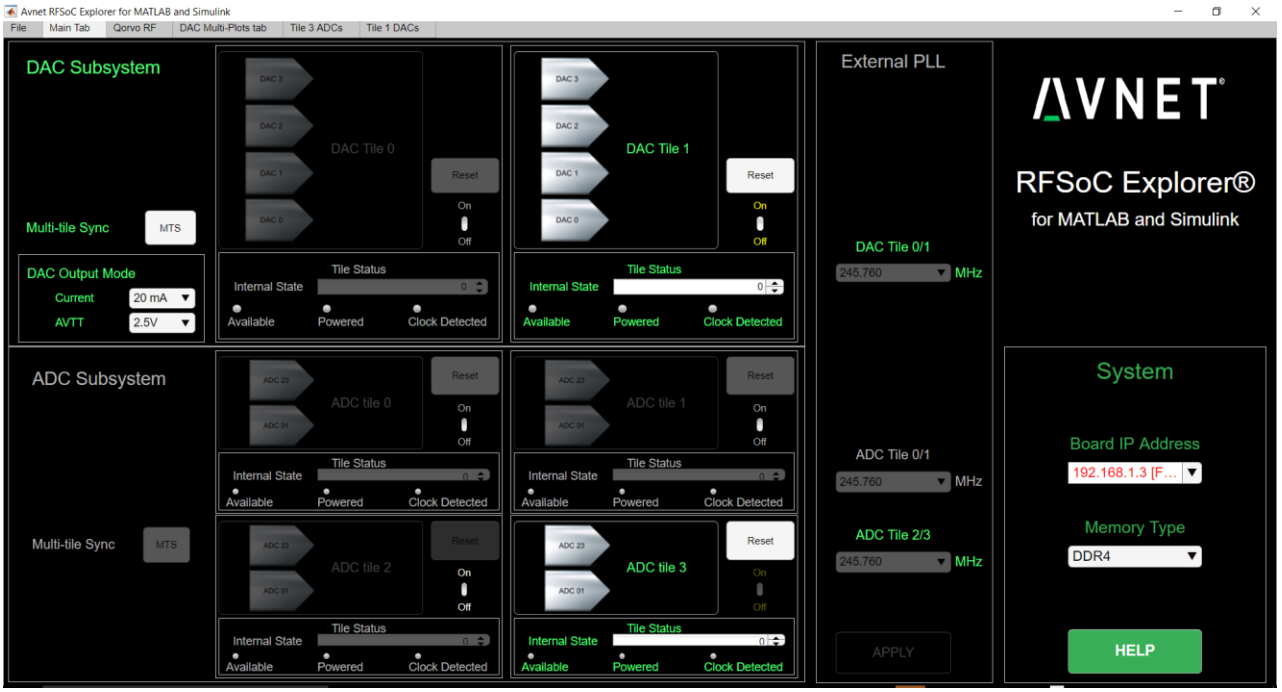
   Type '**e**' at the terminal command line followed by a carriage return, then type '**0**' to enable the TX TQL9092 driver amplifier in channel 1 of the Qorvo card.

Channel 1 TX signal chain of the Qorvo card has been re-enabled, while the digital attenuators remain at maximum attenuation. Refer to Figure 9.

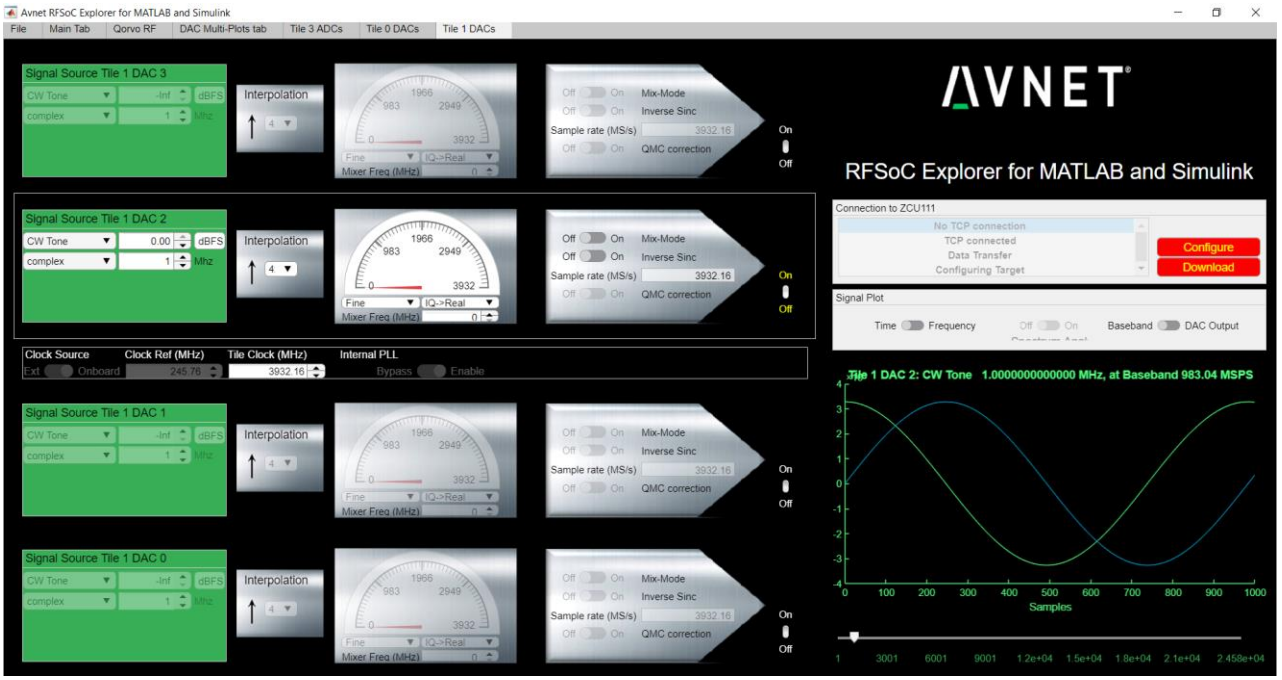
We now proceed to configure the RF-DAC to generate a CW Tone for the Qorvo card.

Configuring the RF-DAC in the transmit path

1. Enable DAC Tile 1 in RFSoC Explorer. Click to enter the tile.



2. Enable RF-DAC block 2, connecting to channel 1 transmit path of the Qorvo RF card. Refer to Figure 10

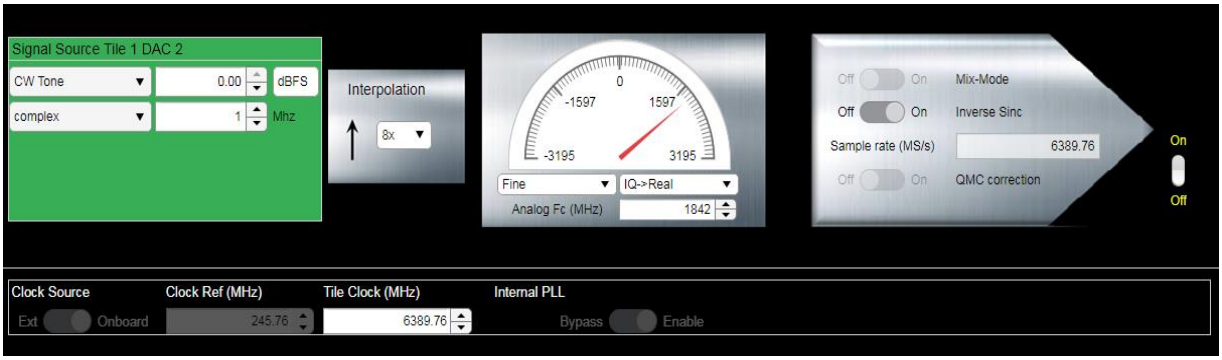


3. Adjust the DAC tile clock to 6389.76 MHz. This sets the sample rate for all 4 DACs in the tile.

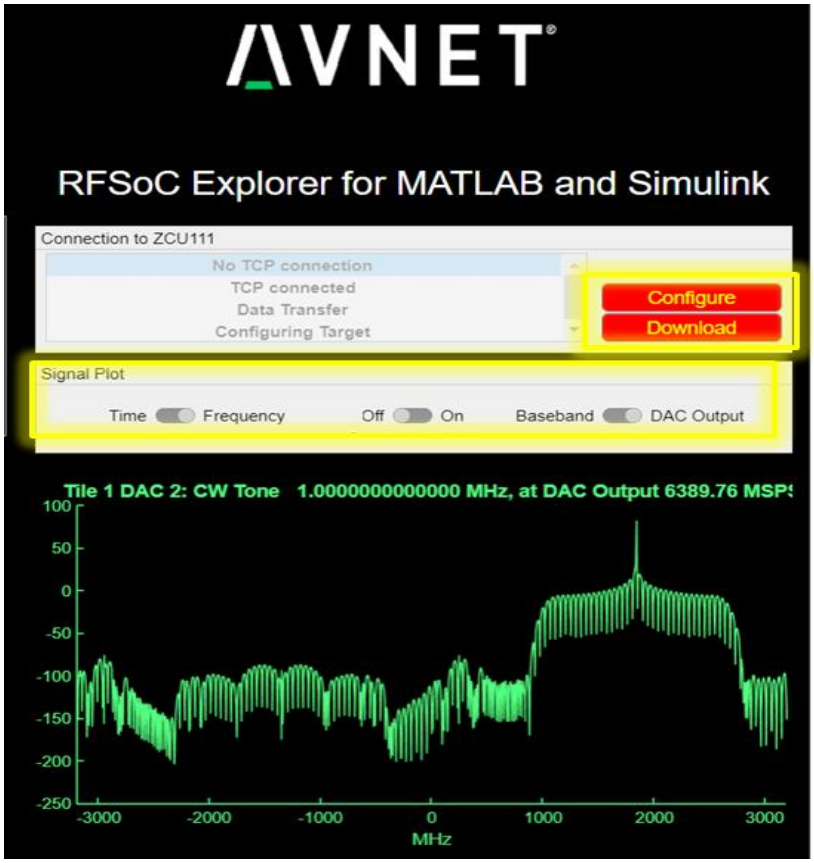
   Leave 'Signal Source' parameters to default values: CW Tone, complex, 0 dBFS, 1 MHz.

   Set the complex mixer within the RF-DAC tile to centre-frequency of LTE Band-3, 1842 MHz. The resulting CW tone will be at 1843 MHz at the output of the DAC.

   Set Interpolation = 8.



4. In the 'Signal Plot' panel, set to 'Frequency' domain and select 'DAC Output'. This is useful for frequency planning by displaying the interpolated signal at the DAC output sampling rate, post-mixer. Finally press 'Configure', then 'Download' to transfer the signal data from MATLAB to the DAC memory buffer of ZCU111.



5. At this point the RF-DAC is continuously transmitting a 1 MHz CW Tone, digitally mixed with a 1842 MHz carrier to emerge at 1843 MHz from ZCU111 through the TX signal chain of the Qorvo RF front-end card. The output of the power amplifier is coupled back through the DPD observation path towards the RF-ADC for signal capture.

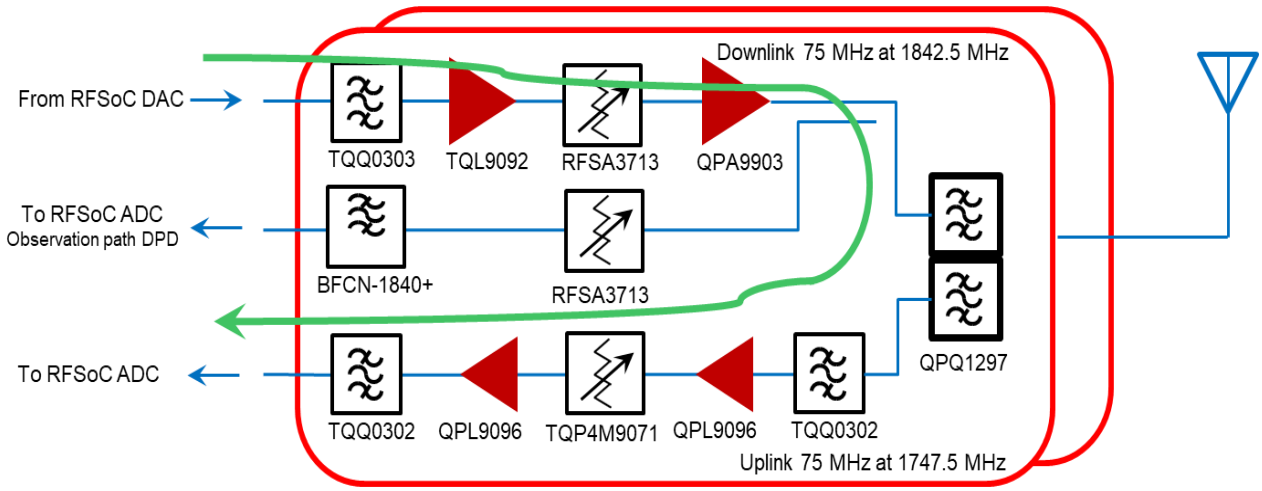
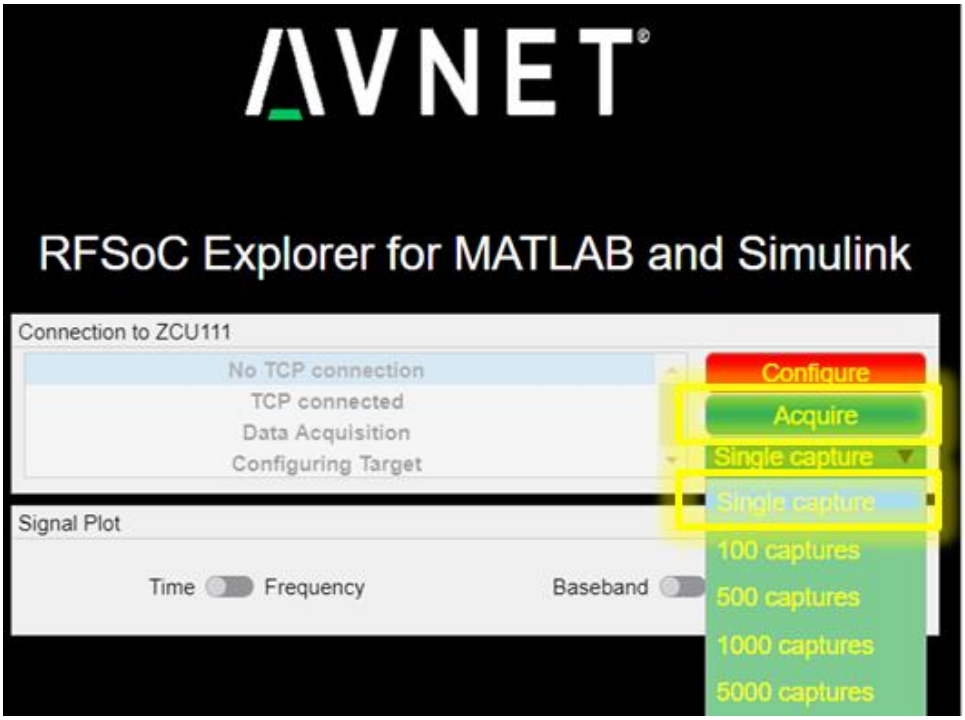


Figure 20 – LTE Band-3 downlink and DPD observation signal paths

6. Return to the main tab and descend into ADC Tile 3. Select 'Single Capture' and press 'Acquire'.



7. Observe the CW tone which has been mixed back to 1 MHz by the ADC mixer. The signal level is low because the digital attenuators are still at maximum attenuation.

8. Select ‘500 Captures’ and press ‘Acquire’.

We shall now relax the DPD observation path attenuation in 10 dB steps, gradually increasing the signal level at the RF-ADC while the acquisition is underway.

9. Type ‘**c**’ at the terminal command line followed by a carriage return, then enter the value ‘**80**’ to decrease the attenuation by 10 dB. Repeat with values ‘**40**’ and ‘**0**’. Observe the corresponding increase in signal level, which should ultimately reach approximately -1.65 dBFS.

Finally we can relax the Channel 1 TX digital attenuator, which until now has remained at maximum attenuation.

10. Type ‘**a**’ at the terminal command line followed by a carriage return, then enter the value ‘**119**’ to decrease the attenuation by 1.65 dB. The signal level should now be approximately 0 dBFS, full-scale.

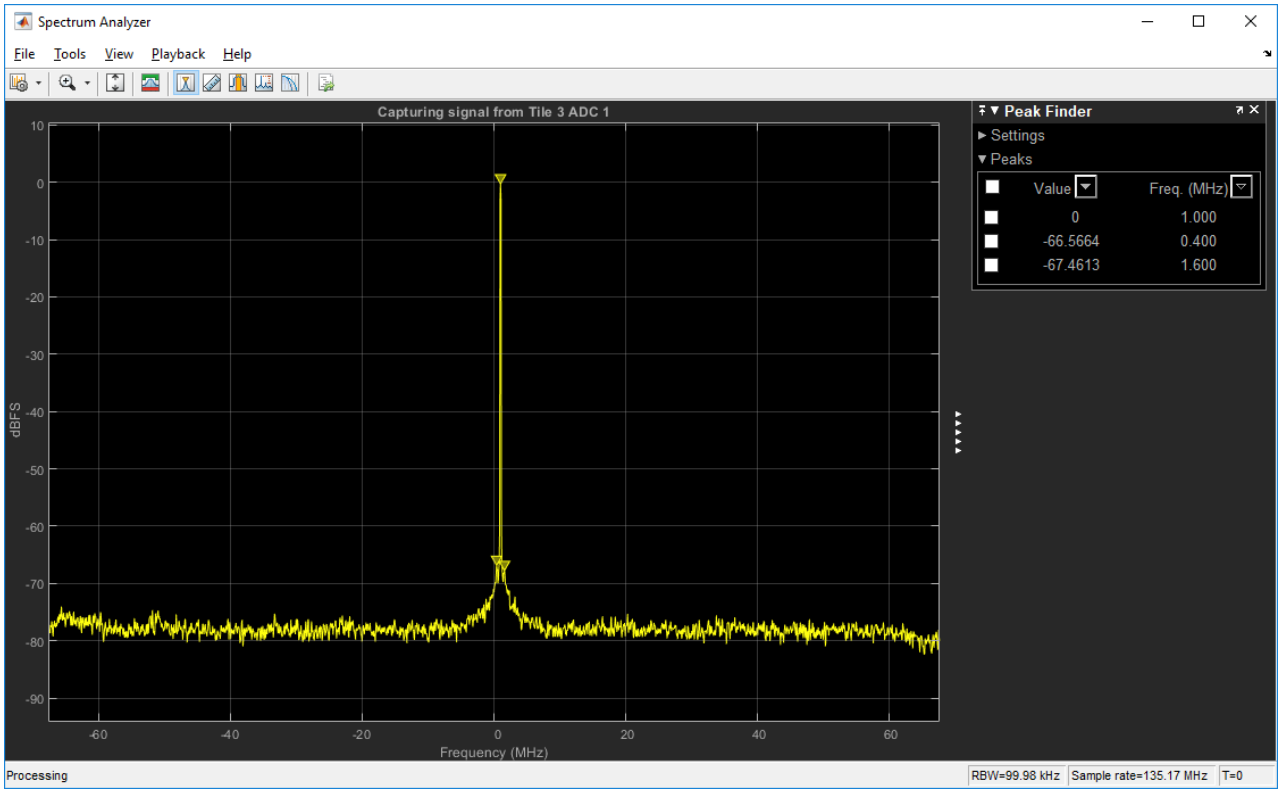


Figure 21 - Channel 1 Tx Attenuator relaxed by 1.65 dB to reach 0 dBFS at observation ADC

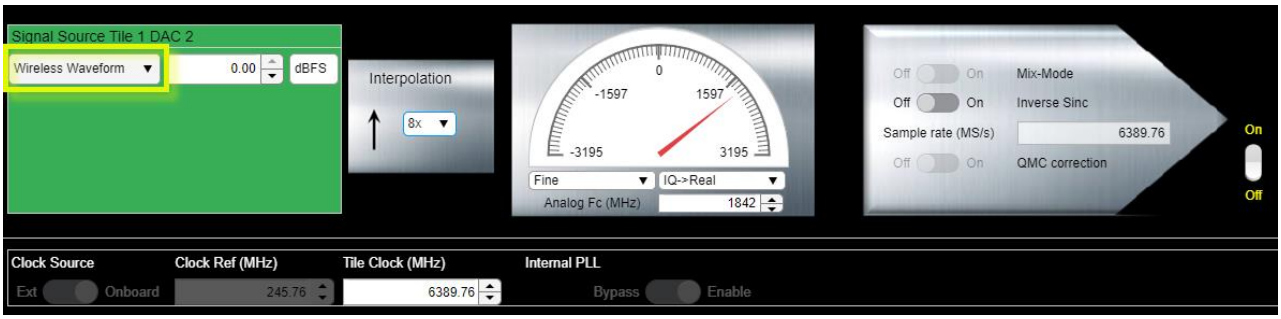
Important: Increasing the signal strength through the DPD observation path beyond this level may cause damage to the RF-ADC.

This completes experiment 1.

Experiment 2: Generating an LTE signal through the TX Path

The power amplifier (PA) output in each channel of the Qorvo RF card is routed back to an RF-ADC through a directional coupler, providing an observation path typically used for digital pre-distortion of the PA. In this experiment we shall generate an LTE standard-compliant signal in the digital domain from the RFSoC Explorer graphical user interface (GUI) running under MATLAB on the host PC. The digital signal data will be downloaded to the ZCU111 over TCP/IP and stored in DDR4 memory dedicated to the RF-DACs.

1. Return to DAC Tile 1. From 'Signal Source' of DAC 2, select 'Wireless Waveform'.



From the Wireless Waveform Generator, select **LTE (4G) Downlink RMC** as the Waveform Type.

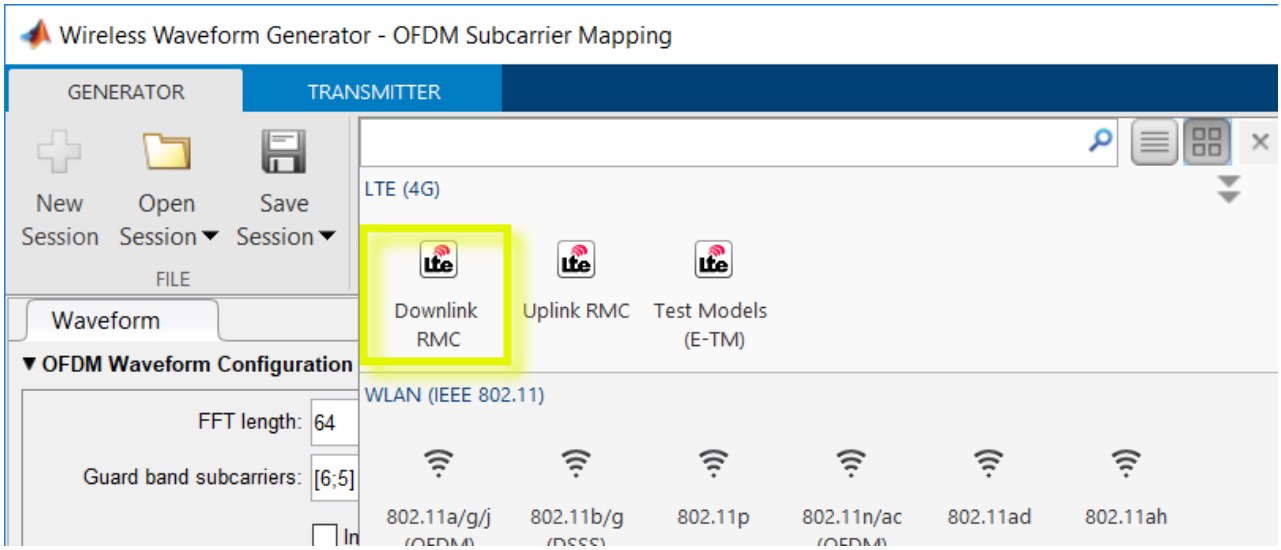


Figure 22 – MathWorks LTE Toolbox in Waveform Generator

In the 'Waveform' tab on the left, use the **Reference channel** dropdown menu to select **R.9 (Port 0, 100 RB, 64 QAM, CellRefP=1, R=3/4)**, then click **Generate** to create the waveform.

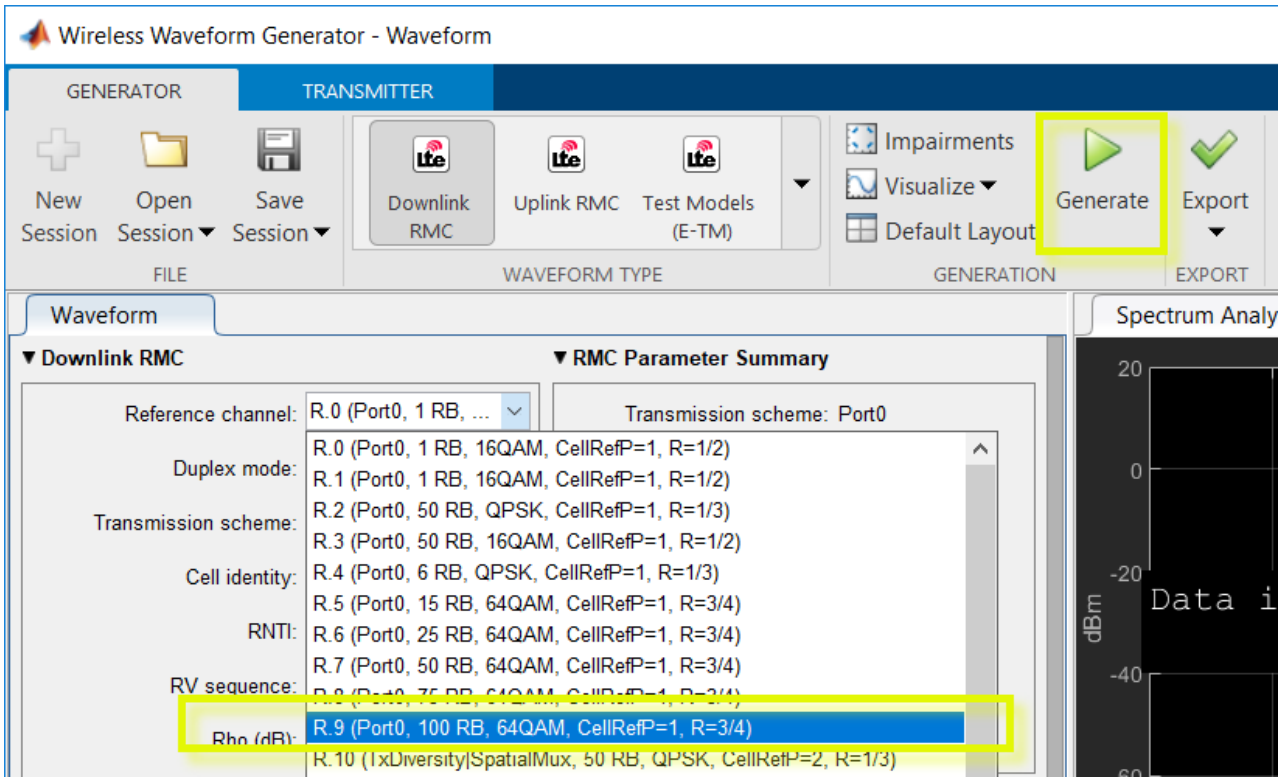


Figure 23 - MathWorks LTE Downlink R.9 Reference Channel Waveform

Next, use the Export dropdown menu in the top ribbon to select **Export to RFSoC Explorer**

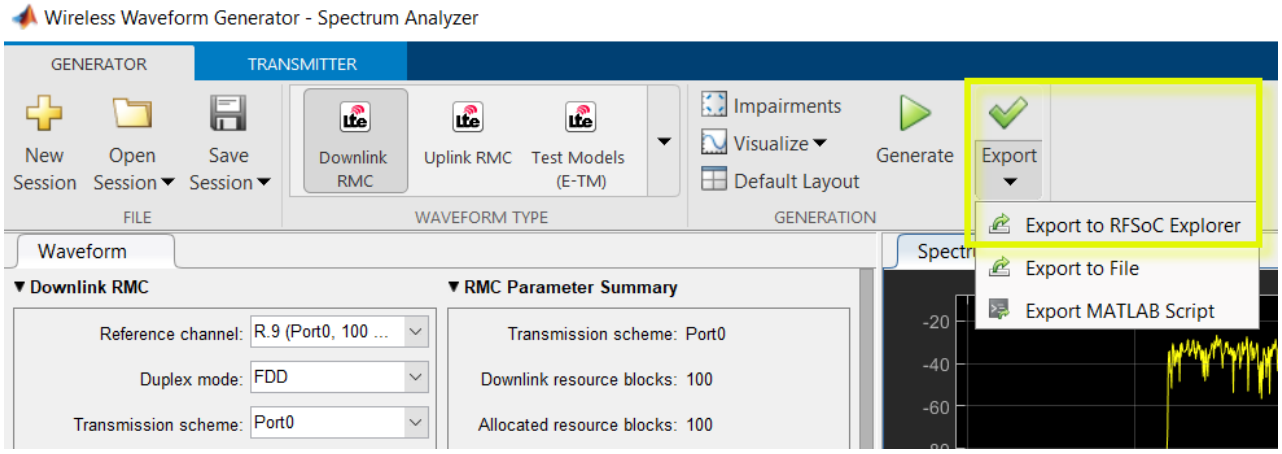
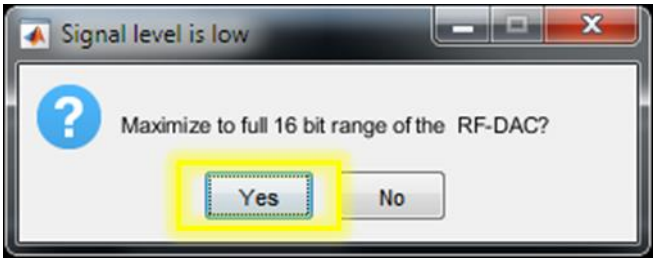
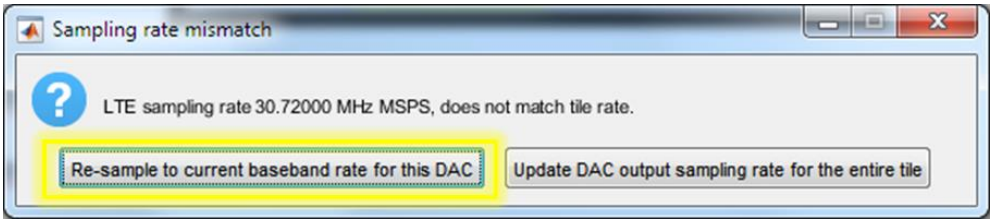


Figure 24 - Export Waveform Generator Signal to RFSoC Explorer

At the information dialog select ‘Yes’ to maximize the signal level to the full available dynamic range for the DAC.



2. By default the LTE waveform is generated at its native sampling rate of 30.72 MSPS. Accept the prompt to re-sample the signal at the current DAC sampling rate.



3. Scroll through the LTE parameters table to confirm the new sampling rate of 798.720 MSPS.

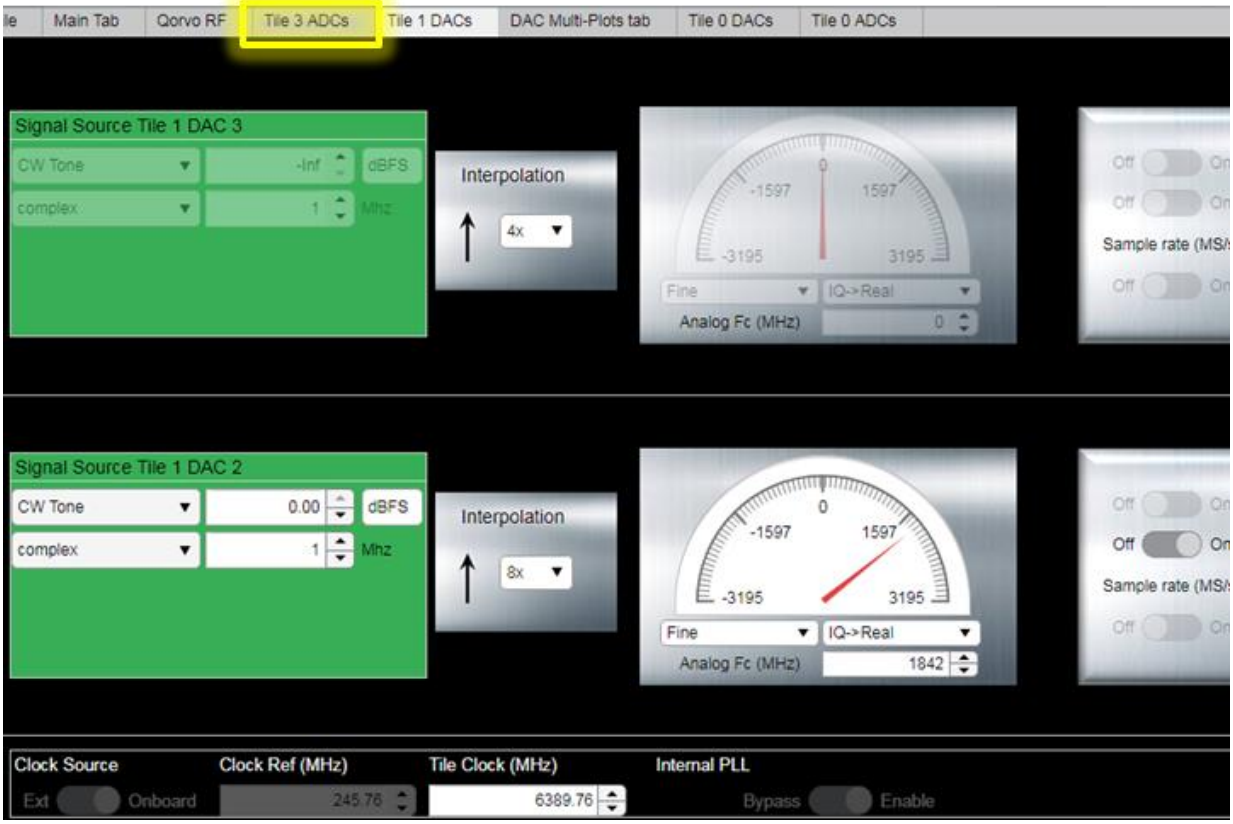
   Set interpolation factor to 8X. Set the complex mixer frequency to 1842 MHz. (See Figure **20**)

   Press 'Configure' to send the DUC parameters to the RFSoC RF Data Converter subsystem.

   Press 'Download' to transfer the signal data from MATLAB to the DAC memory buffer of ZCU111.

Figure 25- Generating a 20 MHz LTE waveform

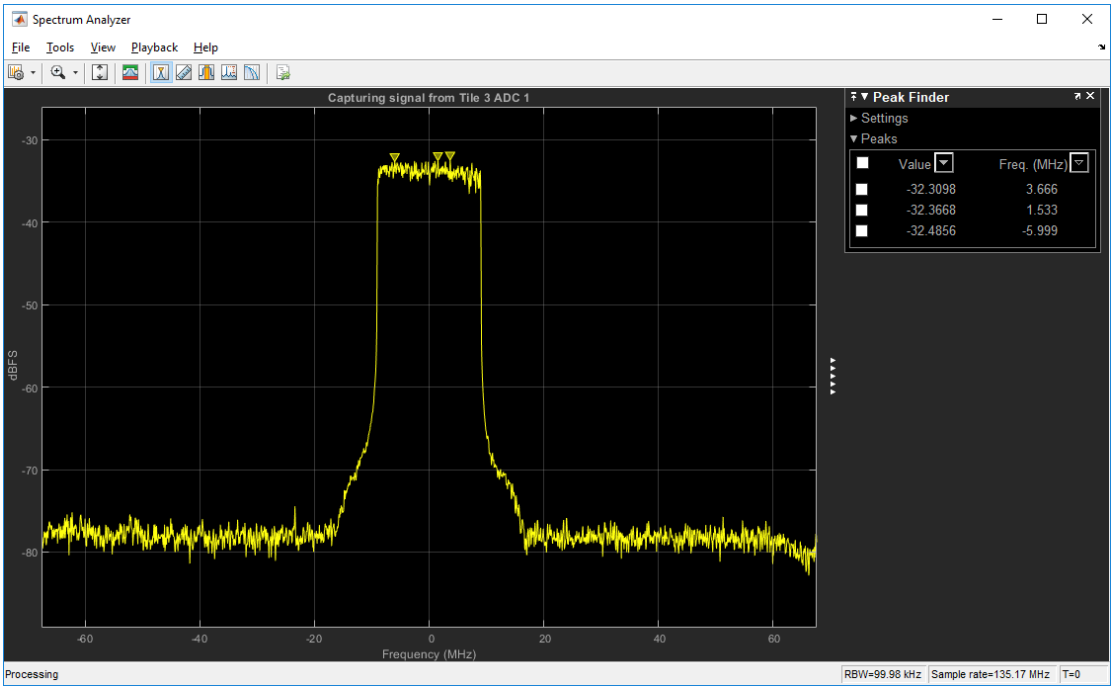
4. Select 'Tile 3 ADCs' within the Tab group at the top of the screen.



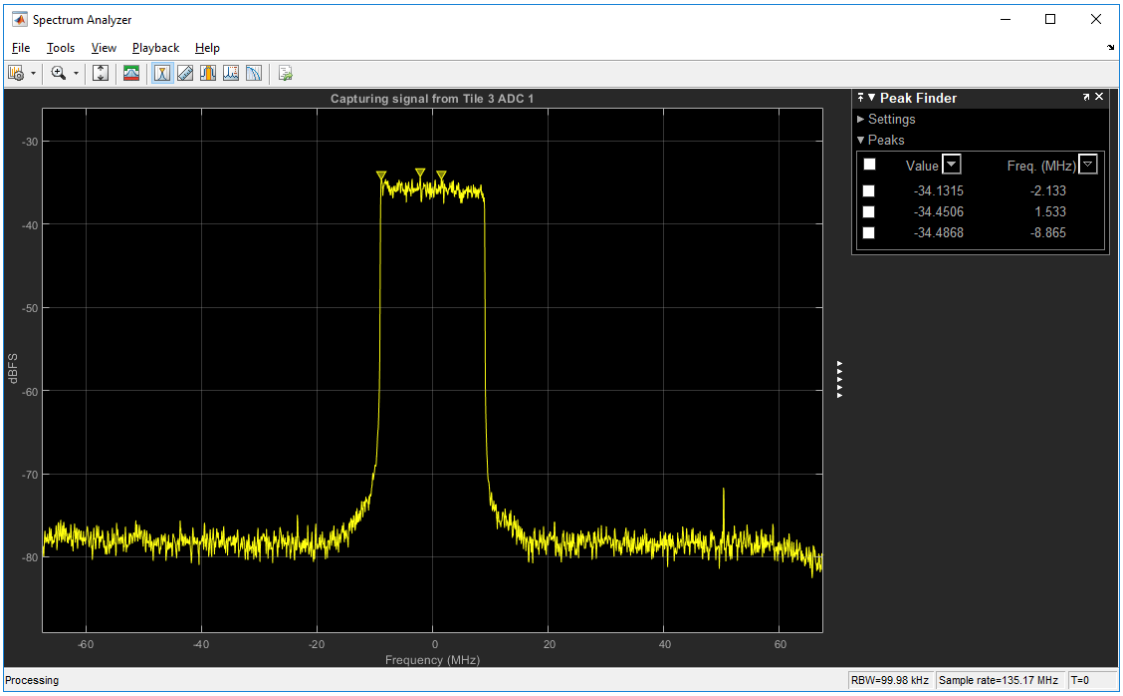
5. The ADC23 settings should have retained the state from the previous experiment.

   Press ‘single capture’.

6. Observe low level distortion products in the skirts of the output spectrum of the QPA9903 power amplifier. Clearly the input level into the PA is causing non-linear behavior as the amplifier approaches saturation.



Reduce the input level into the PA by typing '**a**' at the terminal command line, followed by a carriage return, then enter the value '**127**' to increase the attenuation and decrease the signal power entering the PA by 1.65 dB. Press 'single capture' to observe the PA now operating in the linear region.



This concludes experiment 2.

This introduction to the *Avnet Zynq UltraScale+TM RFSoC Development Kit with Qorvo RF Front End* has demonstrated usage of the Avnet RFSoC Explorer graphical user-interface to control the ZCU111 development board, generate and acquire signals through the Qorvo RF front-end card in the MATLAB environment.

For a comprehensive description of the functionality of the RF front-end, see *Qorvo 2-Channel RF Front-end 1.8 GHz Card Hardware User Guide* at www.avnet.com/rfsockit

Appendix A: Installation of USB UART Driver

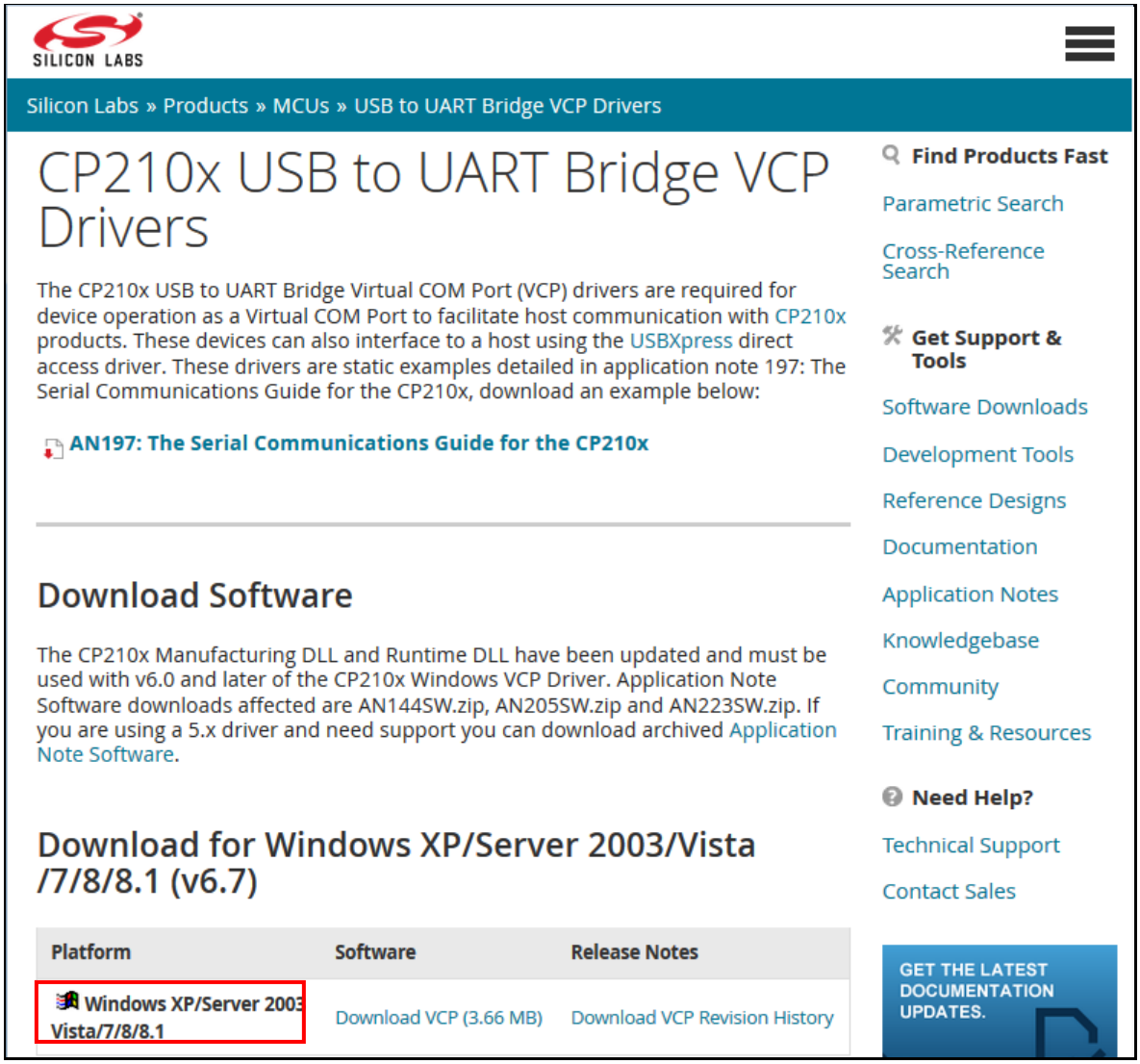
The Xilinx ZCU111 uses the Silicon Labs CP2102 USB-to-UART Bridge IC. This connects a PC's USB port to the evaluation board and looks like a UART to the PC. A virtual COM port will be created on the PC by means of a Silicon Labs CP2102 USB-to-UART bridge driver. Follow the instructions listed below to install the Silicon Labs drivers.

Download and Install the Required Software

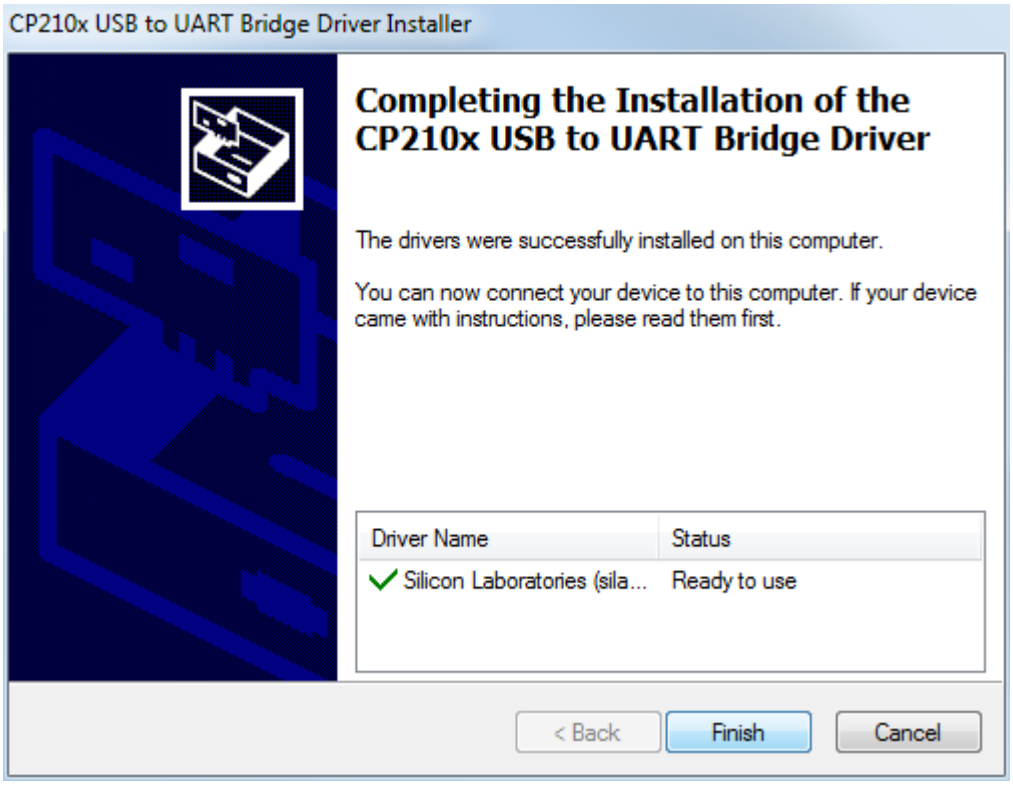
1. Using your web browser, navigate to the Silicon Labs website:

   http://www.silabs.com/products/mcu/pages/usbtouartbridgevcpdrivers.aspx

2. Download the **VCP Driver Kit** for your PC's operating system. Drivers for MacOS and Linux are also available.



3. Once the file is downloaded, extract the **CP210x VCP Driver Kit** archive. For example, for Windows XP/Vista/7 the file is CP210x_VCP_Windows.zip. Once the archive is extracted, open the folder where the archive was extracted and choose the correct installer for a 32-bit (CP210xVCPInstaller_x86.exe) or 64-bit (CP210xVCPInstaller_x64.exe) PC. The installer will guide you through the setup. Accept the license agreement and install the software on your PC. Click **Finish** button when completed.

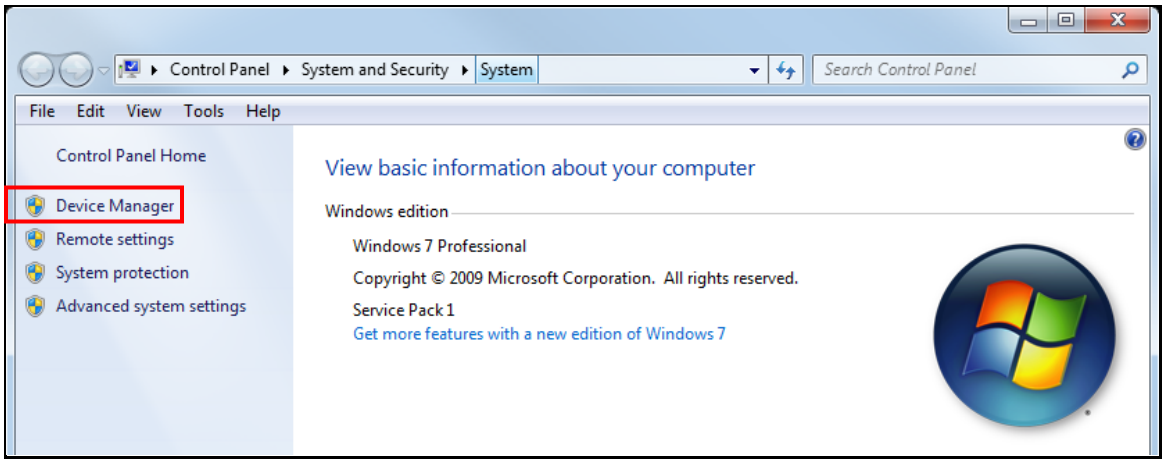


Determining the Virtual COM Port

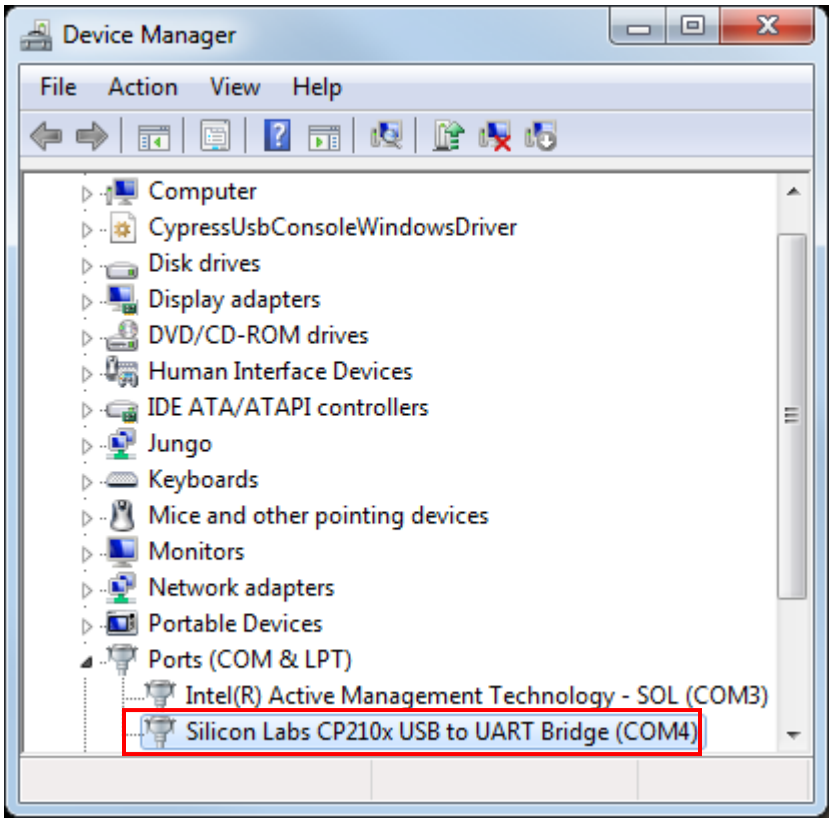
Now you can connect the ZCU111's USB-to-UART port to one of the USB ports on your PC. The new hardware detection will pop up and enumeration of the driver will start. Once finished a virtual COMx port is created and you are ready to setup a connection using Windows HyperTerminal or comparable serial terminal emulation utility. Follow these instructions to determine the COMx port assigned to the USB-to-UART bridge:

1. Open the Device Manager by right-clicking on 

, select Properties, then click on the Device Manager.



2. In the Device Manager, scroll down to Ports and expand the list. You will see the Silicon Labs CP210x USB to UART Bridge and its assigned COM port. In the example below, it is COM4. Make note of this COM port number for use with the serial terminal you will use elsewhere in this design tutorial. This concludes these USB UART driver and virtual COM port installation instructions.



Appendix B: Getting Support

Avnet Support

- If you have any questions about the Avnet Zynq UltraScale+ RFSoC Development Kit, Avnet's RFSoC Explorer application, or this tutorial please use the **UltraScale+ RFSoC Forum** on our element14 ZedBoard Community page: https://www.element14.com/zedboardcommunity

- To access the most current collateral, visit the product page at www.avnet.com/rfsockit

MathWorks Support

For questions regarding MathWorks software and support for the Avnet Zynq UltraScale+ RFSoC Development Kit, please contact rfsoc@mathworks.com

Regulatory Compliance Information

REGULATORY COMPLIANCE INFORMATION

FCC WARNING

This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Use of the kit should be limited to a development lab environment only.

CE WARNING

This evaluation kit is for use by professionals for their research and development purposes. The kit may not be put into service for use on a regular basis, or integrated into an end product (Annex I.4 of the RED). This kit is does not bare the CE mark of certification. As such, this kit may be operated only within the requirements of RED section 1.6.2.5, Custom-built evaluation kits.

Revision History

Date	Version	Revision
27 Sep, 2019	1.0	Initial Release
03 Oct, 2019	1.1	Added Regulatory Compliance Information
25 Oct, 2019	1.2	Updated MATLAB required version. Updated SW installation.
31 Oct, 2019	1.3	Updated app startup method as a MATLAB Add-On app
14 Nov, 2019	1.4	Updated LTE Experiment for Waveform Generator in R2019b
18 Nov, 2019	1.5	Updated waveform used in LTE Experiment
26 Nov, 2019	1.6	Revised MATLAB SW Requirements. Revised SD card preparation instruction.
05 Jun, 2020	1.7	Updated SD card formatting instructions. Updated hyperlinks for setting up USB-Serial. Revised for new Qorvo 2-Channel “loopback enabled” revision (AES-LPA-QRF18000-RVS-G) Added section - Regulatory Compliance Information
24 Feb, 2023	1.8	Added SD card image link for support of Avnet RFSoC Explorer version v2.0.0 and later

[i] Avnet Qorvo 2-Channel RF Front-end 1.8 GHz Card Hardware User Guide www.avnet.com/rfsockit

[ii] https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_1/pg269-rf-data-converter.pdf

[iii] https://github.com/Xilinx/embeddedsw/tree/master/XilinxProcessorIPLib/drivers/rfdc