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White Paper

Achieve Fast and Accurate Over-Current Detection Using Optically Coupled Sigma-Delta Modulators

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Introduction

In an industrial motor control system, sensing and feedback of various parameters such as motor phase, DC bus current and voltage, torque, direction, and speed are required for proper operation of the system. As the trend of the system moves towards higher precision, power, speed, multi-axis, and multi-directional, these requirements become increasingly important. As the motor encoder measures the torque, speed, and direction, the sigma-delta modulator provides high accuracy, high linearity, wide dynamic range, fast-response current, and voltage sensing. Traditionally, current sensing is done by using current transformer (CT) or a Hall effect sensor (HES), but these solutions are bulky, expensive, and less accurate over operating temperature. A smaller, low-cost solution can be realized by directly connecting a shunt resistor to the sigma-delta modulator. Phase current flows through the shunt resistor with a resistance value selected such that the maximum current range corresponds to an optimum low voltage of about ±50 mV (for ACPL-C799) or ±200 mV at the input of the sigma-delta modulator. At this low voltage, power dissipation loss across the shunt resistor is minimized. Figure 1 illustrates the phase current sensing and DC bus voltage and current sensing of a sigma-delta modulator in a motor control system.

Optically Coupled Sigma-Delta Modulators

One of the most expensive devices in a motor control system is a power semiconductor switching device like the IGBT or power MOSFET. Switching at high frequency, these power devices introduce unintended noise and high-voltage transients across the control system. This high-frequency transient may affect the normal operation of the sensitive, costly microcontroller. Sigma-delta modulators in combination with superior optical coupling isolation technology deliver high noise margins and excellent immunity against isolation mode transients. With a minimum distance through insulation (DTI) of 0.5 mm, these sigma-delta modulators provide reliable double protection and a high working voltage suitable for fail-safe designs. This proven isolation performance is superior to magnetic or capacitive-based isolators, where DTI is only a third of 0.1 mm.

Sigma-delta modulators[1,2,3,4] convert the analog input signal into high-speed single-bit data streams by means of a second-order sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. This white paper specifically discusses the ACPL-796J and ACLP-C799 optically isolated sigma-delta modulators.

1. "ACPL-C799 Optically Isolated ±50 mV Sigma-Delta Modulator", pub-005830 Data Sheet, August 26, 2016
2. "ACPL-C797 Optically Isolated ±50 mV Sigma-Delta Modulator", AV02-2581EN Data Sheet, November 18, 2013
3. "ACPL-796J Optically Isolated Sigma-Delta Modulator", AV02-1670EN Data Sheet, March 6, 2015
4. "ACPL-798J Optically Isolated Sigma-Delta Modulator with LVDS Interface", AV02-4339EN Data Sheet, August 8, 2015

There are two types of sigma-delta modulators, based on whether the clock source is internally built-in or externally provided to the modulator. For the internally clocked type, a 10 MHz or 20 MHz fixed clock is built in at the primary side of the isolation barrier where the sigma-delta encoder is located. The clock signal is encoded together with the data and coupled across the isolation barrier to the secondary side of the isolation barrier where the clock and data signals are decoded. The externally clocked-in type receives the clock signal at frequency ranges from 5 MHz to 25 MHz at the secondary side and then it is coupled across the isolation barrier to the primary side. At the secondary side of both types of modulators, data is decoded into a high-speed data stream of digital ones and zeros. Figure 2 illustrates the simplified block diagrams of internally and externally clocked sigma-delta modulators.

Figure 1: Sigma-Delta Modulator Used in Output Phase with DC Bus Voltage and Current Sensing

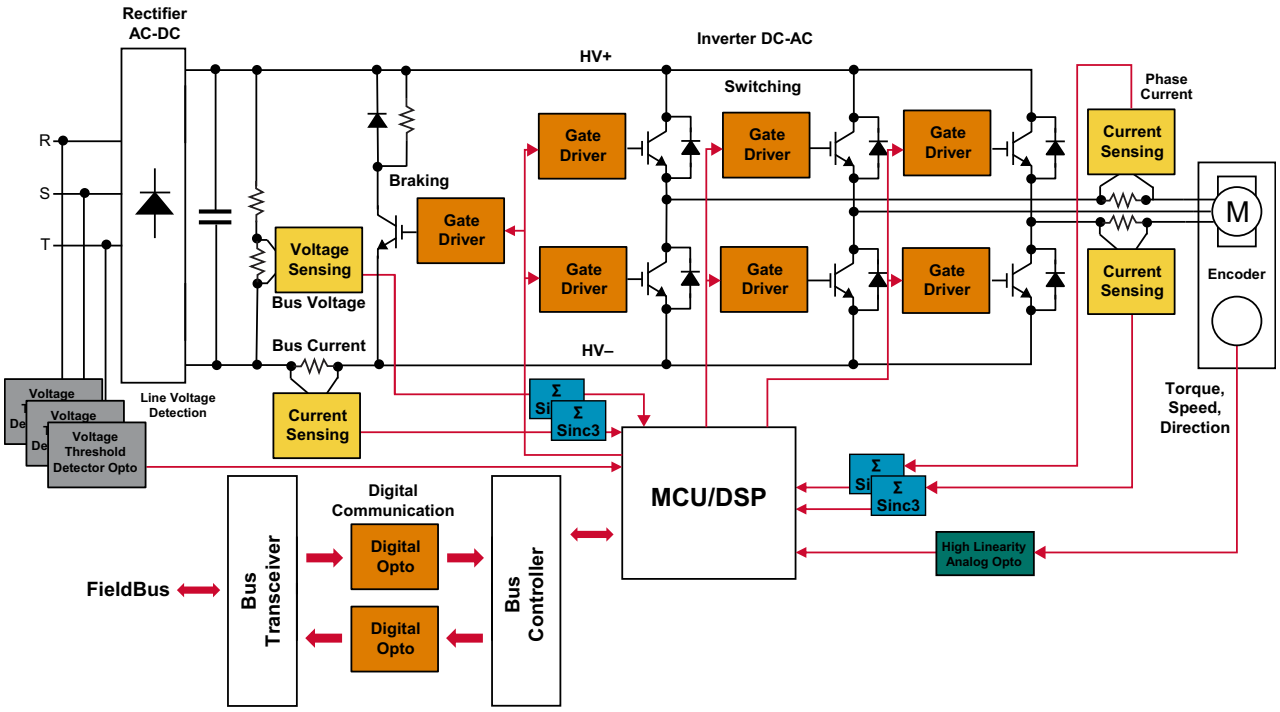
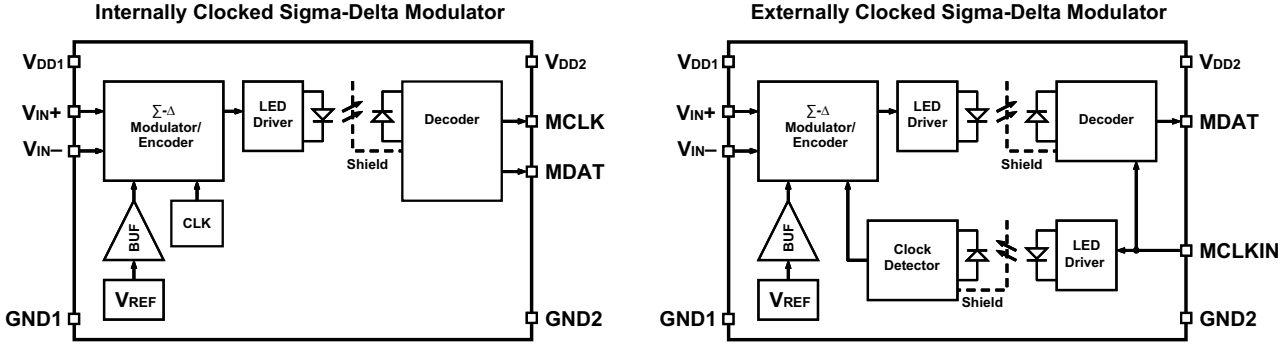


Figure 2: Simplified Block Diagrams of Internally and Externally Clocked Sigma-Delta Modulators



Original analog input information is represented by the density of digital ones or zeros at data output. Table 1 shows the input voltage with an ideal corresponding density of ones at the modulator data output and ADC code. The modulator data received on the isolated side is then sent to a processor for filtering and conversion. A Sinc3 decimation filter can be implemented on an FPGA or microprocessor to recover the desired signal. The decimation filter averages or decimates the high-speed oversampled bit stream to a lower rate by a factor commonly known as decimation ratio. By selecting a higher decimation ratio, better resolution of the recovered data can be achieved at the expense of longer filter delay time.

Table 1: Sigma-Delta Modulator Input Voltage with the Corresponding Density of Ones and Zeros at Modulator Data Output and ADC Code

Analog Input	ACPL-796J Voltage Input (±50 mV)	ACPL-C799 Voltage Input (±200 mV)	Density of Ones	Density of Zeros	ADC Code (16b Unsigned Decimation)
Full-Scale Range	640 mV	160 mV	—	—	—
+Full-Scale	+320 mV	+80 mV	100%	0%	65,535
+Recommended Input Range	+200 mV	+50 mV	81.25%	18.75%	53,248
Zero	0 mV	0 mV	50%	50%	32,768
–Recommended Input Range	–200 mV	–50 mV	18.75%	81.25%	12,288
–Full-Scale	–320 mV	–80 mV	0%	100%	0

Fast-Response Over-Current Detection

Over-current or short-circuit conditions in an IGBT can occur due to a phase-to-phase short, a ground short, or a shoot through. Typically, an IGBT can survive short-circuit conditions up to 10 µs[5] before failure. Within this time period, a fault must be generated as feedback to the microcontroller to trigger an immediate shutdown procedure within the system. One method is to detect the over-current directly from sensing the phase current using the sigma-delta modulator. Usually, a longer post-processing time of the sigma-delta modulator output data is required to achieve higher resolution of the measured phase current. As a result, over-current may not be detected quickly enough to shut down the entire control system.

One implementation[6] uses two Sinc3 filter paths: one with a decimation ratio of 256 for higher resolution and another with a decimation ratio of 32 for fast over-current detection. A typical application using a 20 MHz clock frequency requires about 12.8 µs filter delay time with a decimation ratio of 256 and 1.6 µs with a decimation ratio of 32. Besides the filter delay, an additional 0.5 µs must be considered for the sigma-delta processing and for latency across the isolation barrier. To shorten the response time further, a simple fault-detection logic block can be used in place of the low decimation ratio Sinc3 filter. This method detects a pre-programmed continuous N-bits of one or zero directly from the data output of the sigma-delta modulator without going through further processing or conversion. This implementation is illustrated in Figure 3 and Figure 4.

5. J. Li, R. Herzer, R. Annacker, B. Koenig, "Modern IGBT/FWD Chip Sets For 1200 V Applications," Semikron Elektronik GmbH, 2007.
6. "Safe and Accurate Isolated Current Sensing in Motor Control using Optically Isolated Sigma-Delta Modulators", AV00-0278EN Technical Note, December 18, 2013

Figure 3: Output Data of an ACPL-796J Connected to Separate Paths Inside the FPGA (For High-Resolution Conversion and Fast Response Detection)

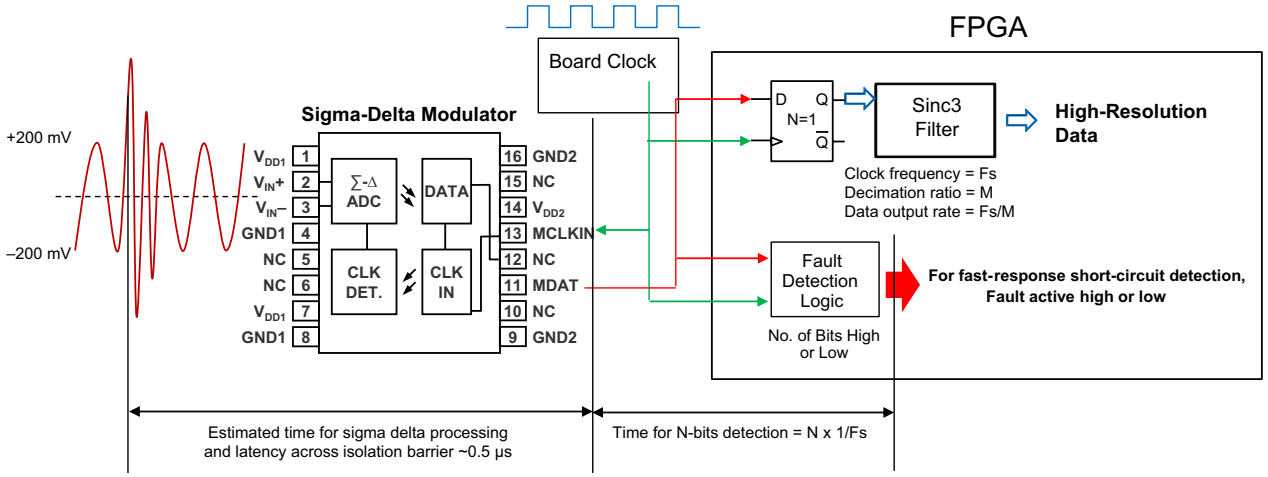
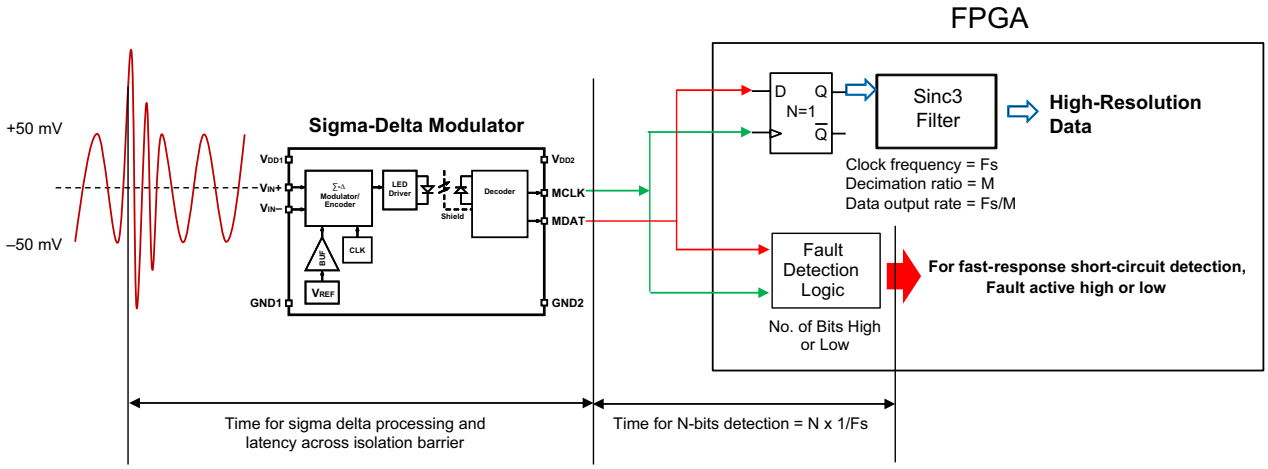


Figure 4: Output Data of an ACPL-C799 Connected to Separate Paths Inside the FPGA (For High-Resolution Conversion and Fast Response Detection)



Fault detection logic can be easily implemented in an FPGA or microcontroller. One method is to implement an N array of D-type flip-flops. The outputs of the N number of flip-flops are connected to an AND gate for N-bits high detection and to a NOR gate for N-bits low detection. When the first bit of a stream of continuous high or low bits reaches the last flip-flop (n=N), the AND gate output turns logic high for continuous N-bits logic 1 (high). Similarly, the NOR gate output goes high when continuous N-bits logic 0 (low) are detected. This provides fault feedback to the microcontroller. Figure 5 shows the fault detection logic for continuous 20-bits high and Figure 6 shows continuous 20-bits low. To demonstrate this, a fault detection logic block was implemented in the ACPL-C799 Xilinx FPGA evaluation board (as shown in Figure 7) and actual response time was measured.

Figure 5: Example of Fault Detection Logic for Continuous 20-Bits High

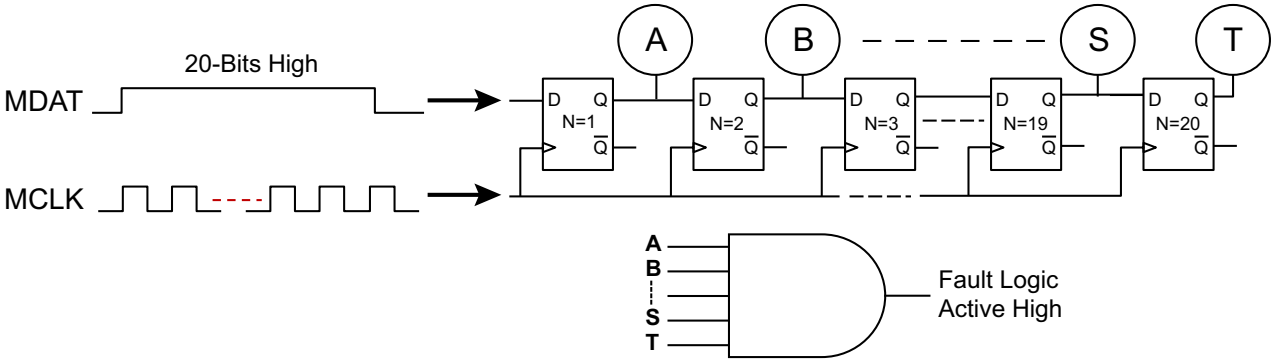


Figure 6: Example of Fault Detection Logic for Continuous 20-Bits Low

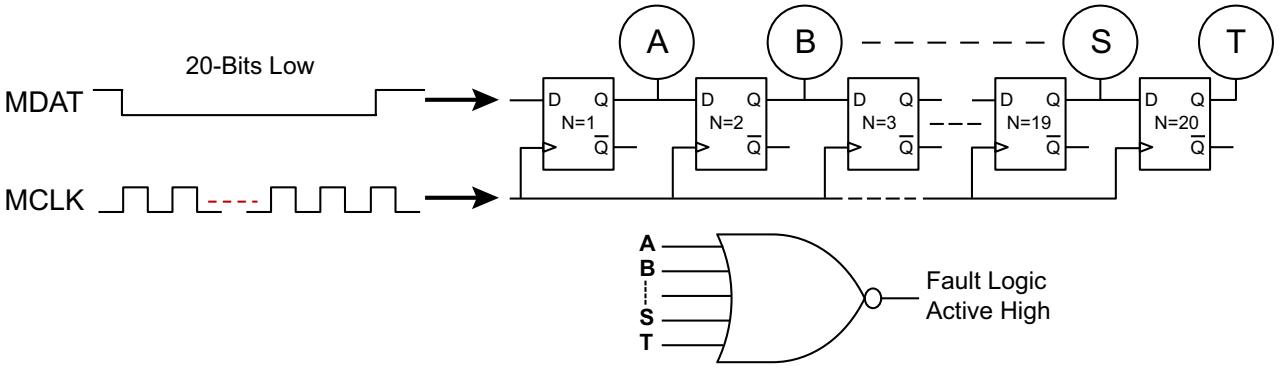
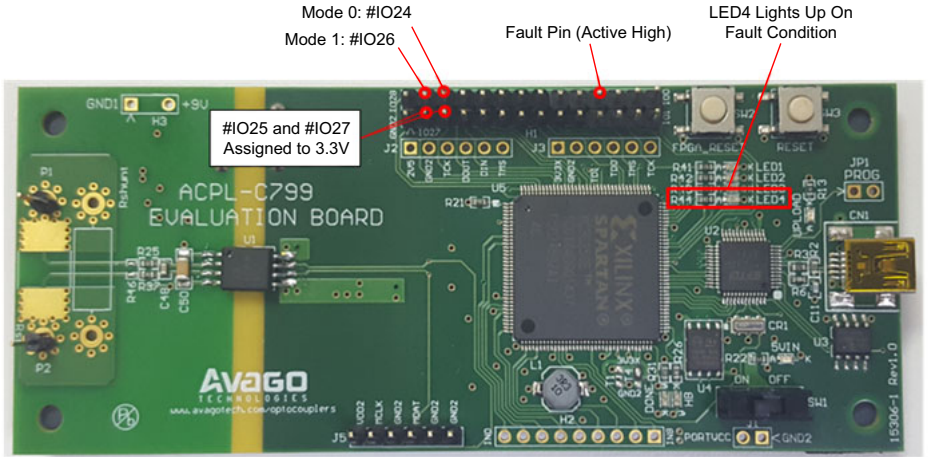


Figure 7: Over-Current Fault Detection Implemented on the ACPL-C799 Xilinx FPGA Evaluation Board

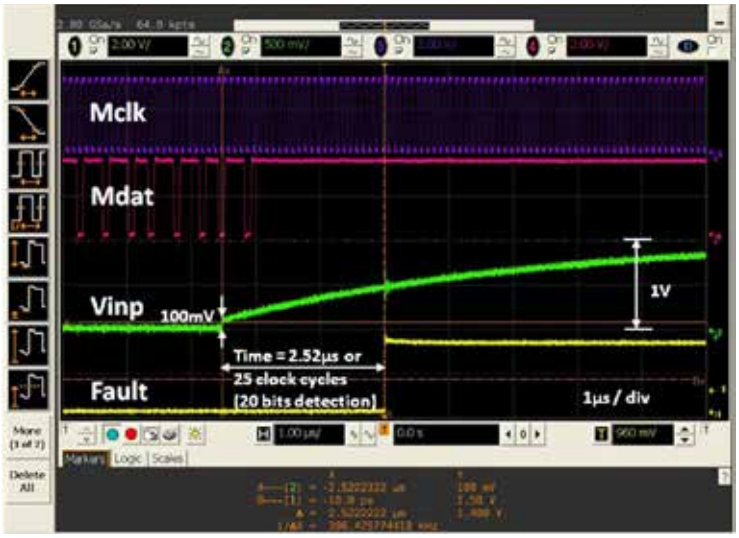


Mode (1:0)	Fault Detection
01	10-bits continuous low or high
10	15-bits continuous low or high
11	20-bits continuous low or high

As described in Table 1, the densities of bit 1 and bit 0 are proportionate to the voltage level at the input of the sigma-delta modulator. A continuous stream of 20-bits logic 1 is detected at an input voltage level of +270 mV for the ACPL-796J and +63 mV for the ACPL-C799. Likewise, a continuous 20-bits logic 0 is detected at –270 mV for the ACPL-796J and –63 mV for the ACPL-C799. If a shunt resistor is selected such that an optimum recommended input voltage range of ±200 mV for ACPL-796J and ±50 mV for ACPL-C799 is measured at the input of the sigma-delta modulator corresponding to a target-measured current range, then a stream of continuous 20-bits high or low will not be present at the output during the normal condition. However, when there is an over-current event, the input voltage rises immediately beyond the recommended voltage level range. By then, a continuous stream of 20 or more high or low bits is sent out from the sigma-delta modulator output. The fault detection logic captures this output data and triggers a fault signal immediately within 1.54 µs (for the ACPL-796J) or 2.52 µs (for the ACPL-C799) from the start of the over-current event.

Figure 8 illustrates the actual measurement for a 20-bits high detection on the ACPL-C799 whereby time response includes 20 clock cycles (at 10 MHz frequency) and about 5 clock cycles of additional delay required for sigma-delta processing, the latency across the isolation barrier, and flip-flop delay.

Figure 8: Measured Response Time for 20b High Detection on the ACPL-C799



For the ACPL-796J, a further reduction of response time to sub-1 µs can be achieved if the input voltage range of the sigma-delta modulator is optimized to ±50 mV. When an over-current event occurs, the input voltage level goes beyond ±100 mV and corresponds to 5-bits continuously high or low at the sigma-delta output.

For the ACPL-C799, a further reduction of response time can be achieved if 15-bit or 10-bit detection is used. However, a smaller input operating range results in a lower signal-to-noise ratio (SNR) during normal operation.

Table 2 shows various configurations of N-bit detection versus response time and the suggested normal operating input range.

Table 2: N-Bits Detection vs. Response Time and Suggested Normal Operating Input Range

Device	Continuous N-Bits High or Low	Input Voltage Corresponding to Continuous N-Bits High or Low	Suggested Normal Input Operating Range	Clock Frequency	Measured Response Time
ACPL-796J	5 bits	±100 mV	±50 mV	20 MHz	773 ns
	10 bits	±205 mV	±100 mV		1.01 µs
	15 bits	±240 mV	±200 mV		1.36 µs
	20 bits	±270 mV	±200 mV		1.54 µs
ACPL-C799	10 bits	±47 mV	±30 mV	10 MHz	1.39 µs
	15 bits	±57 mV	±40 mV		2.02 µs
	20 bits	±63 mV	±50 mV		2.52 µs

Conclusion

Fast shutdown of the motor control system during an over-current event prevents catastrophic damage to the expensive power semiconductor switching devices. Optically coupled sigma-delta modulators not only provide high-resolution current measurement with proven and reliable fail-safe isolation protection, but additional fast-response over-current fault detection functionality can be easily implemented by feeding the single-bit stream output data directly to a simple bit-stream detection circuitry. This can be accomplished without even having to change hardware configuration or increase component count.