



Application note No. 3: using high-level synthesis to accelerate image processing algorithms

Project objectives

This is the final of three application notes for creating imaging solutions using the 96Boards onsemi Dual Camera Mezzanine and Ultra96V2.

This project demonstrates how to leverage Xilinx Vitis HLS to implement image processing algorithms using C / C++ algorithms.

The expected outcome is a project running on the Avnet Ultra96V2 board with the 96Boards onsemi Dual Camera Mezzanine, which includes a simple Vitis HLS block that manipulates the output video.

This application note is the final of three application notes based on creating imaging solutions using the 96Boards onsemi Dual Camera Mezzanine and Ultra96V2, as this project requires the use of embedded Linux. The project outlined in this application note is created on a Xilinx-supported 64-Bit Linux operating system.

Getting started: requirements

The following hardware is required to follow this series of application notes.

- Ultra96V2
- Ultra96V2 power supply
- 96Boards onsemi Dual Camera Mezzanine
- SD card
- JTAG / USB adaptor
- Display port capable monitor
- Mini display port cable
- 16 GB SD card

To implement this series of application notes, you need the following Xilinx software installed:

- Vitis 2020.1, includes Vivado 2020.1.
- PetaLinux 2020.1
- Git
- Terminal application

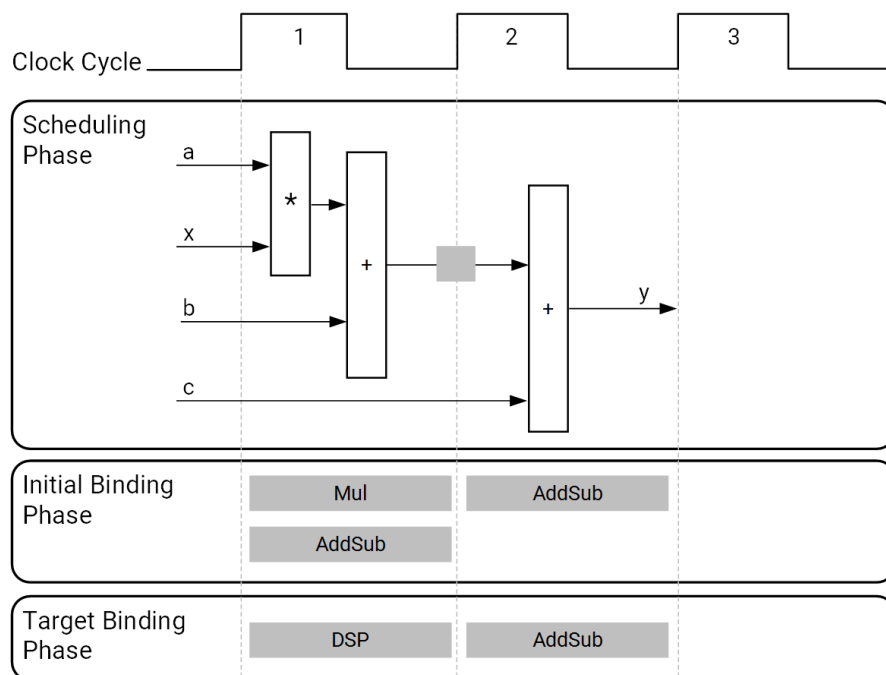
You'll need a few licenses for this implementation. Bitstreams for the Xilinx ZU3EG device can be generated license-free as part of the Xilinx Vivado webPACK. However, some of the IP used within this design requires an additional license. This license is provided with the Ultra96V2 and is marked "OEM Zynq ZU3 Ultra96 Vivado Design Edition with SDSoc Voucher Pack." Redeem this license and install it on the machine you're using to implement the project. Once it is installed, you can use the license manager to see the licensed IP, including the On-Screen Display (OSD).

What is Vitis HLS?

Vitis HLS enables the developer to create an IP module to be implemented in the Vivado design using higher-level languages than Verilog and VHDL. Developers using Vitis HLS leverage the increased productivity provided by using higher-level languages such as C and C++. To further increase productivity, several HLS-compatible libraries are provided for a range of applications, such as quantitative finance, linear Algebra and image processing, to name a few. These domain-specific libraries are also supported by a range of common libraries.

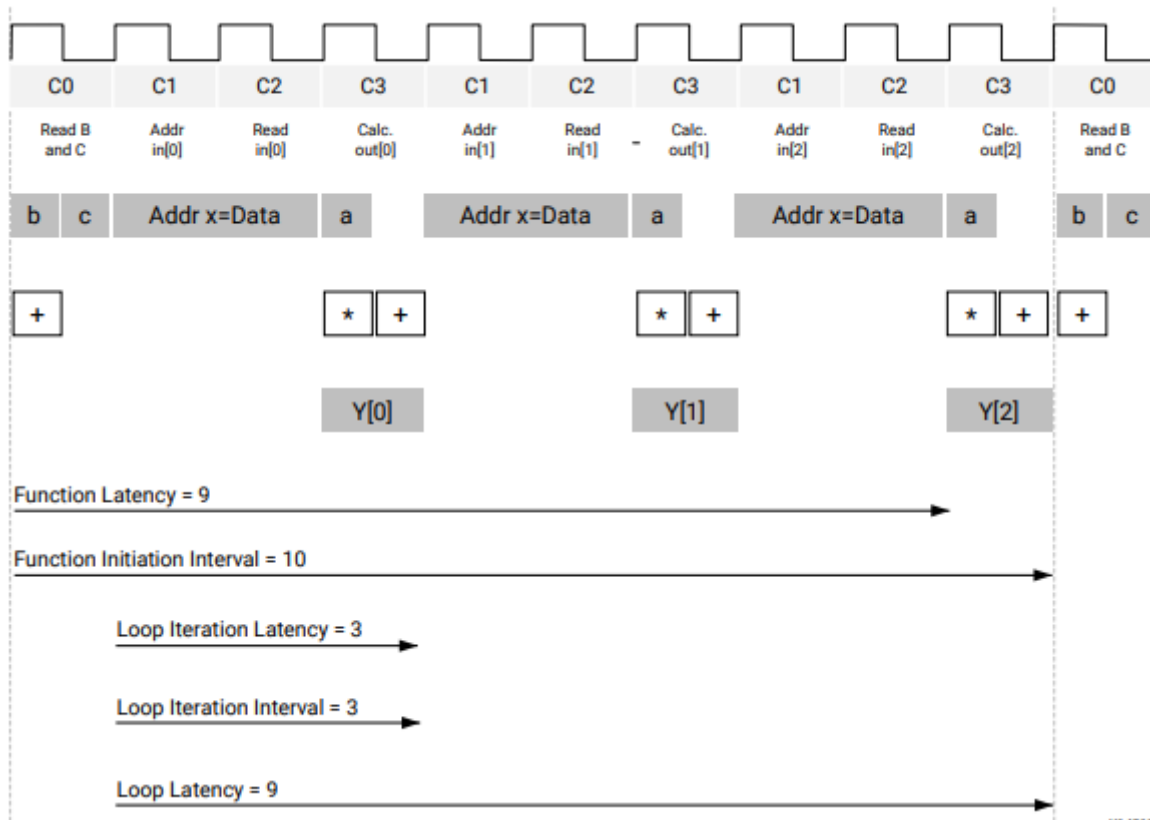
The benefit of using C/C++ for development of IP is that it enables a much faster development time, as C/C++ is inherently untimed and results in much faster verification. Synthesis from C / C++ to RTL, such as Verilog or VHDL, is called high-level synthesis and takes three stages.

1. **Scheduling** or assignment of operation in the untimed C/C++ operations to clock cycles based upon the target device and the required clock period
2. **Binding** of the design to logic elements available in the target device (for example, BRAM, DSP elements or LUT and Registers)
3. **Control Logic Extraction** or implementation of control structures necessary to control the behavior of the IP block.



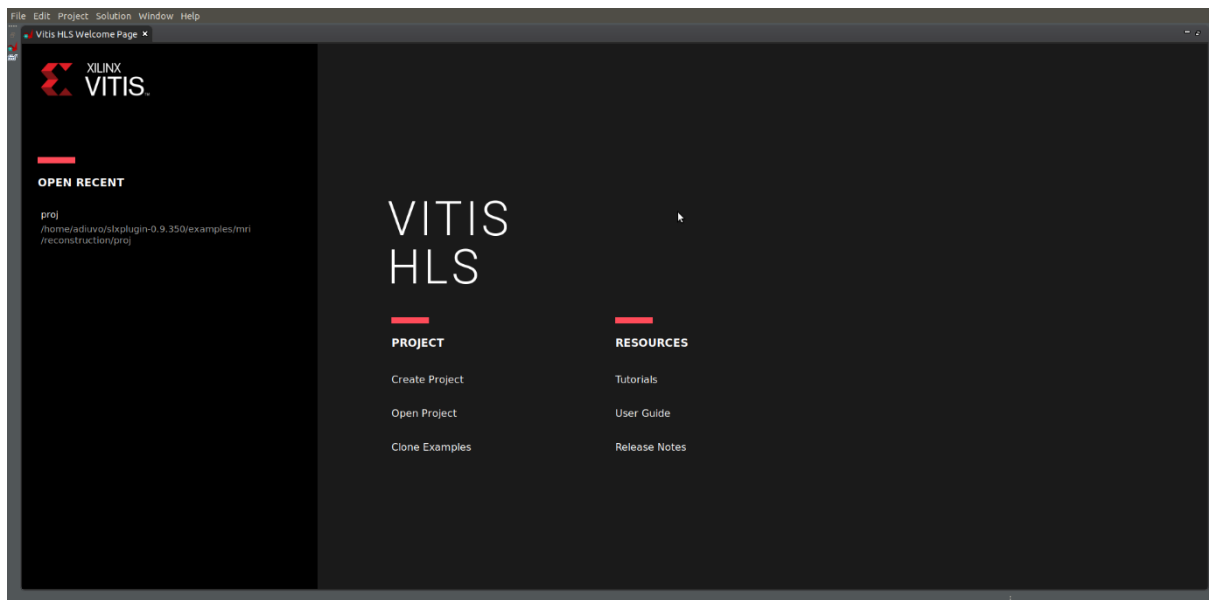
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To control the module interfacing, throughput and latency performance of the implemented IP modules in Vivado, the designer can leverage optimization pragmas that control the decisions made by the HLS engine.

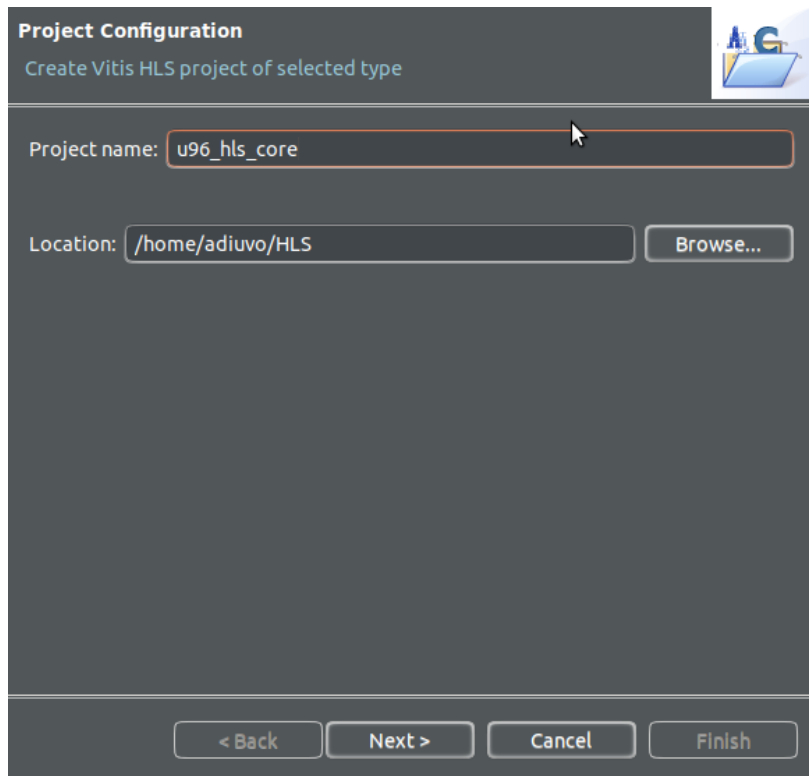


Creating the Vitis HLS IP core

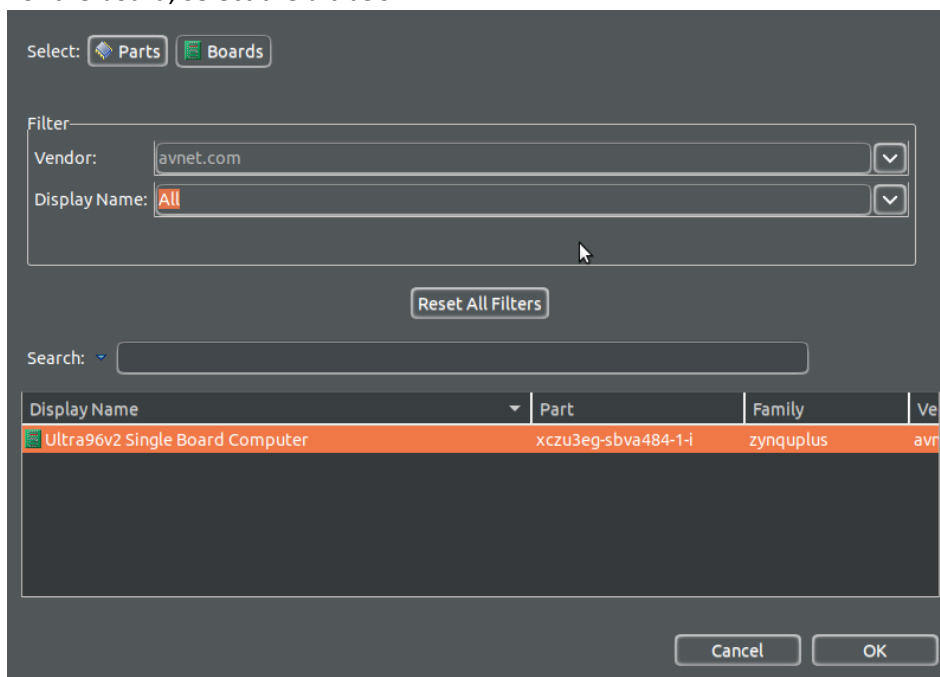
1. Open the Vitis HLS tool and select Create Project.



2. Select a location to save the project and a project name.



3. Leave the Source and test bench file addition empty and click next on both.
4. For the board, select the ultra96V2.



5. Leave the solution configuration unchanged and click Finish.

Solution Configuration
Create Vitis HLS solution for selected technology

Solution Name:

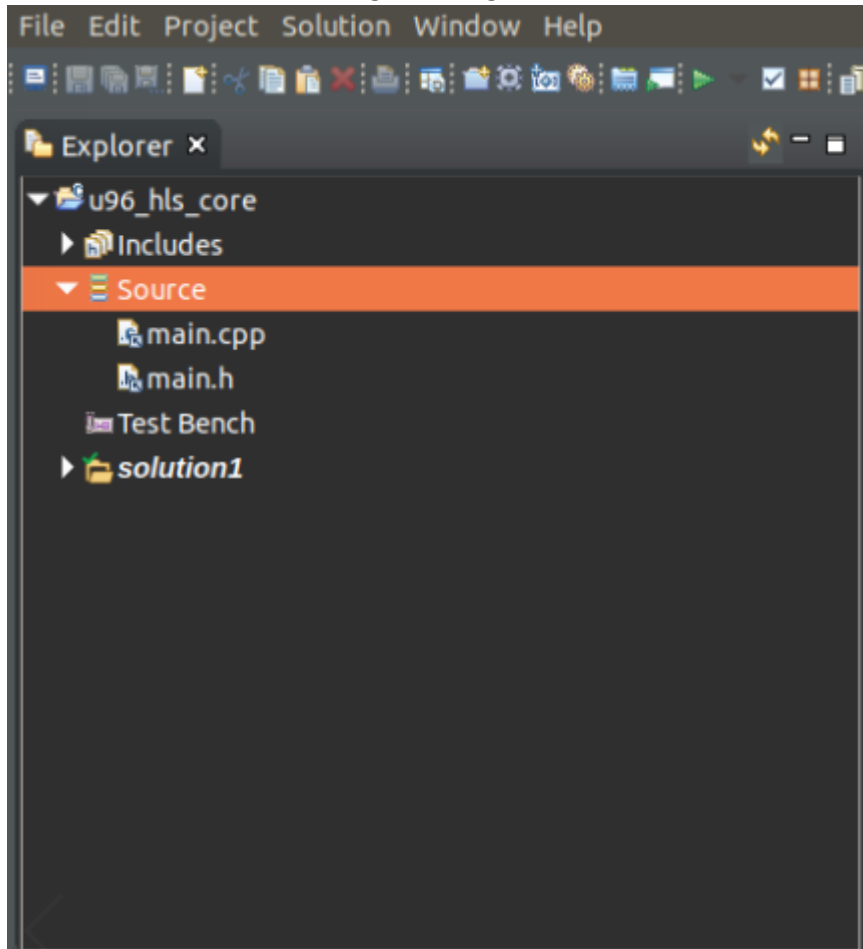
Clock
Period: Uncertainty:

Part Selection
Part: **Ultra96v2 Single Board Computer (xczu3eg-sbva484-1-i)**

Flow Target
 Configure [several options](#) for the selected flow target

6. Once the project opens, create two new files under the source tab by right clicking and selecting New File. Name the first file main.c and the second file main.h. These will be the

files into which we are entering our design.



7. In the main.c file, copy and paste the code below

```

#include "main.h"
#include "stdint.h"

void video_top(AXI_STREAM& vidip, AXI_STREAM& vidop, ap_uint<1> invert){
#pragma HLS INTERFACE axis port=vidip
#pragma HLS INTERFACE axis port=vidop
AXIYPE dataInA;
AXIYPE dataOutB;
uint16_t pix1, pix2;

while(1){
    dataInA = vidip.read();
    dataOutB = dataInA; // copy all fields data, dest, keep, tlast, tuser, id, strb,
    pix1 = (uint16_t) (dataInA.data >>16); //shift pixels by 16 bit
    pix2 = (uint16_t) (dataInA.data);
    if (invert ==1){ //do we want to wait for external trigger or free run
        dataOutB.data = ((16384 - pix1) <<16) | (16384 - pix2);
    }
    else {
        dataOutB.data = dataInA.data;
    }
    vidop.write(dataOutB);
}
}

```

8. Do the same with the code below for the main.h

```

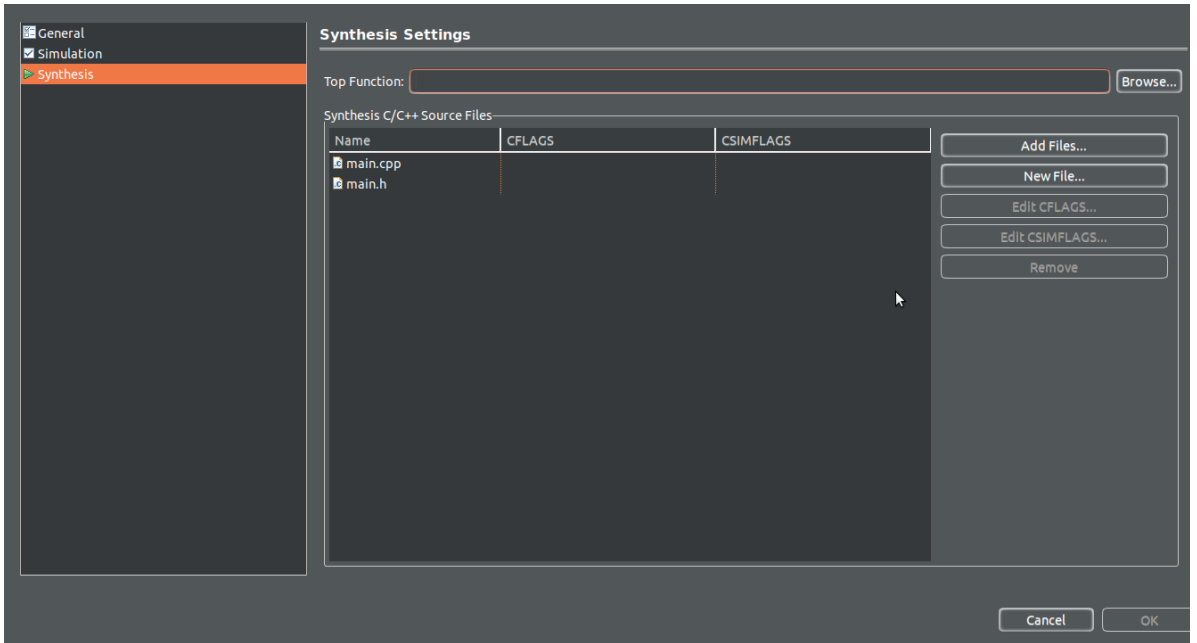
#include <ap_fixed.h>
#include <ap_axi_sdata.h>
#include "ap_utils.h"
#include "hls_stream.h"

#define WIDTH 32

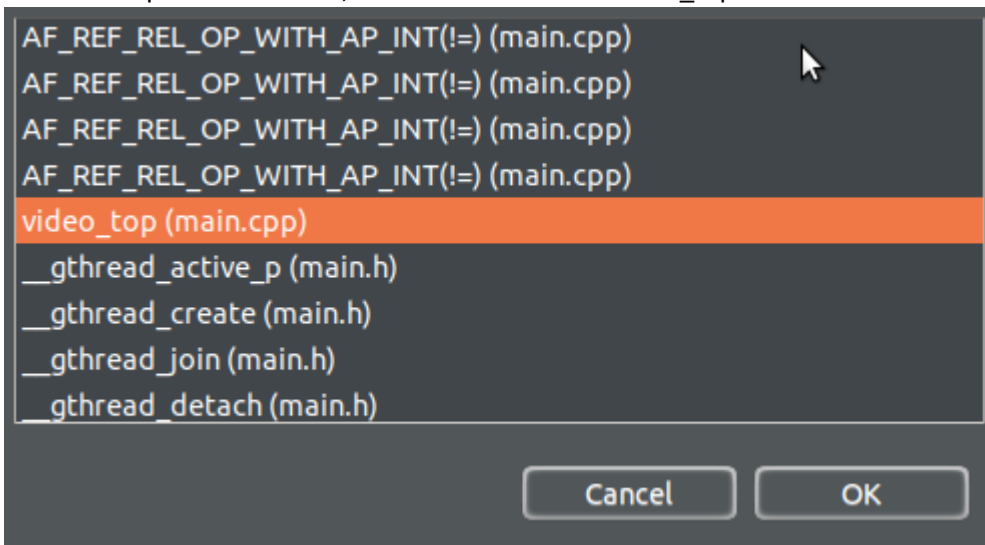
typedef ap_axiu< WIDTH, 1, 1, 1> AXIYPE;
typedef hls::stream<AXIYPE> AXI_STREAM;
void video_top(AXI_STREAM& vidip, AXI_STREAM& vidop, ap_uint<1> invert);

```

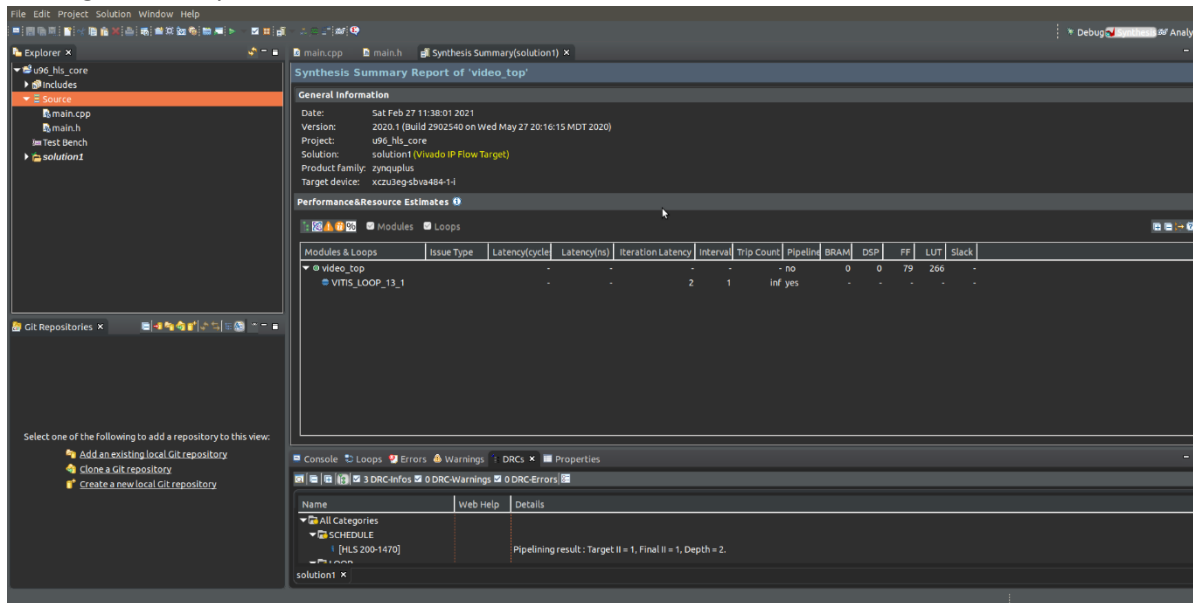
9. Once the code is entered, the next step is to define the top-level function that will be synthesised. Open the project settings.



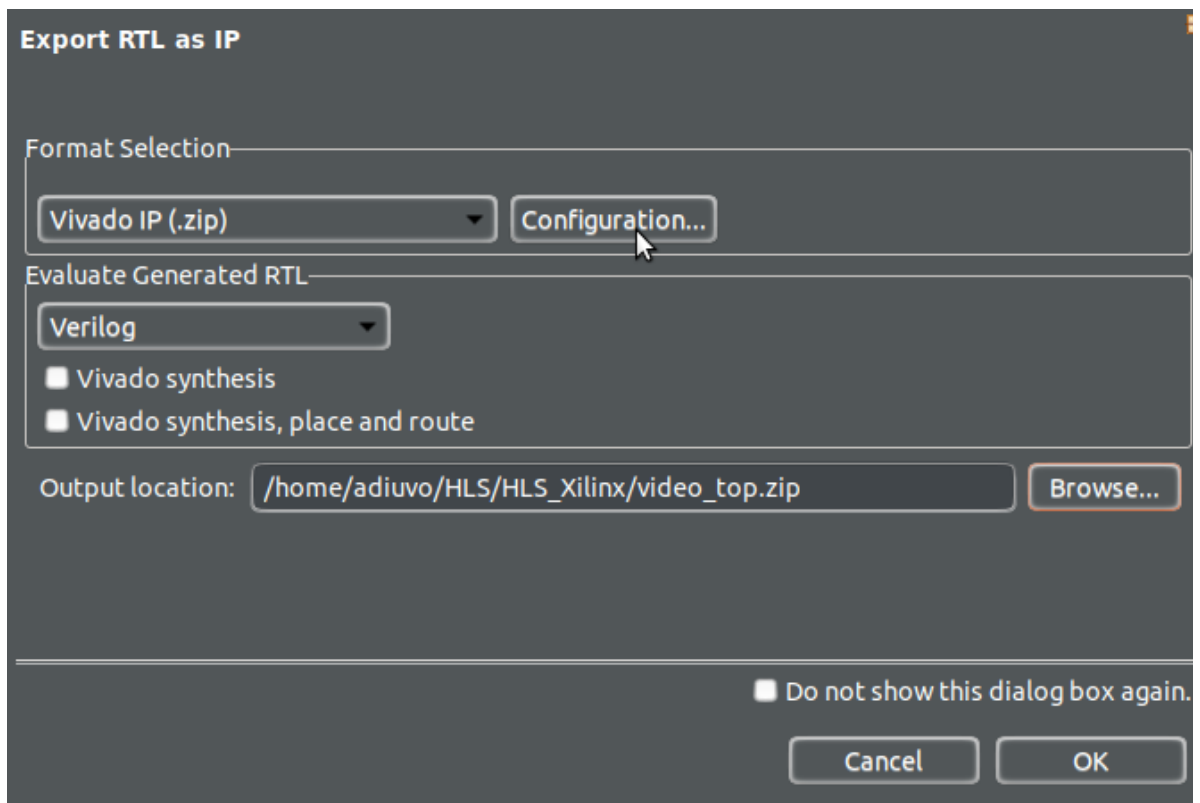
10. Enter the top function name, click browse and find video_top.



11. Run the HLS synthesis to generate the output RTL for export. You can run the synthesis by clicking the Run Synthesis button on the menu bar.



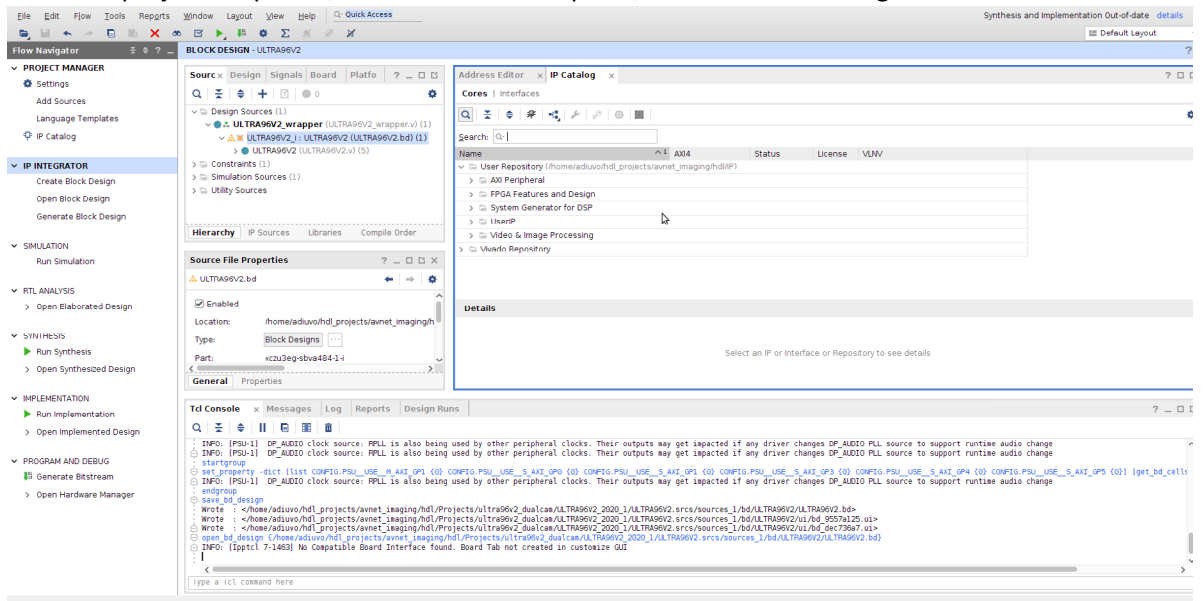
12. With the synthesized RTL available, we are now ready to export the IP module for use in Vivado. Click on the export IP button on the menu bar. Select an output location and click OK.



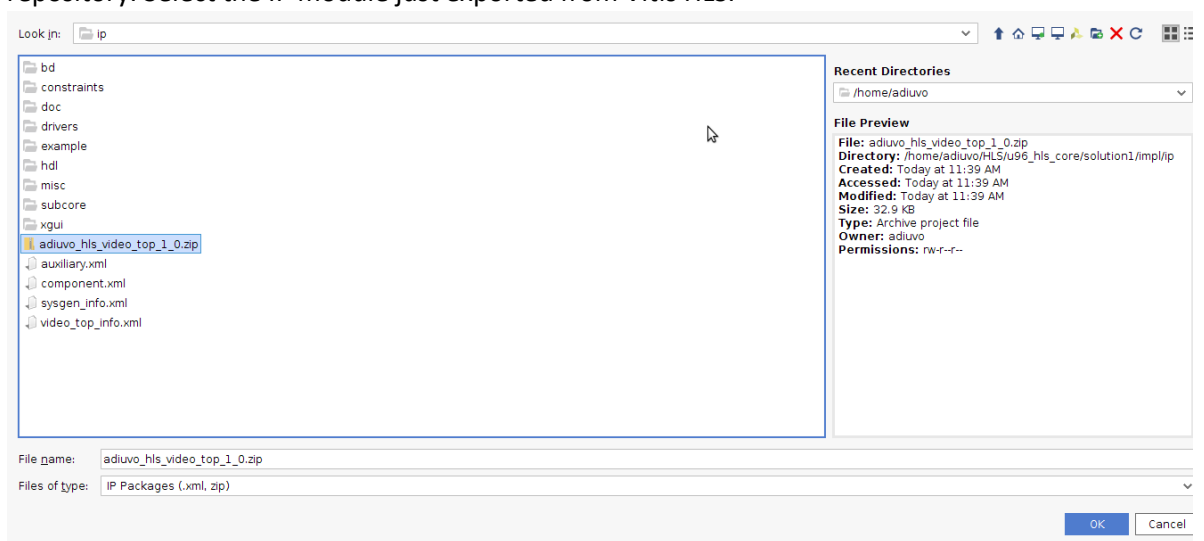
13. Close Vitis HLS.

Updating the Vivado Design

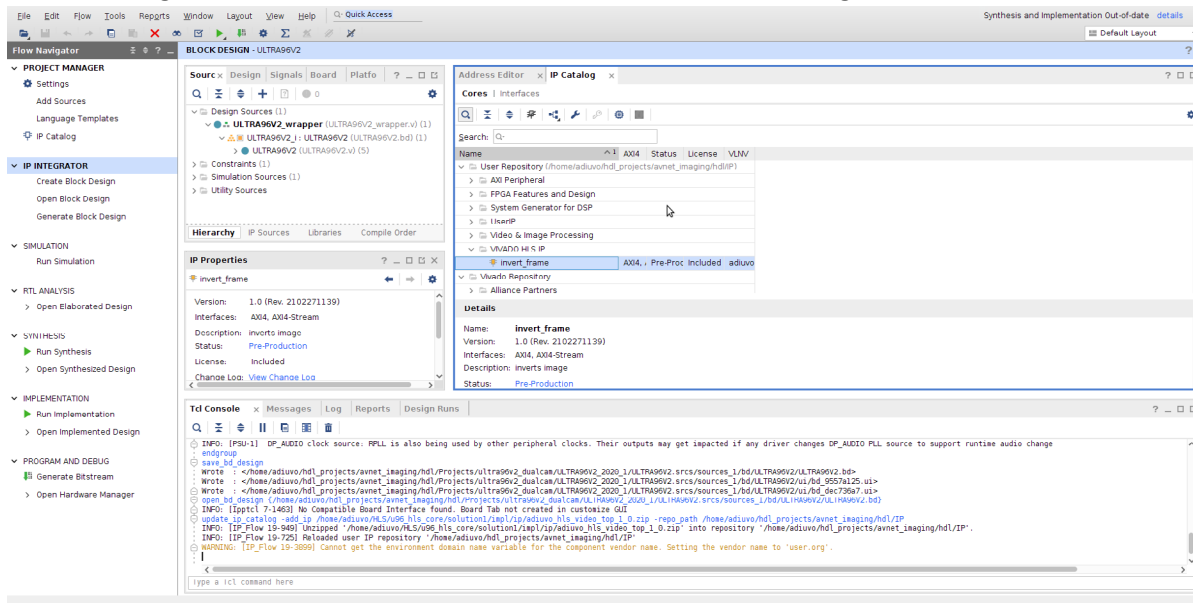
1. Open Vivado and the Ultra96V2 Camera project.
2. Once the project is opened, from the window option, select the IP Catalog.



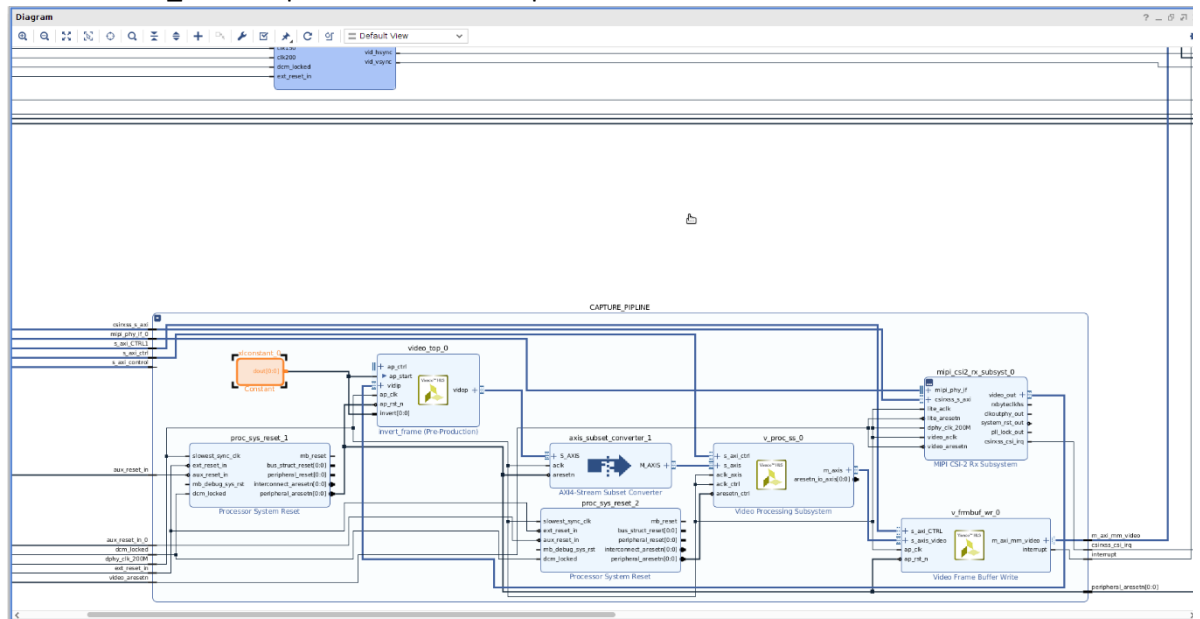
3. Select the user Repository, right click and select from the menu that appears. Add IP to the repository. Select the IP module just exported from Vitis HLS.



- You should now be able to see the HLS module available under the Vivado HLS IP directory in the IP Catalog. Double click on the IP core and select add to block design.



- On the block design, you will notice the new IP block has been added. Insert the block between the MIPI output and the AXI Subset converter. Add in a constant block and connect this to the AP_START input and the Invert Input.



- Rerun the bitstream generation of the design by selecting the generate bitstream option from the menu bar. When the bit stream is completed, select export hardware design from the file menu.

7. Select a fixed platform type.



Export Hardware Platform

This wizard will guide you through the export of a hardware platform for use in the Vitis or Petalinux software tools.

To export a hardware platform, you will need to provide a name and location for the exported file and specify the platform properties.

Platform type

- Fixed
A platform supporting embedded software development only.
- Expandable
A platform supporting acceleration.



< Back

Next >

Finish

Cancel

8. Select Include Bitstream.

Output

Set the platform properties to inform downstream tools of the intended use of the target platform's hardware design.



- Pre-synthesis
This platform includes a hardware specification for downstream software tools.
- Include bitstream
This platform includes the complete hardware implementation and bitstream, in addition to the hardware specification for software tools.



< Back

Next >

Finish

Cancel

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Finish

Cancel

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