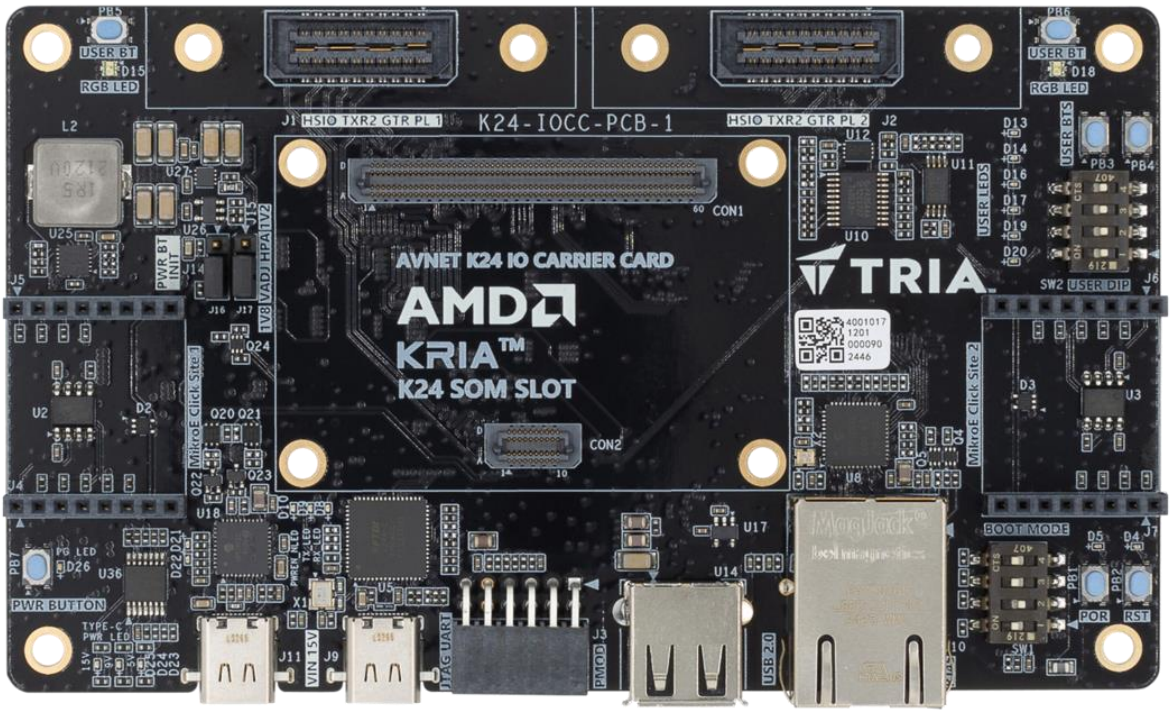
K24KIT

TRIA™



K24 Development Kit
Hardware User Guide

Version 1.2

LIT# K24-IO-DK-UG-V1P2

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1 Document Control

Document Version: 1.2

Document Date: 5 February 2025

2 Version History

Version	Date	Comment
1.0	09/11/2024	Initial Release
1.1	01/16/2025	Production Photos
1.2	02/05/2025	Update Website Links

3 Introduction

The K24 Development Kit is a solution that incorporates the AMD Kria™ K24 SOM based on Zynq UltraScale+ MPSoC and a carrier board targeted for broad use in many applications:

- Offering an AMD based Development Kit in Commercial (0ºC to 70ºC) temperature grade for engineers to adopt in development, proof-of-concept, and production projects.
- Combine programmable logic designs with quad-core ARM® Cortex®-A53 MPCore™ and dual-core Arm Cortex-R5F MPCore in a convenient and expandable board.
- Allow expansion to a variety of sensors and peripherals through the Mikroe Click Board and HSIO (High-Speed IO) expansion connectors.
- Target many applications for development, including:
    - Machine Vision
    - Factory Automation
    - Industrial IoT and Smart Sensors
    - Smart Home Appliances
    - Prototyping and Experimentation

3.1 Reference Documents

[1] **Kria K24 SOM Data Sheet – DS985**

[2] **UltraScale Architecture and Product Datasheet: Overview DS890**

[3] **Zynq UltraScale+ DC and AC Switching Characteristics DS925**

[4] **UltraScale+ Device Packaging and Pinout Product Specification UG575**

[5] **UltraScale Architecture PCB Design Guide UG583**

[6] **UltraScale Architecture SelectIO Resources UG571**

[7] **UltraScale Architecture Configuration User Guide (UG570)**

[8] **Xilinx Vivado Design Suite**

[9] **Xilinx Vitis Unified Software Platform**

[10] **Mikroe Click Boards Standards Specifications**

[11] **Vivado Design Suite User Guide: System-Level Design Entry (UG895)**

[12] **Kria K24 SOM Thermal Design Guide (UG1094)**

4 Architecture and Features

The K24 Development Kit provides a hardware environment for developing designs targeting the AMD Kria K24 SOM focusing on Zynq UltraScale+ devices. The K24 Development Kit provides features common to many systems including LPDDR4 memory, 10/100/1000 Ethernet PHY, USB2.0, multiple expansion interfaces, and UART interfaces. The details for the K24 Development Kit features are described in Functional Description sections that follow.

4.1 List of Features

The K24 Development Kit supports the following features:

- AMD Kria K24 SOM - Zynq UltraScale+ MPSoC **XCK24-UBVA530-2LV-C**
  - Custom-built Zynq UltraScale+ MPSoC exclusive for the SOM)
- AMD Kria K24 SOM - Memory/Storage
  - 2 GB LPDDR4 Memory
  - 64 MB QSPI Memory
  - 64 Kb EEPROM Memory
- AMD Kria K24 SOM - TPM2.0 Security Module
- K24 IO Carrier Card - 10/100/1000 Ethernet Interface
  - Microchip 10/100/1000 Ethernet Transceiver
    - Part Number: **KSZ9131RNXI**
- K24 IO Carrier Card – USB2.0 Type-A Interface
  - Microchip USB2.0 Transceiver
    - Part Number: **USB3321C-GL**
- K24 IO Carrier Card – microSD Card Connector
  - Bi-Direction Level Shifter for SD3.0-SDR104
    - Diodes Inc Part Number: **PI4ULS3V4857GEAEX**
- K24 IO Carrier Card - HSIO (HSIO) Expansion Sites
  - Mixed Programmable Logic I/O and Processor Based Gigabit Transceivers
    - Samtec Connector Part Number: **QSH-020-01-F-D-DP-A-K**
- K24 IO Carrier Card - MikroE Click Board™ Expansion Sites
    - Samtec Connector Part Number: **SSW-108-01-F-S**
- K24 IO Carrier Card - Digilent Pmod™ Click Expansion Sites
    - Samtec Connector Part Number: **SSW-106-02-T-D**
- K24 IO Carrier Card - I2C Bus Interface
  - I2C MAC ID / EEPROM Part Number: **AT24MAC402-XHM-B**
  - I2C Expander Part Number: **PCA9544APW,118**
- K24 IO Carrier Card - User RGB LEDs, RED LEDs, Push Buttons, and Switches
- K24 IO Carrier Card - USB Type-C JTAG and USB-to-UART Debug Interface
- K24 IO Carrier Card - USB Type-C Input Power Connector
  - USB Type-C Power Delivery Controller
    - Microchip Custom Programmed Part Number: **AVT~UPD301C/KYX~471416~PM**
- K24 IO Carrier Card - Power On/Off Controller and Power Sequencer
  - Renesas GreenPak™ Custom Power On/Off Controller
    - Part Number: **SLG7AV45289V**
  - Renesas GreenPak™ Custom Power Sequencer
    - Part Number: **SLG7TD43741V**
- K24 IO Carrier Card - Voltage Regulators
  - Renesas Multi-topology and Buck Regulator / Converter
    - Part Number: **ISL85014FRZ**
  - TDK Buck Regulator / Converter
    - Part Number: **FS1406-0600-AS**

        - Part Number: **FS1404-3300-AS**
    - OnSemi ecoSwitch™ - Load Switch with Integrated FET
        - Part Number: **NCP45524IMNTWG**

4.2 Block Diagram

The following figure is a high-level block diagram of the K24 Development Kit and the peripherals attached to the AMD Kria K24 SOM.

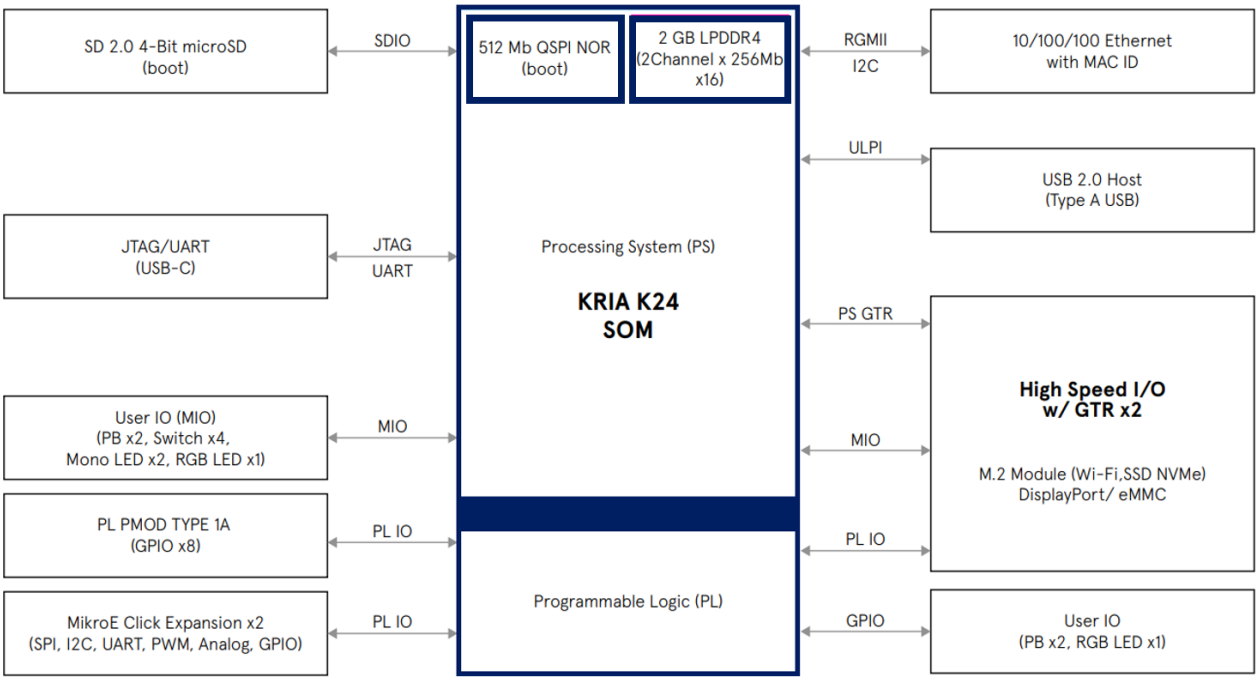


Figure 1 – Development Kit Block Diagram

4.3 What's In The Box

The K24 Development Kit includes a K24 SOM and K24 IO Carrier Card. The kit is meant for SOM platform evaluation with the carrier card providing a variety of standard interfaces and expansion connectors allowing for the integration of many of-the-shelf solutions of different peripherals. The K24 Development Kit includes the following in the box:

- K24 System-On-Module (no eMMC)
- K24 IO Carrier Card
- Quick Start Card

Customers need to acquire an appropriate Type-C power supply, Type-C cables, Ethernet cable, and microSD card. Customer will also need to procure or produce appropriate modules that target the various expansion interfaces. Here are links to companies that provide such products:

- Type-C AC/DC Power Supply 15V/3A (45W): **Advantech PSA-A45WM-U Power Supply**
- Avnet HSIO: **Avnet Add-On Products - High Speed IO Modules**
- MikroE Click: **https://www.mikroe.com/click**
- Opal Kelly SYZYGY: **https://docs.opalkelly.com/syzygy-peripherals/**

5 Functional Description

The following sections provide brief descriptions of each feature provided on the K24 Development Kit.

5.1 Interfaces and Connectors

The following figure provides an overview of the physical connections, their designators, and relative position on the K24 Development Kit. The image of the K24 IO Carrier Card is of a prototype, but the designators and the locations of the major components remains the same.

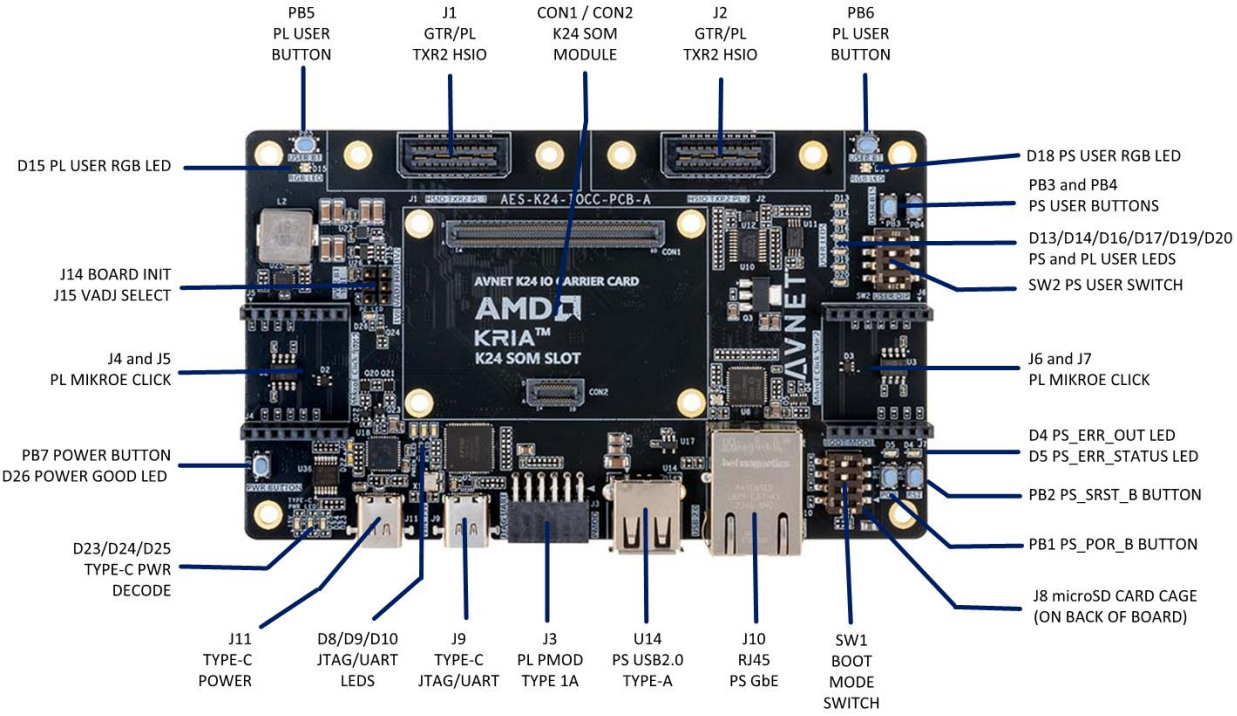


Figure 2 – Interfaces and Connectors

5.2 Powering the K24 Development Kit

The K24 Development Kit requires a 15V / 3A Type-C power supply to power the kit. The power supply and Type-C cable is not included in the kit. The power supply Type-C connector plugs into the Type-C power receptacle (J11) to supply the +15V power source to K24 Development Kit.

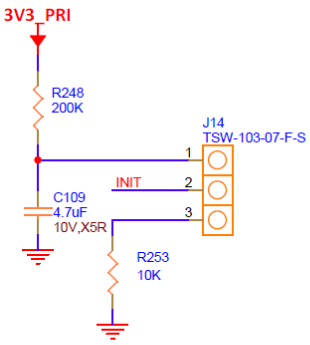
NOTE: If a 15V Type-C power supply is supplied to the Type-C power receptacle (J11), LED D25 will illuminate. If LED D23 or LED D24 illuminate, the Type-C power supply is not providing 15V and the board will not power up.

To power up the K24 Development Kit a user must push the **PB7** Power Button to turn power on to the board (depending on the state of the BOARD INIT header **J14**).

To power down the K24 Development Kit a user must HOLD the **PB7** Power Button to turn power off to the board (depending on the state of the BOARD INIT header **J14**) until the board powers down.

- When **J14** is shunted pin 2 to pin 3, the board powers up and down with the **PB7** Power Button being exercised.

- When **J14** is shunted pin 2 to pin 1, the board powers up when power is applied to the Type-C power receptacle, **J11**, and the board powers down when power is removed from the Type-C power receptable, **J11**.



J14	Result
PIN 1/2	Board powers up when power applied
PIN 2/3	User must press Power On button (Default)

Figure 3 – Board INIT Header J14

The K24 Development Kit provides the power supply rails and control necessary to ensure the appropriate power sequencing, device power budgets, and interface power budgets are met. The following is a brief description of the power supply sequence.

- The K24 IO Carrier Card power is enabled depending on the position of header **J14**.
- The K24 IO Carrier Card has an on-board regulator that generates a 5V supply and provides power to other voltage regulators and the K24 SOM.
- The SOM power rail (VCC_SOM) is powered by the 5V supply.
- The SOM on-board power-on sequencing starts.
- The K24 IO Carrier Card completes the sequence by providing the programmable logic (PL) the VCCO voltage rails after the SOM asserts the VCCOEN_PL_M2C signal.
- Power good indicator LED **D26** will illuminate indicated power up success.

The K24 IO Carrier Card supplies power to the I/O peripherals as specified by the following interface specifications.

- **USB2.0** – The USB2.0 interface port can deliver a 5V supply to the attached I/O peripherals with up to 500mA. The port is protected against an over-current event through a current-limiting high-side power-switch.
- **Pmod Connector** – The 12-pin Pmod interface (Digilent, Inc.) is specified to be 3.3V / 100ma. The interface is support by the 3.3V VCCO_HDA power-switch.
- **microSD Card** – The microSD card is support by the 3.3V supply voltage. The supply to this interface is not limited.

- **High-Speed I/O (HSIO) Interface** – There are two HSIO interfaces on the K24 IO Carrier Card. Each interface supplies 3.3V VCCO_HDA from the supported power-switch and 1.8V or 1.2V VCCO_HPA from its power-switch. The VCCO_HPA voltage is passed from the creation of the VADJ_HPA voltage. The VADJ_HPA voltage is selected by shunting header J15 appropriately. 1.8V for VADJ_HPA is generated from an on-board 1.8V regulator and 1.2V for VADJ_HPA is generated from an on-board 1.2V regulator.

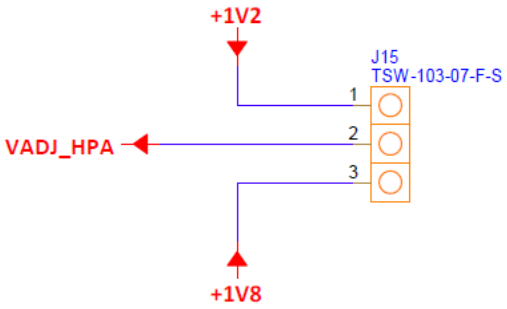


Figure 4 – VADJ_HPA Voltage Select J15

- **MikroE Click Interfaces** – There are two MikroE Click interface on the K24 IO Carrier Card. Each interface supplies 5V and 3.3V according to the Click specifications. The supplies to these interfaces are delivered by the 5V VCC_SOM power supply and the 3.3V VCCO_HDA power supply.

5.2.1 Power-On and Processor Subsystem Resets

The Zynq UltraScale+ MPSoC processing system supports an external power-on reset signal, **PS_POR_B**. The power-on reset signal is the master reset of the Zynq UltraScale+ MPSoC device. The power-on resets signal resets every register in the device capable of being reset. On the K24 IO Carrier Card this reset signal is labelled **PS_POR_N** and it is connected to a push button, **PB1**.

To stall the Zynq UltraScale+ MPSoC boot-up, this reset signal should be held low. Pressing **PB1** will cause the **POWER_GOOD** LED **D26** to turn-off.

The power-on reset signal **PS_POR_B** resets several interfaces on the K24 IO Carrier Card. The GbE Ethernet interface, USB2.0 interface, and the JTAG interface are reset upon **PS_POR_B** being pulled low.

The Zynq UltraScale+ MPSoC processing system also supports a soft reset signal, **PS_SRST_B**. This signal being asserted low resets the processor as well as erases all debug configurations. On the K24 IO Carrier Card this reset signal is labelled **PS_SRST_N** and it is connected to a push button, **PB2**.

The reset signal **PS_SRST_B** is provided to the JTAG interface like the **PS_POR_B** power-on reset signal.

NOTE: The **PS_SRST_B** signal cannot be asserted while the boot ROM is executing following a power-on reset (**PS_POR_B**). If **PS_SRST_B** is asserted while the boot ROM is running through a power-[on reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or **PS_POR_B** needs to be asserted.

5.2.2 Status LEDs

There are several status LEDs on the K24 Development Kit. Some of these LEDs reside on the Kria K24 SOM such as a green PS DONE LED indicator - DS34, a heartbeat LED – DS35, and a PS Status LED

DS36. On the K24 IO Carrier Card, two additional status LEDs are implemented. LED **D4** is connected to status signal **PS_ERROR_OUT** and LED **D5** is connected to status signal **PS_ERROR_STATUS**.

PS_ERROR_OUT is asserted when there is an accidental loss of power, a hardware error, or an exception in the PMU. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask **PS_ERROR_OUT**. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* (**UG1085**).

PS_ERROR_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status. For secure scenarios where device status is disabled from external visibility, there are PMU control registers to mask **PS_ERROR_STATUS**. For more information, see the *Zynq UltraScale+ Device Technical Reference Manual* (**UG1085**).

5.2.3 Battery Backup Circuit

The Zynq UltraScale+ MPSoC implements bitstream encryption key technology. The K24 Development Kit provides the encryption key backup battery circuit. The rechargeable 1.5V lithium button-type battery, BAT1, is to be soldered to the board with the positive output connected to the VCCBATT pin A1 on the SOM Connector CON1. BAT1 is charged from the **+1V8** +1.8V rail through a series diode and a 4.7 kΩ current limit resistor.

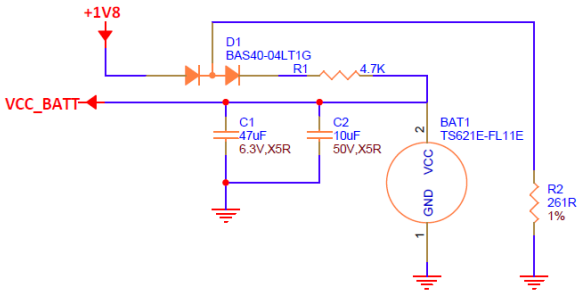


Figure 5 – Battery Backup Circuit

NOTE: The 1.5V lithium button-type battery, BAT1, is not installed and if this function is desired the proper battery must be procured and installed by the end user. The 1.5V lithium button-type battery is a Seiko Instruments TS621E-FL11E.

5.3 Kria K24 System-On-Module

K24 Development Kit features a Kria K24 SOM that leverages the Zynq UltraScale+ MPSoC **XCK24-UBVA530-2LV-C** device (-2 Speed Grade, UBVA530 Package, -C Commercial Temperature Grade, and -LV Low Voltage).

The Kria K24 SOM contains the following features:

- 2GB 32-bit wide 1066Mb/s LPDDR4 memory
- 512 Mb QSPI
- 64 Kb EEPROM
- TPM2.0 Security Module
- 240-pin Connector and 40-pin Connector with the following:
  - PS-MIO
  - PS-GTR Transceivers
  - PS-I2C Platform Control Bus
  - PL-HPIO

- PL-HDIO
- Sideband Platform Signals
- Power and Power Sequencing Signals

The Kria K24 SOM provided with the K24 Development Kit does not include the following component:

- 32 GB eMMC

For more details regarding the Kria K24 SOM, please refer to the **Kria K24 SOM Datasheet, DS985**.

5.3.1 Vivado Board Definition File

The Kria K24 SOM is enabled in the Vivado Design Suite through the Vivado Board Flow functionality. Vivado Board Flow enables a level of hardware abstraction that automatically configures peripherals fixed on the SOM card (e.g., LPDDR4), defines associated timing constraints, and presents the customizable physical I/O available on the SOM connector(s). It is expected that this Vivado board file will be utilized as the starting point for any design targeting the K24 Development Kit.

The Vivado SOM board model is available through the Vivado installation process as well as on the Vivado board file GitHub repository. The following Kria K24 SOM Vivado board files is available:

- SM-K24-XCL2GC: K24 commercial grade production SOM containing eMMC

NOTE: The eMMC is not populated on the K24 SOM contained in the K24 Development Kit. Therefore, a user may modify their Vivado Block Design to omit this interface as it is unavailable for use.

For additional information on using the Vivado tools and the Vivado board flow, refer to the Vivado Design Suite User Guide: System-Level Design Entry (UG895).

5.4 Boot Source and Storage Devices

The Kria K24 SOM includes a non-volatile storage boot device in the form of QSPI flash memory. The K24 IO Carrier Card provides a secondary boot device via a SD card interface on the carrier card.

The Kria K24 SOM included with the K24 Development Kit does not include a secondary non-volatile storage. Normally a Kria K24 SOM provides an eMMC device, but the Kria K24 SOM provided with the K24 Development Kit does not have the eMMC flash memory populated. A user must rely on the microSD card on the carrier card as the secondary boot device.

The K24 Development Kit supports the following boot modes:

- Master SPI flash memory using the onboard Quad SPI flash memory.
- microSD card memory using the carrier card microSD card cage.
- JTAG using a Type-C USB cable for connecting the host PC to the K24 Development Kit configuration port J9.

The configuration interface corresponds to one or more boot modes and bus widths as listed in Table 1. The default mode setting is **M[3:0] = 0010**, which selects Master SPI flash memory at board power-on.

BOOT Mode	M[3:0]	SW1
Master SPI Flash Memory	0010	ON-ON-OFF-ON
microSD Card Memory	0101	ON-OFF-ON-OFF
JTAG	0000	ON-ON-ON-ON

Table 1 – MPSoC Boot Modes

The K24 Development kit allows the MPSoC Boot Mode to be selected by setting the Boot Mode Switch, SW1 to the appropriate values depicted in Table 1. The Boot Mode Switch, SW1, is placed on the bottom right hand corner of the K24 Development Kit. The proper MPSoC Boot Mode should be set prior to board power-on for proper operation. Figure 1 shows the MPSoC Boot Mode Switch, SW1.

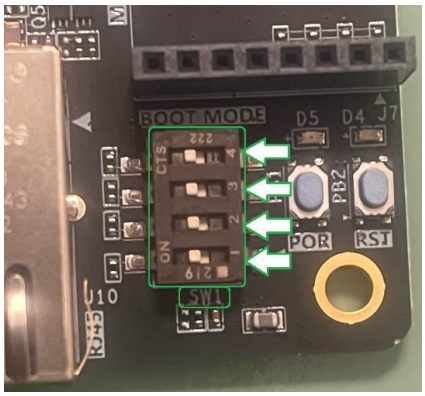


Figure 6 – MPSoC Boot Mode Switch SW1

The primary boot device is the QSPI device located on the Kria K24 SOM. The necessary elements are packaged in an AMD Zynq™ UltraScale+™ MPSoC specific format and the file is captured as *BOOT.BIN*. The *BOOT.BIN* file contains board-specific boot firmware that consists of the following elements:

- FSBL: First-Stage Boot-Loader Firmware
- PMU: Platform Management Unit Firmware
- ATF: ARM® Trusted Firmware
- U-BOOT: Second-Stage Boot Loader

U-Boot provide the functionality for hand-odd between the primary boot device and the secondary boot device. It searches through a U-Boot defined prioritized list of secondary boot devices with the priority give to the SD card interface.

The secondary boot device on the K24 Development Kit is the microSD card. It typically contains the operating system image and associated application files.

NOTE: Avnet has available an HSIO Add-On card meant for use on the HSIO expansion connectors which provides access to an eMMC via PLIO. As of the writing of the K24 Development Kit User Guide, the HSIO Add-On eMMC storage has not been tested to see if eMMC via PLIO is a supported secondary boot mode option.

5.4.1 SOM QSPI Interface

The Kria K24 SOM includes a 512 Mb (64MB) QSPI flash memory device. It supports interface clocks speeds up to 40 MHZ and can be used as the primary boot device for the MPSoC processing subsystem. The QSPI device is left blank during manufacturing of the Kria K24 SOM.

The Quad-SPI Flash connects to the Zynq UltraScale+ MPSoC PS QSPI interface. This requires connection to specific pins in MIO Bank 500, specifically MIO[0:5] as outlined in the Zynq UltraScale+ TRM (Technical Reference Manual, UG1085).

MIO BANK 500	MIO PIN NAME	MPSoC Package Pin
MIO0	QSPI_CLK	G18
MIO1	QSPI_DQ1	K21
MIO2	QSPI_DQ2	F18
MIO3	QSPI_DQ3	H17
MIO4	QSPI_SQ0	L20
MIO5	QSPI_CS_B	H22

Table 2 – QSPI Interface Pin Map

5.4.2 microSD Card Interface

The K24 Development Kit provides a microSD card interface for use as a boot device and / or for user storage. The Kria K24 SOM exposes PS MIO[45-51] on the 240-pin connector, CON1 and these PS MIO pins are used to interface to the microSD card connector that operates at 3.3V. The PS MIO bank on the Kria K24 SOM has its voltage set to 1.8V. The K24 IO Carrier Card implements a Diodes, Inc. 6-Bit Bi-directional Level Shifter for SD card applications so that it can translate the signals between the 1.8V and 3.3V voltages.

- Manufacturer: Diodes, Inc
- Part Number: PI4ULS3V4857GEAX

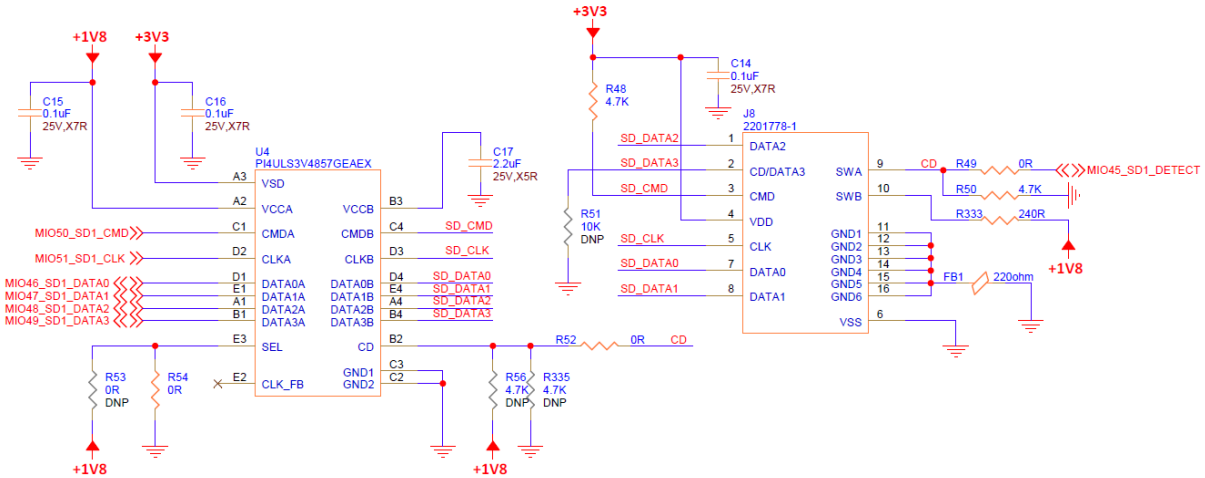


Figure 7 – microSD Card Interface

Carrier Card Net Name	J8 Signal Name	CON1 Pin Name (Number)	MPSoC Package Pin
MIO45_SD1_DETECT	CD	MIO45 (D33)	N10
MIO46_SD1_DATA0	SD_DATA0	MIO46 (D34)	N14
MIO47_SD1_DATA1	SD_DATA1	MIO47 (C34)	N13
MIO48_SD1_DATA2	SD_DATA2	MIO48 (C35)	N12
MIO49_SD1_DATA3	SD_DATA3	MIO49 (C36)	M14
MIO50_SD1_CMD	SD_CMD	MIO50 (B36)	J10
MIO51_SD1_CLK	SD_CLK	MIO51 (B37)	K10

Table 3 – microSD Card Interface Pin Map

5.4.3 JTAG Interface

JTAG configuration is provided through an onboard USB-to-JTAG configuration device (U5), in which a host computer accesses the K24 Development Kit JTAG chain through a type-A or type-C (host side) to type-C (K24 Development Kit side J9) USB cable. The USB-to-JTAG configuration device can be used for PL configuration, QSPI flash programming, as well as PS software debugging.

This USB-to-JTAG bridge device is shared with the device that also provides the USB-to-UART interface functionality.

The JTAG interface is translated from 3.3V to 1.8V for use by the Kria K24 SOM. The Kria K24 SOM has access to the JTAG interface via the 240-pin connector, CON1.

LED indicator D10 will illuminate when a USB Type-C cable is properly attached between a host device and the J9 port on the K24 IO Carrier Card is active.

Carrier Card Net Name	CON1 Pin Name (Number)	MPSoC Package Pin
JTAG_TCK	JTAG_TMS_C2M (A25)	E22
JTAG_TDI	JTAG_TDI_C2M (A24)	F23
JTAG_TDO	JTAG_TDO_M2C (A23)	B22
JTAG_TMS	JTAG_TMS_C2M (A22)	A23

Table 4 – JTAG Interface Pin Map

5.5 UART Interface

UART communication interface is provided through an onboard USB-to-UART configuration device (U5), in which a host computer accesses the K24 Development Kit UART interface through a type-A or type-C (host side) to type-C (K24 Development Kit side J9) USB cable. This USB-to-UART bridge device is shared with the device that also provides the USB-to-JTAG interface functionality.

NOTE: Device U5 is not powered by the USB 5V provided by the host PC USB cable. It is powered by an on-board +3V3 power rail.

Note: The VCP (Virtual COM Port) device drivers must be installed on the host PC prior to establishing communications with the K24 Development Kit.

The UART interface is translated from 3.3V to 1.8V for use by the Kria K24 SOM. The Kria K24 SOM has access to the UART interface via the 240-pin connector, CON1.

LED indicators D8 and D9 will toggle on and off with activity on the UART RX signal and / or the UART TX signal.

Carrier Card Net Name	Function	Direction	CON1 Pin Name (Number)	MPSoC Package Pin	U5 Pin Number	U5 Function
MIO36_UART1_TX	Transmit	Data Output	MIO36 (B29)	M12	39	Data Input
MIO37_UART1_RX	Receive	Data Input	MIO37 (B30)	M9	38	Data Output

Table 5 – UART Interface Pin Map

5.6 Ethernet Interface

The K24 IO Carrier Card uses a Microchip PHY device (KSZ9131) at U8 for Ethernet communications up to 1 Gb/s. The PHY connection to the user-provided ethernet cable is through a Bel Fuse L829-1J1T-43 RJ-45 connector (J10) with built-in magnetics.

- Manufacturer: Microchip
- Part Number: KSZ9131RNXI-TR
- 1 Gb/s Ethernet PHY

- Manufacturer: Bel Fuse
- Part Number: L829-1J1T-43
- 1 Gb/s RJ-45 Connector

On power-up, or on reset, the PHY is configured to operate in RGMII mode with PHY address 0b00111 using the settings shown in Table 6. These settings can be overwritten by commands passed over the MDIO interface.

U25 Pin Name / No	Setting	Configuration	
RXC/PHYAD2 (35)	+1V8	PHYAD[2] = 1	PHY ADDRESS = 0x07
LED2/PHYAD1 (15)	+1V8	PHYAD[1] = 1	
LED1/PME_N1/PHYAD0 (17)	+1V8	PHYAD[0] = 1	
RXD3/MODE3 (27)	+1V8	MODE[3] = 1	MODE = 0x0E
RXD2/MODE2 (28)	+1V8	MODE[2] = 1	RGMII MODE
RXD1/MODE1 (31)	+1V8	MODE[1] = 1	1000BT FULL DUPLEX
RXD0/MODE0 (32)	GND	MODE[0] = 0	
CLK125/NDO/LED_MODE (41)	GND	LED_MODE = 0	TRI-COLOR LED MODE
RX_CTL/CLK125_EN	GND	CLK125_EN = 0	DISABLE CLOCK OUTPUT

Table 6 – Ethernet PHY U8 Configuration Pin Settings

The Ethernet connections from the Kria K24 SOM to the KSZ9131 device at U8 are listed in Table 7.

MPSoC Pin (SOM)	CON1 Pin Name (Number)	Schematic Net Name	KSZ9131 (U8) Pin Name (No)
F16	MIO52 (D36)	MIO52_RGMII_TX_CLK	TXC (24)
G15	MIO53 (D37)	MIO53_RGMII_TXD0	TXD0 (19)
E16	MIO54 (D38)	MIO54_RGMII_TXD1	TXD1 (20)
D14	MIO55 (C38)	MIO55_RGMII_TXD2	TXD2 (21)
F15	MIO56 (C39)	MIO56_RGMII_TXD3	TXD3 (22)
C19	MIO57 (C40)	MIO57_RGMII_TX_CTL	TX_CTL (25)
D18	MIO58 (B40)	MIO58_RGMII_RX_CLK	RXC/PHYAD2 (35)
C18	MIO59 (B41)	MIO59_RGMII_RXD0	RXD0/MODE0 (32)
C15	MIO60 (B42)	MIO60_RGMII_RXD1	RXD1/MODE1 (31)
C16	MIO61 (A38)	MIO61_RGMII_RXD2	RXD2/MODE2 (28)
B16	MIO62 (A39)	MIO62_RGMII_RXD3	RXD3/MODE3 (27)
D15	MIO63 (A40)	MIO63_RGMII_RX_CTL	RX_CTL/CLK125_EN (33)
A20	MIO76 (D44)	MIO76_GEM2_MDC	MDC (36)
A19	MIO77 (D45)	MIO77_GEM2_MDIO	MDIO (37)

Table 7 – Ethernet RGMII Connections to U8

5.6.1 Ethernet PHY Clock Source

A 25MHz, 50ppm CMOS oscillator at X2 is the clock source for the KSZ9131 PHY at U8. Figure 8 shows the clock source.

- Manufacturer: ECS
- Part Number: ECS-2016MV-250-BN-TR
- 25MHz XO CMOS Oscillator

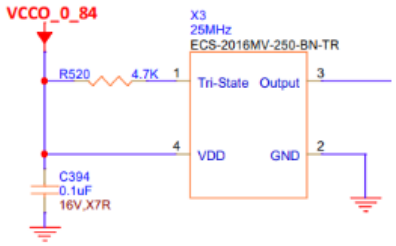


Figure 8 – Ethernet PHY Clock Source

5.6.2 Ethernet PHY LEDs

There are two LED drivers, LED0 and LED1, from the Ethernet PHY that connects to the RJ45 Ethernet Jack (J10). The Microchip KSZ9131 data sheet contains details concerning the potential functions mapped to the LED0 and LED1 pin. For LED0, a LINK function is mapped to this pin. For LED1, an ACTIVITY function is mapped to this pin.

5.7 USB2.0 Interface

The K24 IO Carrier Card uses a Microchip PHY device (USB3321C) at U13 for the USB2.0 interface. The PHY connection to the user-provided USB devices is through a Samtec USB-A-S-F-B-TH USB2.0 Type-A connector (U14).

- Manufacturer: Microchip
- Part Number: USB3321C-GL-TR
- USB2.0 ULPI PHY

- Manufacturer: Samtec
- Part Number: USB-A-S-F-B-TH
- USB2.0 Type-A Connector

The USB ULPI connections from the Kria K24 SOM to the USB3321C device at U13 are listed in Table 8.

MPSoC Pin (SOM)	CON1 Pin Name (Number)	Schematic Net Name	USB3321 (U13) Pin Name (No)
B15	MIO64 (D40)	MIO64_USB1_CLK	CLKOUT (A5)
B13	MIO65 (D41)	MIO65_USB1_DIR	DIR (A4)
B12	MIO66 (D42)	MIO66_USB1_DATA2	DATA2 (C4)
A12	MIO67 (C42)	MIO67_USB1_NXT	NXT (B5)
A13	MIO68 (C43)	MIO68_USB1_DATA0	DATA0 (B4)
A14	MIO69 (C44)	MIO69_USB1_DATA1	DATA1 (C5)
B19	MIO70 (B44)	MIO70_USB1_STP	STP (A3)
A15	MIO71 (B45)	MIO71_USB1_DATA3	DATA3 (D5)
B18	MIO72 (B46)	MIO72_USB1_DATA4	DATA4 (D4)
A17	MIO73 (A42)	MIO73_USB1_DATA5	DATA5 (E5)
A18	MIO74 (A43)	MIO74_USB1_DATA6	DATA6 (E4)
A16	MIO75 (A44)	MIO75_USB1_DATA4	DATA7 (D3)

Table 8 – USB ULPI Connections to U13

5.7.1 USB PHY Clock Source

A 26MHz, 50ppm MEMS CMOS oscillator at U16 is the clock source for the USB3321C PHY at U13. Figure 9 shows the clock source.

- Manufacturer: Microchip
- Part Number: DSC6101ME1B-026.000
- 26MHz MEMS CMOS Oscillator

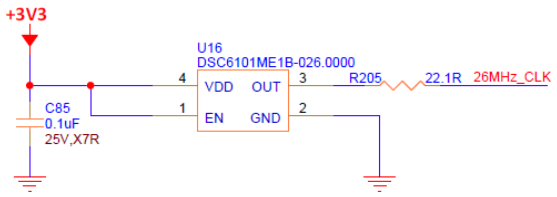


Figure 9 – USB PHY Clock Source

5.8 Click Expansion Interfaces

The K24 Development Kit contains two MikroE compatible Click sites. These Click sites allow for inexpensive Click Board expansion through the MikroE Click ecosystem. The Click sites are implemented with Samtec SSW-108-01-F-S connectors.

Visit **https://avnet.me/click** for a listing of some of the available Click boards.

Figure 10 is the implementation of the MikroE Click site interfaces. The analog pins, AN, has support provided by Microchip MCP3201T-CI/SN A/D converters. The I2C interfaces on the MikroE Click sites are accessed via the NXP PCA9544APW,118 device which is a 4CH I2C bus multiplexer. Please see the I2C Bus Switch section of this document for more details on using that device.

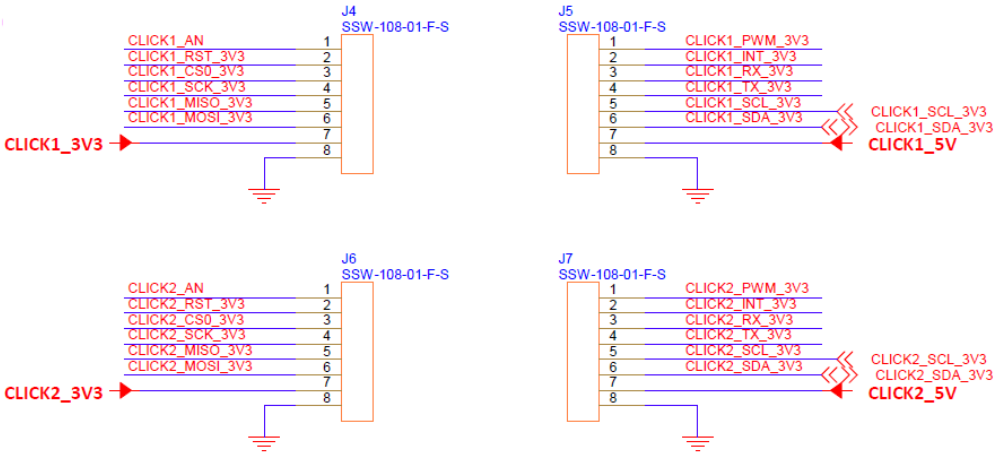


Figure 10 – MikroE Click Site Implementation

Table 9 shows the pinout of the first MikroE Click Expansion Header and the differences from the MikroE Click specification.

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	Click Interface (J4 / J5) Pin Name / No
G10	HDA04 (B17)	CLICK1_CS1	U2 / SPI IF
U2 / SPI IF	U2 / SPI IF	CLICK1_AN	AN / J4-1
F12	HDA09 (A15)	CLICK1_RST	RST / J4-2
H9	HDA03 (B16)	CLICK1_CS0	CS0 / J4-3
H10	HDA02 (D18)	CLICK1_SCK	SCK / J4-4
G13	HDA01 (D17)	CLICK1_MISO	MISO / J4-5
H13	HDA00_CC (D16)	CLICK1_MOSI	MOSI / J4-6
G9	HDA05 (B18)	CLICK1_PWM	PWM / J5-1
G12	HDA08_CC (C20)	CLICK1_INT	INT / J5-2
F10	HDA06 (C18)	CLICK1_RX	RX / J5-3
F9	HDA07 (C19)	CLICK1_TX	TX / J5-4
MIO24_I2C_SCK (K24)	U10 / 13 (Switch)	CLICK1_SCL	SCL / J5-5
MIO25_I2C_SDA (J18)	U10 / 12 (Switch)	CLICK1_SDA	SDA / J5-6

Table 9 – MikroE Click Site #1 Connections to SOM

Table 10 shows the pinout of the second MikroE Click Expansion Header and the differences from the MikroE Click specification.

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	Click Interface (J6 / J7) Pin Name / No
D9	HDA15 (B20)	CLICK2_CS1	U3 / SPI IF
U3 / SPI IF	U3 / SPI IF	CLICK2_AN	AN / J6-1
B9	HDA20 (C24)	CLICK2_RST	RST / J6-2
D10	HDA14 (D22)	CLICK2_CS0	CS0 / J6-3
E12	HDA13 (D21)	CLICK2_SCK	SCK / J6-4
F13	HDA12 (D20)	CLICK2_MISO	MISO / J6-5
E9	HDA11 (A17)	CLICK2_MOSI	MOSI / J6-6
D13	HDA16_CC (B21)	CLICK2_PWM	PWM / J7-1
B10	HDA19 (C23)	CLICK2_INT	INT / J7-2
C13	HAD17 (B22)	CLICK2_RX	RX / J7-3
C10	HDA18 (C22)	CLICK2_TX	TX / J7-4
MIO24_I2C_SCK (K24)	U10 / 16 (Switch)	CLICK2_SCL	SCL / J7-5
MIO25_I2C_SDA (J18)	U10 / 15 (Switch)	CLICK2_SDA	SDA / J7-6

Table 10 – MikroE Click Site #2 Connections to SOM

5.9 HSIO Expansion Interfaces

The K24 IO Carrier Card offers two Samtec connectors for HSIO (high-speed I/O) expansion interfaces. These two interfaces contain a mix of GTRs (processor based multi-gigabit transceivers) and HP (high performance) PL (programmable logic) I/Os. Samtec QSH-020-01-F-D-DP-A-K-TR connector is used to provide the two high-speed sites with GTR transceivers which is also known as a TXR2 PLIO expansion interface. Table 11 and 12 shows the pinout of the two HSIO expansion interface sites.

NOTE: The processor based multi-gigabit transceivers can be used to implement multi-lane Display Port interface up to 4Kx2K, multi-lane PCIe version 2.1, SATA 3.1 interfaces, USB3.0 interface at 5Gb/s line rates, and serial GMII interface supporting Gigabit Ethernet.

The I2C ports mapped to the HSIO expansion sites are delivered via the I2C bus switch, U10 at I2C address 0x71. Please review the I2C Bus Switch section of this document for more details on how the I2C pins from the HSIO expansion sites are mapped to the I2C bus switch device.

- Manufacturer: Samtec
- Part Number: QSH-020-01-F-D-DP-A-K-TR
- 0.50mm / 40-position differential array connector

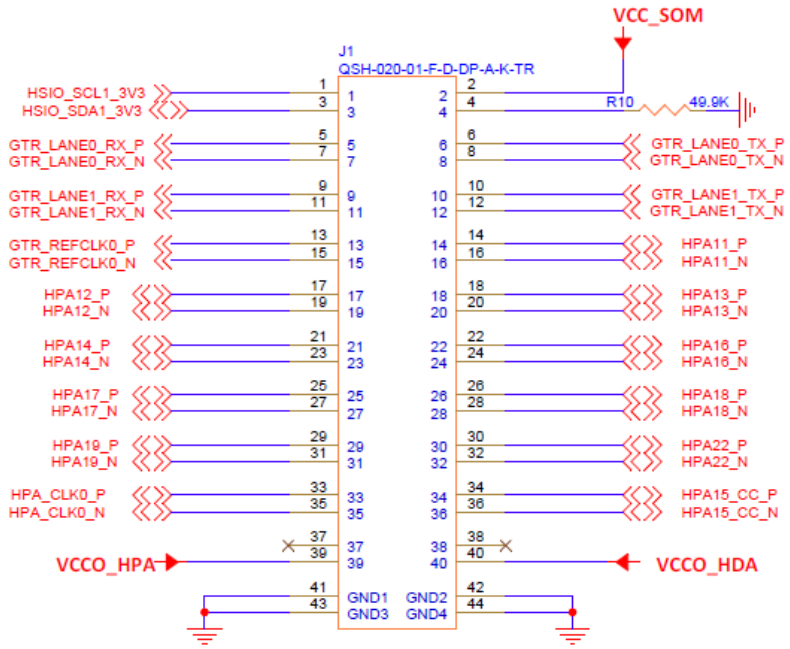


Figure 11 – HSIO Expansion Site #1 Implementation

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	HSIO Interface (J1) Pin Numbers
MIO24 / MIO25 (J18 / K24)	U10 6 /5 (Switch)	HSIO_SCL1 / HSIO_SDA1	1 / 3
K30 / K31	A55 / A56	GTR_LANE0_RX_P/N	5 / 7
G27 / G28	B57 / B58	GTR_LANE0_TX_P/N	6 / 8
H30 / H31	C55 / C56	GTR_LANE1_RX_P/N	9 / 11
E27 / E28	A47 / A48	GTR_LANE1_TX_P/N	10 / 12
N27 / N28	C47 / C48	GTR_REFCLK0_P/N	13 / 15
L2 / M1	B10 / B11	HPA11_P/N	14 / 16
H8 / J7	A09 /A10	HPA12_P/N	17 / 19
J1 / K1	A12 / A13	HPA13_P/N	18 / 20
G7 / H7	D13 / D14	HPA14_P/N	21 / 23
F7 / G6	A01 / A02	HPA16_P/N	22 / 24
E1 / F1	D02 / D03	HPA17_P/N	25 / 27
C1 / D1	B02 / B03	HPA18_P/N	26 / 28
D2 / E2	C04 / C05	HPA19_P/N	29 / 31
V6 / V5	B05 / B06	HPA22_P/N	30 / 32
P2 / P1	A06 / A07	HPA_CLK0_P/N	33 / 35
H2 / H1	C01 / C02	HPA15_CC_P/N	34 / 36

Table 11 – HSIO Expansion Site #1 Connections to SOM

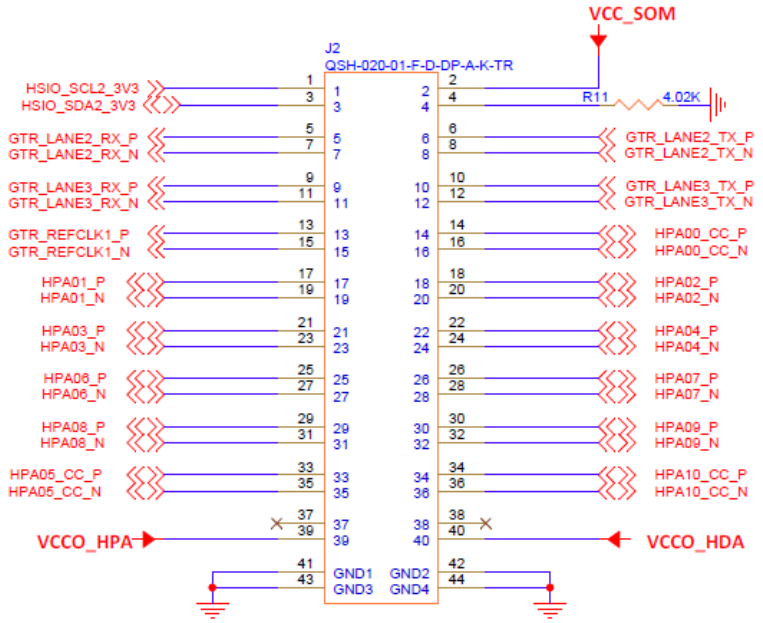


Figure 12 – HSIO Expansion Site #2 Implementation

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	HSIO Interface (J2) Pin Name / No
MIO24 / MIO25 (J18 / K24)	U10 9 / 8 (Switch)	HSIO_SCL2 / HSIO_SDA2	1 / 3
F30 / F31	B53 / B54	GTR_LANE2_RX_P/N	5 / 7
C27 / C28	D57 / D58	GTR_LANE2_TX_P/N	6 / 8
D30 / D31	D49 / D50	GTR_LANE3_RX_P/N	9 / 11
A27 / A28	C51 / C52	GTR_LANE3_TX_P/N	10 / 12
M30 / M31	B49 / B50	GTR_REFCLK1_P/N	13 / 15
N6 / P6	C03 / C04	HPA00_CC_P/N	14 / 16
N4 / P4	D07 / D08	HPA01_P/N	17 / 19
M7 / N7	D04 / D05	HPA02_P/N	18 / 20
T6 / U5	C06 / C07	HPA03_P/N	21 / 23
T4 / U4	B04 / B05	HPA04_P/N	22 / 24
V4 / V3	A03 / A04	HPA06_P/N	25 / 27
K7 / k6	B07 / B08	HPA07_P/N	26 / 28
R1 / T1	C09 / C10	HPA08_P/N	29 / 31
N2 / N1	D10 / D11	HPA09_P/N	30 / 32
T2 / U2	B01 / B02	HPA05_CC_P/N	33 / 35
K2 / L1	C12 / C13	HPA10_CC_P/N	34 / 36

Table 12 – HSIO Expansion Site #2 Connections to SOM

5.10 Pmod Expansion Interface

The K24 IO Carrier Card implements a Type-1A Pmod expansion header. This header is expected to provide expansion for low-speed interfaces such as I2C, SPI, UART, etc. The Pmod expansion header is connected to various PL pins and translated where necessary from 1.8V to 3.3V.

Table 13 shows the mapping from the K24 IO Carrier Card to the various PL pins on the Kria K24 SOM. For more details on using the interface with off-the-shelf Pmod devices, please refer to the Digilent Pmod specifications.

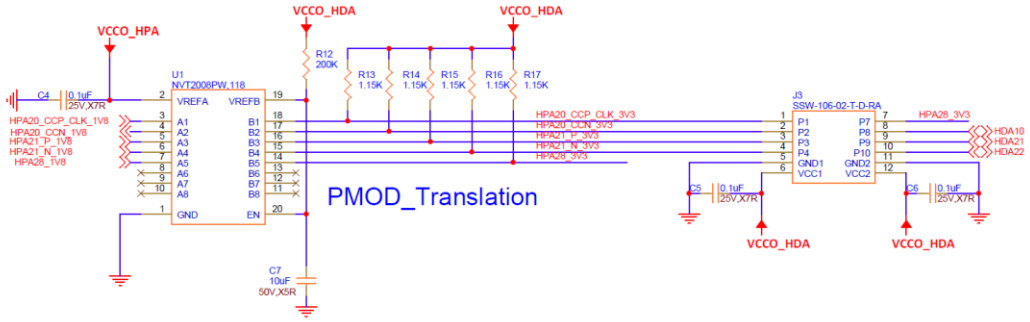


Figure 13 – Pmod Expansion Site Implementation

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	Pmod Interface (J3) Pin Number
A4	A04	HPA20_CCP_CLK	P1
A3	A05	HPA20_CCN	P2
C4	D05	HPA21_P	P3
B4	D06	HPA21_N	P4
D4	B09	HPA28	P7
E10	A16	HDA10	P8
A9	C10	HDA21	P9
A11	A10	HDA22	P10

Table 13 – Pmod Expansion Connections to SOM

5.11 I2C Bus Switch

The K24 Development Kit provides I2C access to the various expansion interfaces through an NXP PCA9544APW,118 which is a 4CH I2C bus multiplexer, **U10**. The PCA9544APW,188 is set to address **0x71**. The I2C bus that is the master to this multiplexer maps to MPSoC via MIO pin **J18** (MIO25_I2C_SCK) and MIO pin **K24** (MIO25_I2C_SDA).

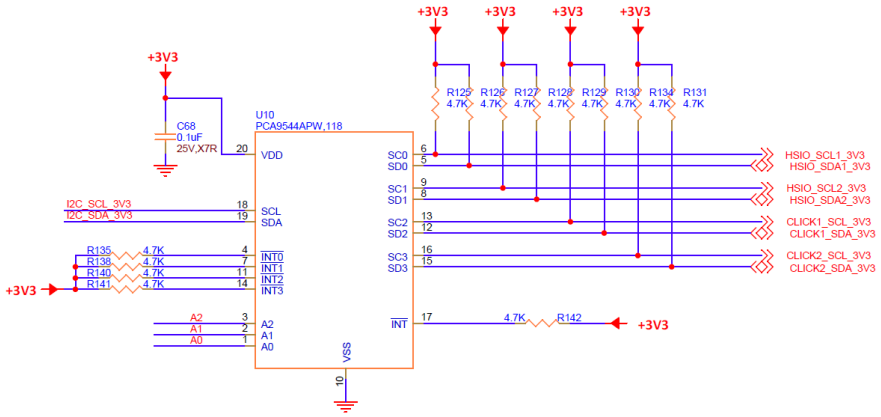


Figure 14 – I2C Bus Switch Implementation

Table 14 shows the list of the expansion interface I2C connections to the 4Ch I2C bus multiplexer.

U10 Mux Port (ADDR 0x71)	I2C Bus Device	Target Device Address
0	HSIO Interface #1 J1	0xTBD
1	HSIO Interface #2 J2	0xTBD
2	Click Interface #1 J4 / J5	0xTBD
3	Click Interface #2 J6 / J7	0xTBD

Table 14 – I2C Bus Multiplexer Connections

5.12 I2C MAC ID EEPROM

The K24 Development Kit contains a Microchip AT24MAC402 I2C based MAC ID EEPROM. This EEPROM provide a unique MAC address for the Ethernet solution on the K24 Development Kit. It also provides the user with 2Kbit of EEPROM storage accessed at up to 1MHz.

The I2C bus that is the master to this EEPROM maps via the MIO pins **J18** (MIO24_I2C_SCK) and pins **K24** (MIO25_I2C_SDA). The I2C address of the MAC ID EEPROM is set to **0x5A**.

There is onboard resistors, R146 / R150, which can be used to enable/disable the WRITE PROTECT feature on the EEPROM. Resistor R150 is populated and R146 is not populated. This disables the WRITE PROTECT feature. If WP is desired, these resistors would need to be modified to enable the WRITE PROTECT feature.

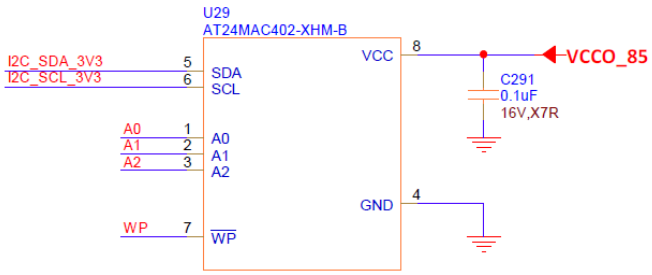


Figure 15 – MAC ID EEPROM

5.13 Board LEDs

The K24 IO Carrier Card contains several board LEDs to convey power and status information to the end user. Table 15 lists these various LEDs and the LEDs respective function.

LED	Schematic Net Name	LED Color	Description
D26	POWER_GOOD	GREEN	Power Sequencing Complete
D4	PS_ERROR_OUT	RED	Power loss, hardware error, or exception in the PMU
D5	PS_ERROR_STATUS	ORANGE	Secure Lockdown State Indicator
D8	UART TX	ORANGE	UART TX Activity
D9	UART_RX	ORANGE	UART TX Activity
D10	PWREN_N	ORANGE	USB-UART Enable
D23	5V_PRESENT	ORANGE	5V Power Supply Present at Connector, J11
D24	9V_PRESENT	ORANGE	9V Power Supply Present at Connector, J11
D25	15V_PRESENT	ORANGE	15V Power Supply Present at Connector, J11
D21	EN_SINK	ORANGE	UPD301C Enable Sink Indicator
D22	CAP_MISMATCH	ORANGE	UPD301C CAP Mismatch

Table 15 – Board LEDs

5.14 User LEDs

The K24 Development Kit provides several User LEDs so an application can display program status visually.

The board provides six fixed color active-high RED User LEDs:

LED	Schematic Net Name	LED Color	SOM Connector Pin (CON1)	MPSoC Pin
D13	MIO27_LED1	RED	D29	L9
D14	MIO28_LED2	RED	D30	J11
D16	MIO29_LED3	RED	C30	M10
D17	MIO30_LED4	RED	C31	K14
D19	HPA23_P	RED	C07	J4
D20	HPA23_N	RED	C08	K4

Table 16 – User Fixed LEDs – PS and PL

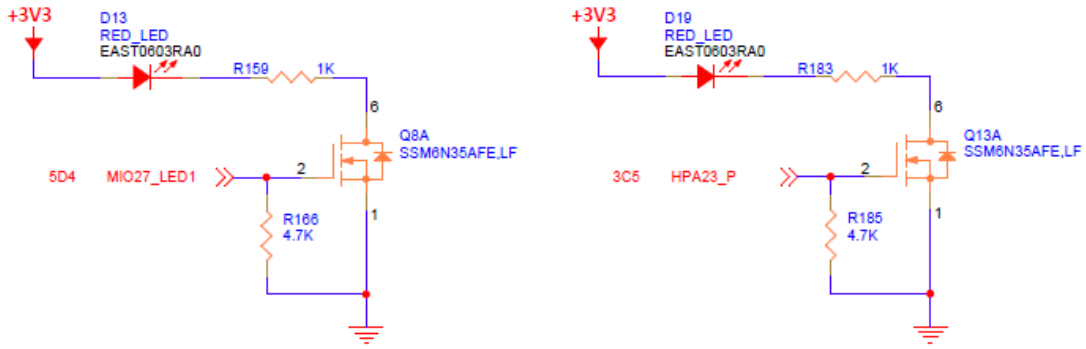


Figure 16 – RED User LED – PS and PL Example

The board also provides two programmable color active-high RGB User LEDs:

LED	Schematic Net Name	LED Color	SOM Connector Pin (CON1)	MPSoC Pin
D15	HPA25_RGB_R1	RED	D08	L6
D15	HPA26_RGB_G1	GREEN	D09	F4
D15	HPA27_RGB_B1	BLUE	B08	B2
D18	MIO38_RGB_R	RED	B32	K12
D18	MIO39_RGB_G	GREEN	B33	K9
D18	MIO40_RGB_B	BLUE	B34	L15

Table 17 – User RGB LEDs – PS and PL

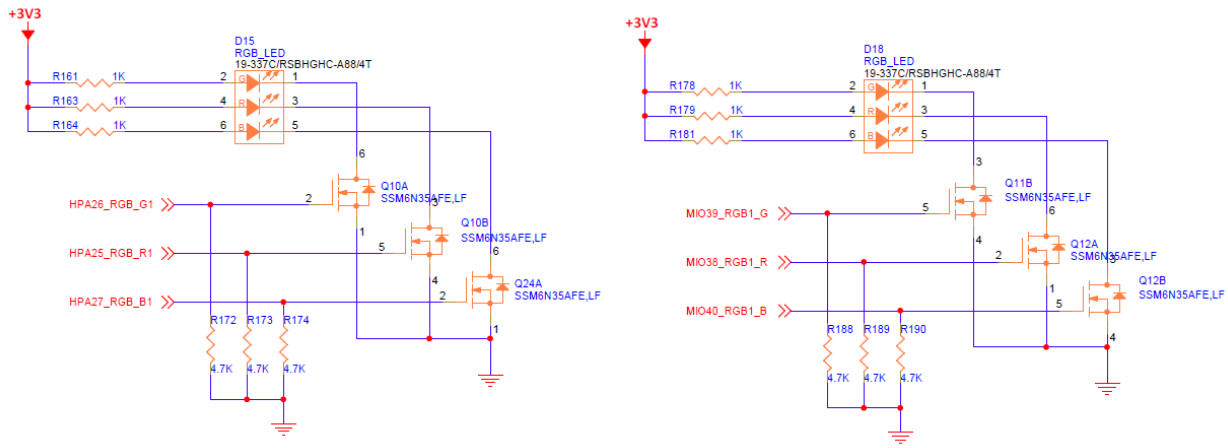


Figure 17 – RGB User LEDs – PS and PL

5.15 User Dip Switch

The K24 Development Kit contains a User Switch so an application can be controlled with a physical switch. The board provides a single User Switch that contains four switches:

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	User Switch (SW1) Pin Number
L13	A34	MIO41_SW1	1 – 8
J9	A35	MIO42_SW2	2 – 7
J15	A36	MIO43_SW3	3 – 6
M13	D32	MIO44_SW4	4 – 5

Table 18 – User Dip Switch Connections to SOM

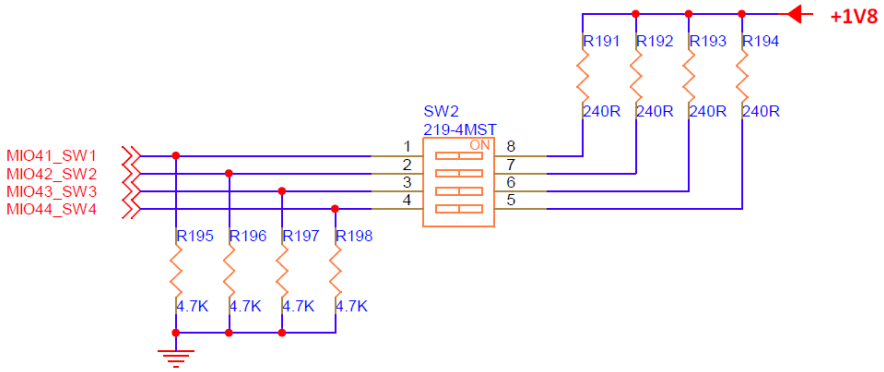


Figure 18 – User Dip Switch - PS

5.16 User Push Buttons

The K24 Development Kit contains User Push Buttons so an application can be controlled with a physical button. The board provides four User Push Buttons:

MPSoC Pin (SOM)	SOM Connector Pin (CON1)	Schematic Net Name	User PB
J12	C32	MIO31_PB1	PB3
K15	B28	MIO35_PB2	PB4
G2	A07	HPA24P_GPIO_PB3	PB5
G1	A08	HPA24N_GPIO_PB4	PB6

Table 19 – User Push Buttons Connections to SOM

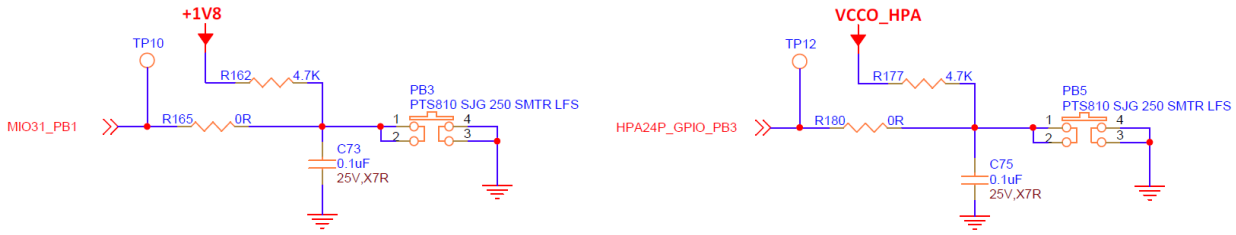


Figure 19 – User Push Buttons – PS and PL Example

5.17 On/Off Power Controller

The K24 Development Kit incorporates an On/Off controller to interface between the on-board power regulators and the Kria K24 SOM. The key inputs/outputs of the system are detailed below:

Signal Name	Source	Destination	Polarity	Description
PWR_PB_N	Push Button (PB7)	On/Off Controller (U21)	Low-Enabled	Push button input for powering on and off. Responds to both short and long pushes. When the system is powered off, a short or long push initiates a power-on sequence. When the system is powered on, a short push will trigger an interrupt to the processor. A long push (~10 seconds held down) issues an interrupt and will power off the system.
MIO34_POWER_KILL_N (Unused on Carrier)	K24 SOM	Not Output from the SOM to the Carrier Card	Low-Enabled	Disable the power regulators immediately. The processor PMU enables this when it has properly processed an internal shutdown command successfully and is ready for the on/off controller to turn off the regulators. Not available from

				the K24 SOM to the K24 IO Carrier Card – Powers down the Kria K24 regulators
EN_SEQ	On/Off Controller (U21)	DC-DC Converters	High-Enabled	Enables the primary 5V power regulator and the power sequencer during a power-up sequence. and de-asserted by the On/Off Controller during a power-down sequence (either a response to KILL_N or a long push).
MIO26_PWR_ INT	On/Off Controller (U21)	Kria K24 SOM	High-Enabled	Interrupt input to the Kria K24 SOM when a power-down push button event has been received.
INIT	Header (J14)	On/Off Controller (U21)	Pin 2-3 Low	When low, the On/Off Controller powers up with the push button control. When high, the On/Off Controller powers up the system as soon as the input voltages are valid.
MIO31_SHUTDOWN	Push Button (PB1)	Kria K24 SOM	Low-Enabled	This is implemented as a generic push button for user access. Could be utilized / implemented for use with the PMU as this pin is available to the K24 IO Carrier Card. Review functionality in the TRM, UG1085.

Table 20 – On/Off Controller Inputs and Outputs

A Renesas GreenPAK programmable device was developed to accomplish the On/Off Controller function on the K24 Development Kit. This device accomplishes everything needed in a very small 2mm x 2.2mm STQFN package. Specifically, the design is based on the Renesas GreenPAK SLG46170 device, with the programmed part number being **SLG7AV45289**.

If you want to duplicate the exact functionality of the On/Off Controller on the K24 Development Kit, the **SLG7AV45289 may be ordered from Avnet**. If you are working on a project with Avnet as your distributor, work with your Avnet FAE to request samples of the device to avoid the 3K MOQ, or you can get Avnet's code for the On/Off Controller to customize it for yourself by submitting a request to your local FAE.

For those that want to modify the power-up initialization from push-button control to power-up with power connected, you will need to move a shunt on the K24 IO Carrier Card, **J14**. By default, **J14** is shunted which selects either pull-down (default, use Push Button) or pullup (power up with power provided to the board). To implement the Power Up with Power Connected function, change the default shunt location on **J14** from pin 2-3 to pin 1-2.

To help explain the functionality of this device, a datasheet is available at **Renesas SLG7AV45289 On-Off Controller Datasheet**. Also, here are the functional diagrams showing the logic within this device.

5.18 Power Regulation

There are 5 voltage regulators and 3 load switches that reside on the K24 IO Carrier Card that provides 1.2V, 1.8V, 3.3V, and 5V power rails to the K24 Development Kit. These voltages are used to power the peripheral devices as well as the Kria K24 SOM.

The primary voltage used to power the Kria K24 SOM is 5V and is supplied by 1 regulator and 1 load switch.

- VCC_SOM +5.0V Renesas ISL85014FRZ / OnSemi NCP45524IMNTWG

There is a voltage that drives the HPIO banks and HDIO banks of the MPSoC and are required by the Kria K24 SOM. These voltages are supplied by 3 regulators and 2 load switches depending on the power sequence.

- VCCO_HDA +3.3V TDK FS1404-3300-AS / OnSemi NCP45524IMNTWG
- VCCO_HPA +1.2V TDK FS1406-0600-AS / OnSemi NCP45524IMNTWG
- VCCO_HPA +1.8V TDK FS1406-0600-AS / OnSemi NCP45524IMNTWG

There is a single voltage generated on the board that is always-on when the Type-C power supply cable is attached to the K24 Development Kit. This regulator named 3V3_PRI is a +3.3V supply that is used to handle functions on the board prior to the board being powered up.

- 3V3_PRI +3.3V OnSemi NCP718ASN330T1G

5.19 Power Sequencing

The K24 Development Kit power architecture follows the POWER SUPPLY SEQUENCING GUIDELINES provided in the Kria K24 SOM Datasheet, DS985**.** The following is a quick list of the recommended power-on / power-off sequencing:

Power-ON Sequence:

POWER-UP: 3.3V_PRI active and On/Off Controller enabled with PB7 activation / Type-C plugged-in J11

EN1: +5V generated from Type-C power and switched to provide power to the SOM

EN2: +3.3V, +1.8V, and +1.2V generated following power-good from EN1 regulators

VCCO_EN: EN3 and VCCOEN_PL_M2C from K24 SOM switches VCCO_HDA and VCCO_HPA

Power-OFF Sequence:

The reverse of the Power-ON Sequence.

To meet the power sequencing guidelines for the K24 Development Kit a power sequencer is used featuring a Renesas GreenPak device. This device can sequence several regulators using combinations of EN (enable) pins and PG (power good) pins and logic gates.

The Renesas GreenPak is a custom programmed device and is available from the Renesas factory. The Renesas part number is **SLG7TD43741VTR**. Here is a link to the device datasheet **SLG7TD43741 TDK**

Power Strip Sequencer. Contact your local FAE if you would like more information about the **SLG7TD43741VTR**.

The following figure is a timing diagram of the **SLG7TD43741VTR**. The EN_SEQ signal represents the CTRL pin on the device and is used to start the power sequence on power up or reverse the power sequence on power down.

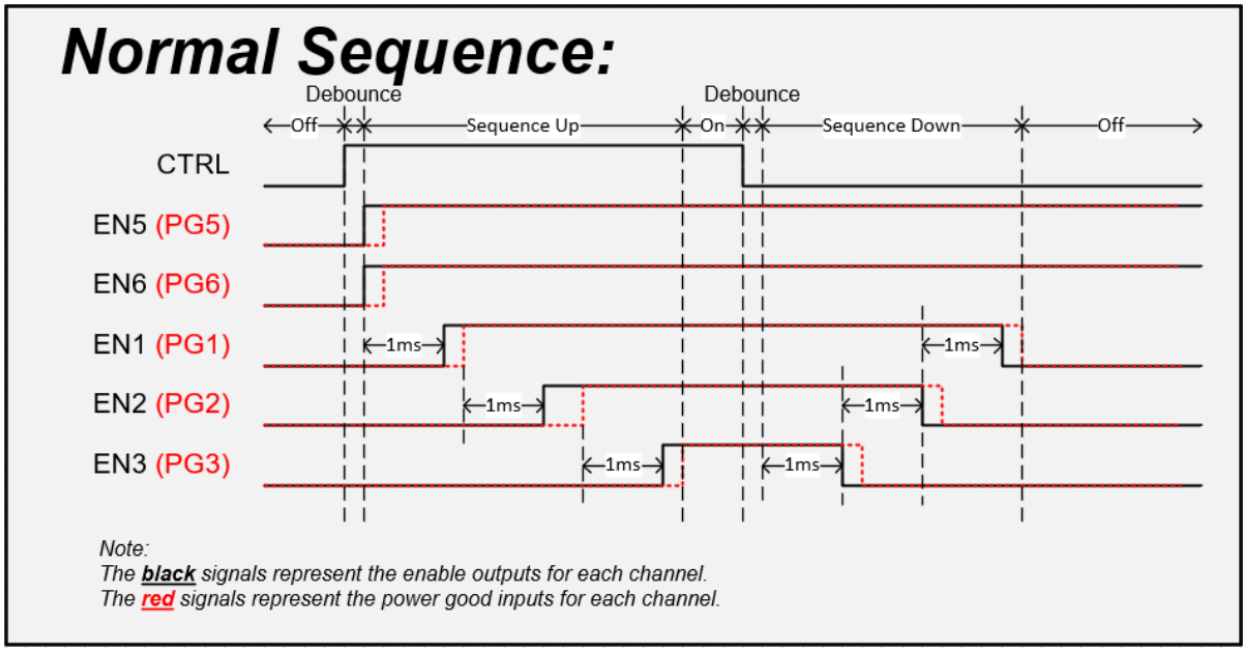


Figure 20 – Power Sequencer Timing Diagram

The following figure shows how the K24 Development Kit implements the **SLG7TD43741VTR**.

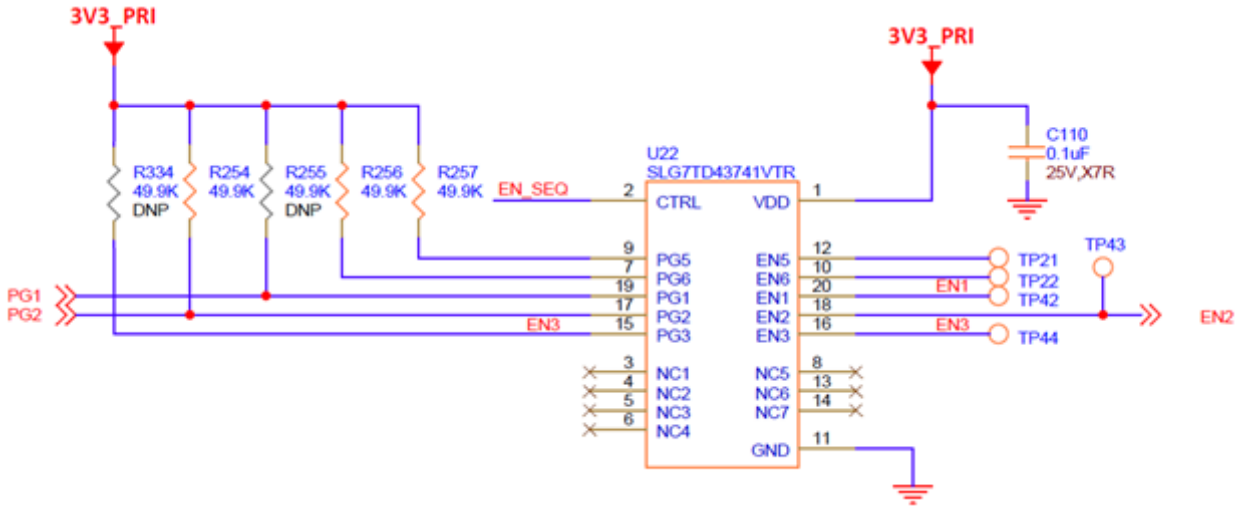


Figure 21 – Power Sequencer Schematic

5.20 Thermal Management

Depending on the end-user application, the performance of the K24 Development Kit may require a thermal solution to help maintain performance across temperature. The K24 Development Kit has been tested only with the thermal plate attached to the Kria K24 SOM.

Under most circumstances on a passive heatsink may be required to provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-user's thermal environment and the possible enclosure of the K24 Development Kit. For aggressive applications it is recommended that an accurate worst-case power analysis be performed to avoid the pitfalls of over designing or under designing your product's power and thermal management system.

NOTE: End users should design a custom thermal solution that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system. When designing a custom thermal solution, it is recommended to review the mechanical information provided by AMD for the Kria K24 SOM in the Kria K24 SOM Datasheet, DS985 and the thermal information provided in the Kria K24 SOM Thermal Design Guide, UG1094.

5.21 Recommended Operating Conditions

This section contains the recommended operating conditions for AUBoard-15P Development Kit. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

Parameter	Min	Max	Units	Notes
Operating Temperature	0	70	C	

Table 21 – Recommended Temperature Range

Parameter	Min	Max	Units	Notes
Input Voltage	14.55	15.45	V	Type-C Power Supply 15V/3A

Table 22 – Recommended Input Voltage

5.22 Mechanical

The K24 Development Kit is designed to be a cell phone sized form factor. The board measures 135mm x 80mm (approximately 5.315" x 3.15").

Several factors can affect the maximum vertical dimension of the board including the Kria K24 SOM height, custom heatsinks attached to the board, and boards attached to expansion ports such as the MikroE Click site or the HSIO expansion sites. A STEP model / DXF file of the PCB and its components can be made available to end users that may require it.

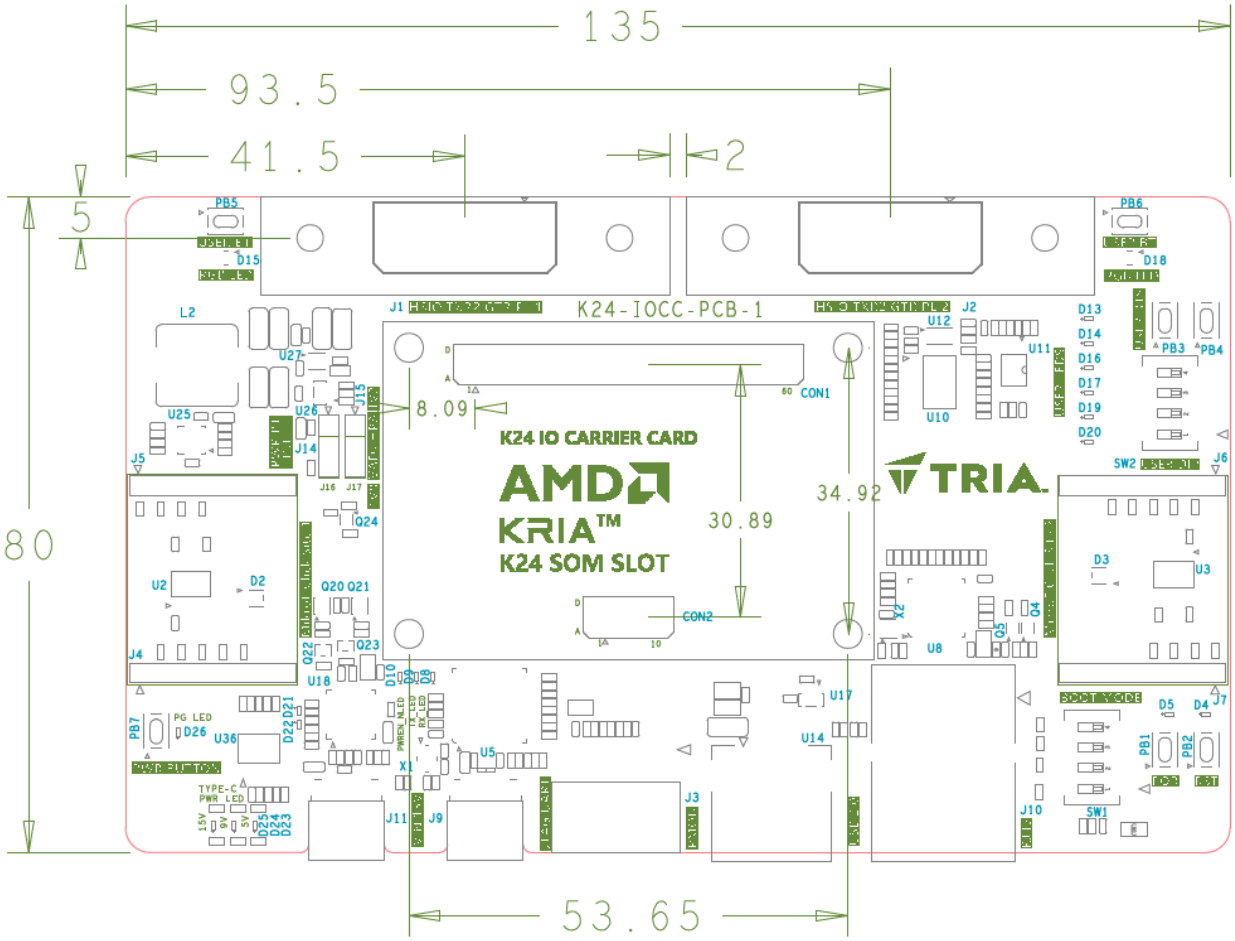


Figure 22 – Mechanical Dimensions

6 Getting Help and Support

If additional support is required, TRIA Technologies has many avenues to search depending on your needs.

For general question regarding K24 Development Kit, please visit our website at **http://avnet.me/k24-dk**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

Detailed questions regarding K24 Development Kit hardware design, software application development, using AMD tools, training and other topics can be posted on the K24 Development Kit Support Forum at **http://avnet.me/k24-dk-forum**. Avnet's technical support team monitors the forum during normal business hours in North America.

Those interested in customer-specific options on K24 Development Kit can send inquiries to **customize@avnet.com**.