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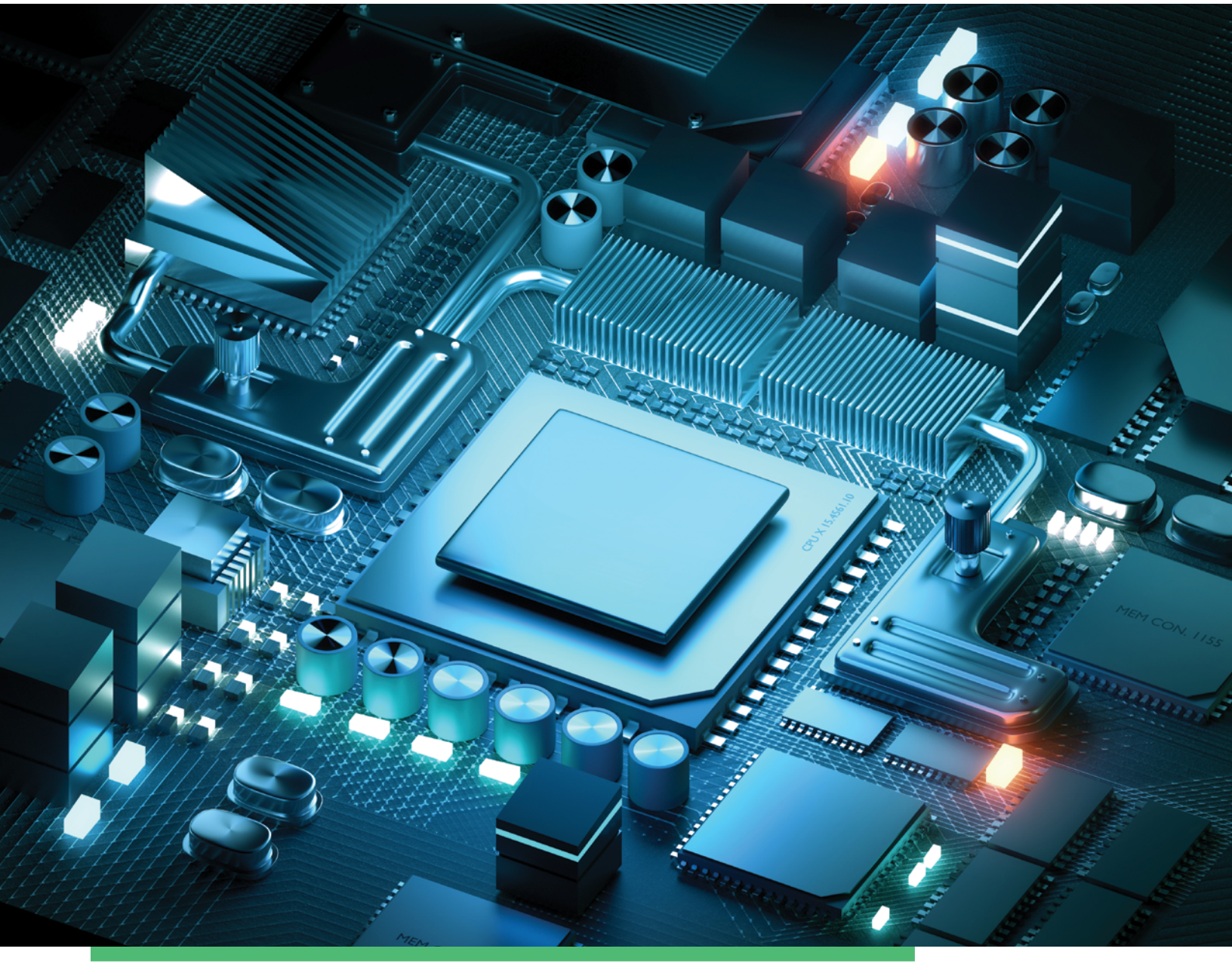

How employing the latest server processor technology can reduce costs through performance and efficiency gains.

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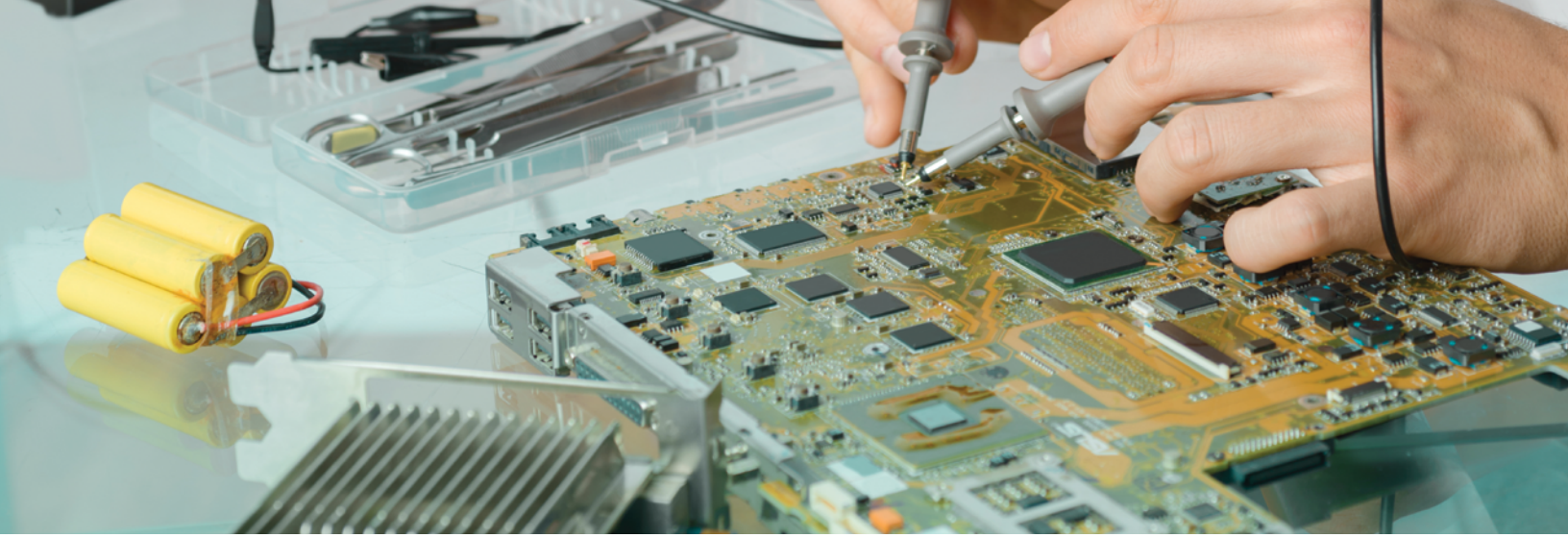


HOW EMPLOYING THE LATEST SERVER PROCESSOR TECHNOLOGY CAN REDUCE COSTS THROUGH PERFORMANCE AND EFFICIENCY GAINS.

Enterprises face many challenges in achieving their IT goals, from extensive software licenses to a broad range of options in configuring hardware. A misstep in hardware configuration can negatively impact software performance, incur unforeseen financial costs and negatively impact user experience. Solid planning can help address these challenges by properly implementing IT hardware that optimizes costs and delivers the best possible performance.

Criteria to consider when evaluating server processors:

1. Cores/threads
2. Sockets
3. L3 cache
4. Non-uniform memory access (NUMA)
5. Maximum memory
6. Memory channels
7. PCIe generations and lanes (PCIe 4.0 channels)
8. Server CPU security

1. CORES/THREADS

Server processors are offered with a wide range of core counts with eight at the beginning of the range and 64 being at the current top of the market. As more cores are integrated into a processor, the additional cores are able to split up the processor's tasks. Overall this makes the processor faster and operate more efficiently. While a thread is considered a virtual version of a CPU core, it's the threads which allow the CPU to perform multiple operations simultaneously. In order for a server to execute multiple intensive processes quickly, a CPU core with many threads is required. While CPU core count is important for performance, it's also vital that the core have the necessary thread count to execute applications properly. The current maximum available thread count per socket is 128 for a 64 core CPU.

AMD EPYC 7002	
Cores	8 to 64
Threads (2x Core)	16 to 128

2. SOCKETS

A socket is the slot on the printed circuit board (PCB) of the server that provides the electrical and mechanical connections needed to connect the CPU chipset. Traditionally, PCB boards on servers and high-performance computing (HPC) devices have had paired sockets ranging from 2-4. This allowed for parity in running multiple CPU configurations. As current multi-core processors have grown more powerful and efficient, the use of single-socket configurations has increased dramatically.

According to a recent Gartner study, by 2021, dedicated x86 **single-socket servers will address 80% of the workloads** in use in enterprise data centers, up from 20% in 2018. The reason for this shift is the limitations on memory and input/output (I/O) capacity of individual CPUs. Businesses often over purchase processing capacity to allow for growth and to ensure that applications run properly. On older CPU designs, it often requires two CPUs and two cores plus additional memory. This can now be accomplished today by one powerful multi-core CPU.

The further benefits of single-socket architecture includes hardware cost savings on CPUs, PCB boards, memory, heat sinks fans and other components. An additional benefit of a single-socket configuration is the ability to reduce application and workload complexity through better use of I/O and non-uniform memory access (NUMA) bandwidth. Without having to share resources with other processors, a properly configured single-socket server can reduce bandwidth degradation by **35% and latency by as much as 75%.** The simplicity of a single-socket solution can also mean less network configuration errors (ghosts) that can often be traced back to multiple processors that are not communicating properly in a dual or quad socket configuration.

A single-socket configuration will use less electrical power to operate and can easily reduce the number of physical servers required, saving on space, maintenance and cooling requirements.

Cost savings in power consumption and overhead should also be taken into consideration. A single-socket configuration will use cooling requirements. This can equate to as much as a 61% reduction in power consumptions, 50% fewer servers, with an overall total cost of ownership (TCO) reduction of up to 54%.

3. CACHE MEMORY

L1, L2 and L3 caches are different hierarchies of memory on a CPU processor that are similar to the RAM in a computer. Cache memory is designed to reside as closely as possible to the processor in order to decrease the time required to access data. This amount of time is referred to as latency. The architecture of L1, L2 and L3 cache memory also differs considerably. Higher level caches (L2 and L3) are more tightly packed and use smaller transistors, but the tradeoff has traditionally been that these forms of cache memory are slightly slower, but still much faster than utilizing RAM. Before the advent of high-speed memory, processor performance was often hampered by the delay of data caused by slow memory. Processor performance is not entirely based on the CPU, but also on the size and type of cache memory that directly feeds the CPU data.

Cache memory has addressed this and can access data in nanoseconds, which helps the CPU execute intensive functions very quickly and efficiently. In general, the more cache memory a CPU processor is designed with **will improve the per-core performance** and greatly enhances the execution and stability of target applications in server and HPC configurations, including the operation of virtual desktop environments.

4. NON-UNIFORM MEMORY ACCESS (NUMA)

NUMA is a computer memory design used in multiprocessing, where the memory access time depends on the physical memory location relative to the processor. Using NUMA, a processor can access its own local memory faster than non-local memory, this is memory local to another processor or memory shared between processors. The benefits of NUMA are limited to particular workloads, notably on servers where the data is often associated strongly with certain tasks or users, especially in VM environments.

The central IO die used in AMD EPYC 7002 Series processors helps with obtaining workload performance consistency by improving memory latencies. It also allows the CPU to be configured as a single NUMA domain enabling uniform memory access for all the cores in the socket.

Using the servers running AMD EPYC 7002 Series processors as an example, the NUMA Nodes Per Socket (NPSx) BIOS settings on a system can be configured with 1,2,4 or 8 domains. Applications that are highly NUMA optimized can improve performance by setting the number of NUMA Nodes per socket to a supported value greater than 1.

EXAMPLES OF NUMA/NPS CONFIGURATIONS USING AMD EPYC 7002 CPUS:

NPS1 designates the CPU as a single NUMA domain. This places all of the cores in the socket and all of the memory into a single NUMA domain. Memory is interleaved across the eight memory channels. All PCIe devices on the socket belong solely to this single NUMA domain.

NPS2 partitions the CPU into two NUMA domains. This places half of the cores and half of the memory channels on the socket into one of two NUMA domains. Memory is interleaved across the four memory channels in each NUMA domain.

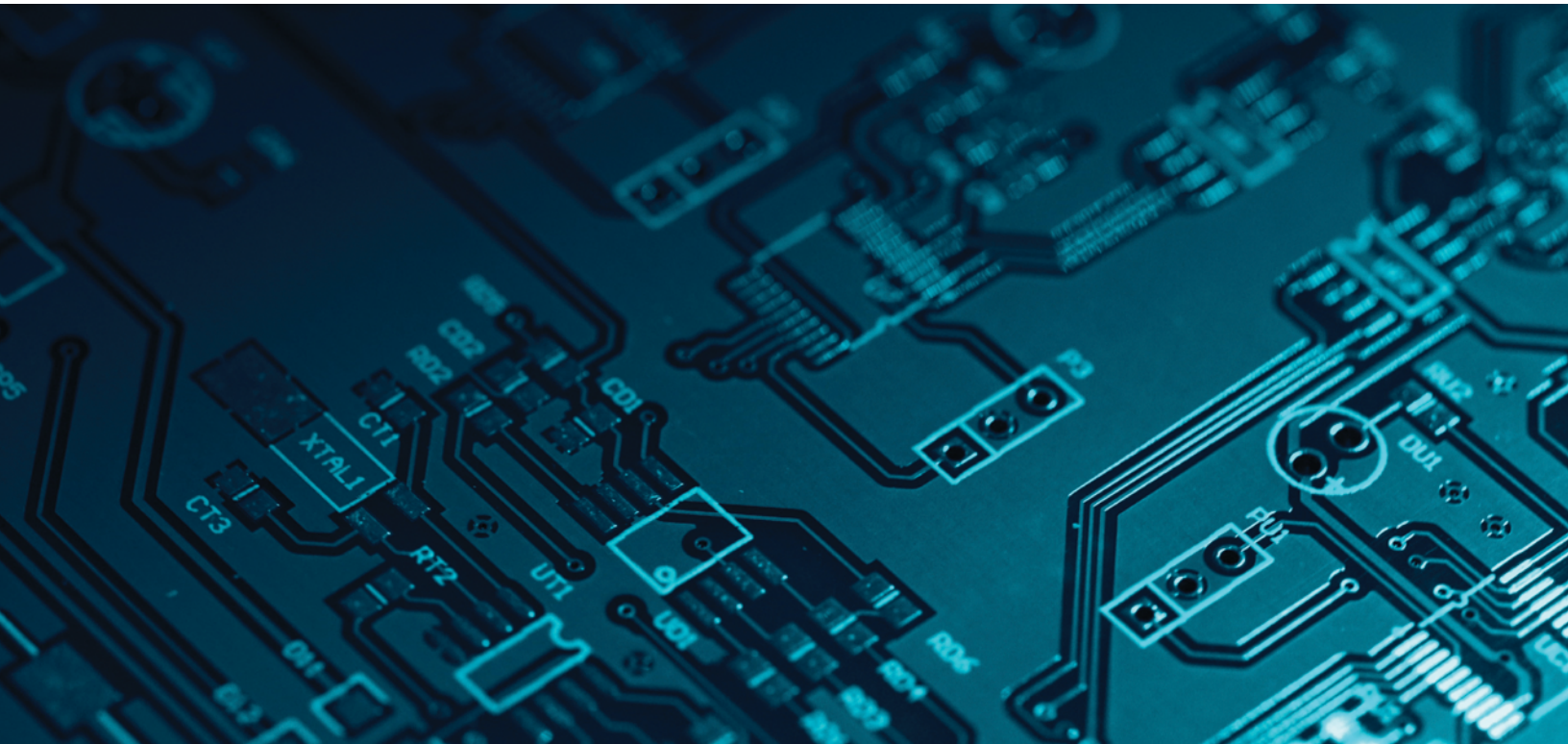
NPS4 partitions the CPU into four NUMA domain quarters. Each quarter is a NUMA domain and memory is interleaved across the two memory channels in each quarter. PCIe devices will be local to one of the four NUMA domain quarters on the socket depending on which quarter of the IO die has the PCIe root for that device.

It is worth noting that not all CPUs can support all NPS settings. Please refer to the CPU technical specifications for exact details.

LLC AS NUMA NODE

This capability specifies whether the processor last-level caches (LLCs) are exposed to the operating system as NUMA nodes. In certain server applications where workloads are managed by a remote job scheduler, it is desirable to pin execution to a single NUMA node, and preferably to share a single L3 cache within that node. BIOS Setup should support an L3AsNumaNode (Boolean) option to create a NUMA node for each Core Complex (CCX) L3 Cache in the system.

When enabled, this setting can improve performance for highly NUMA-optimized workloads if the workloads or related components can be pinned to cores in a CCX and if they can benefit from sharing an L3 cache.



5. MAXIMUM MEMORY

While cache memory is crucial for the CPU processor to execute functions, RAM (random access memory) is an essential component of any server hardware. RAM provides the space needed by the server to read and write data that's then executed by the CPU processor. The more RAM a server has, the less the CPU processor will have to read data from the hard drive. This benefits the server's operation by increasing its overall speed and performance since RAM is much faster than a hard drive. The effectiveness of the server's RAM memory has a direct effect on productivity. Insufficient server memory can cause troublesome bottlenecking, meaning that the CPU processor is left waiting on data to execute functions, which prevents the server from efficient operation.

Not all RAM is the same. Much like the CPU processor, RAM speed is measured in megahertz (Mhz). This is a measure of the clock speed of how many times per second the RAM can access its own memory. For computationally intensive applications, a good practice is to configure the server with the highest speed of memory available, currently 3200Mhz, and in large amounts, current maximum configurations are in the range of 4TB.

Ensuring that a server is configured properly with the right type and size of RAM means that it can handle more data-intensive applications like virtual machines (VMs), distributing their loads more effectively and helping enterprises to run more efficiently.

For reference:

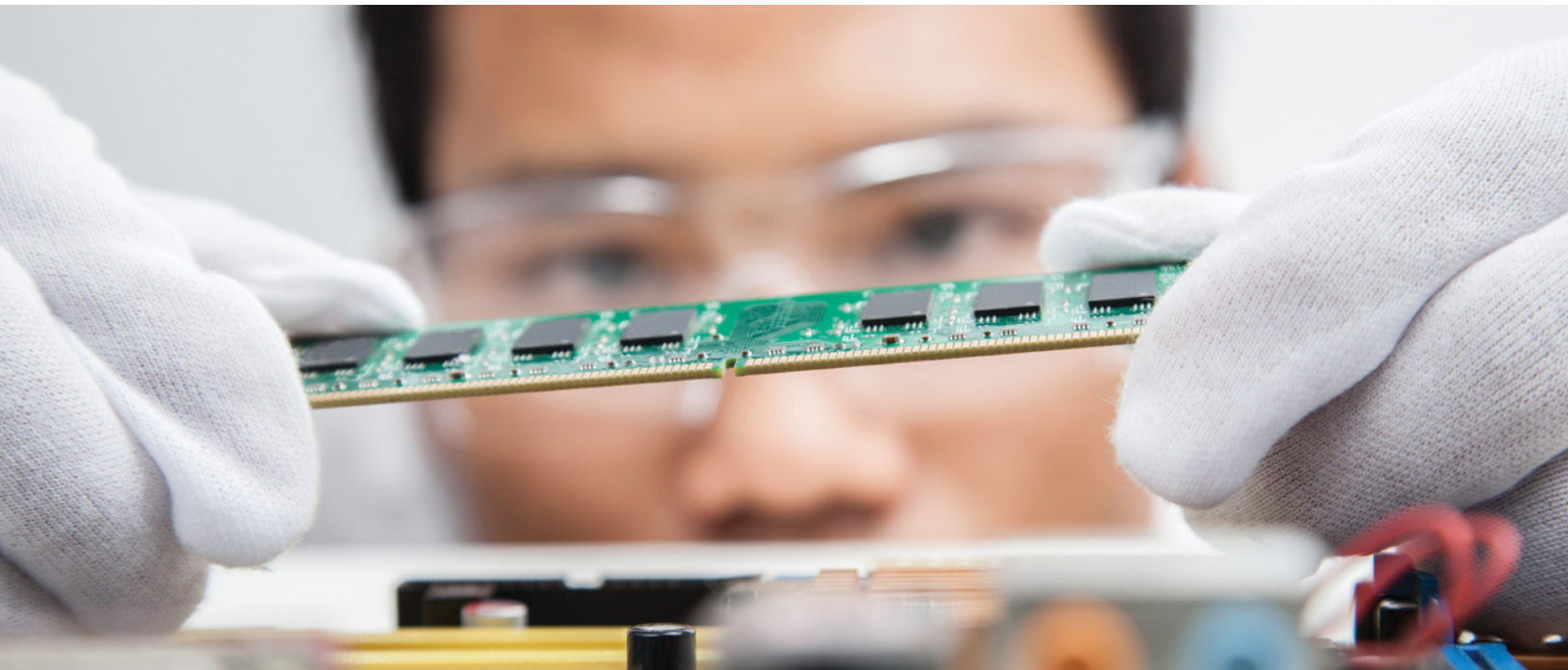
AMD EPYC 7002	
Memory channels	8
Max. memory speed	3200Mhz
Max. memory capacity	4TB

6. MEMORY CHANNELS

Multi-channel memory architecture is a technology that increases the data transfer rate between RAM memory and the memory controller by adding more channels of communication between the two. This multiplies the data rate by exactly the number of channels present. In practice, the greater the number of memory channels that are designed into a CPU processor the better the speed and performance of the system.

For reference:

AMD EPYC 7002		
Memory channels	8	4TB



7. PCIE GENERATION AND LANES

PCIe (Peripheral component interconnect express) is a high-speed serial computer expansion bus standard. A PCIe connection consists of one or more data-transmission lanes, connected serially. Each lane consists of two pairs of wires, one for transmitting and one for receiving. It's the common high-speed interface for linking graphics/video cards, hard drives, SSDs, Wi-Fi and Ethernet hardware to a computer motherboard. The PCIe standard is currently in its fifth generation. Most server configurations are currently running the third-generation PCIe standard. AMD is first to provide PCIe 4.0 support at 16 GT/s (31.5 Gbps) and Intel follows with the Rocket Lake series of processors. No manufacturers currently offer CPU processors with the fifth-generation PCIe standard.

PCIE GENERATIONS CHART					
	1st gen (2003)	2nd gen (2006)	3rd gen (2010)	4th gen (2017)	5th gen (2019)
Speed:	2.5 GT/s (4GBps)	5.0 GT/s (8GBps)	8.0 GT/s (4GBps)	16.0 GT/s (31.5GBps)	32.0 GT/s (63GBps)

For reference:

AMD EPYC 7002	
PCIe generation	4th
PCIe lanes	128

8. SERVER CPU SECURITY

Security has always been a major concern in IT. The number of successful cyberattacks has increased, as has the motivation of hackers to find and exploit vulnerabilities, whether for criminal or state purposes. The growth of shared resources, virtualization and cloud-based infrastructure has presented new challenges to IT environments with solutions placing more emphasis on the CPU as the root of security.

Both Intel and AMD have implemented security solutions on the CPU level. Here is a brief guide to their respective solutions.

SGX

Software Guard eXtensions has been Intel's most well known and advanced processor security feature. SGX allows applications to store sensitive data like cryptographic keys in a secure virtual environment inside hardware-encrypted RAM that can't be accessed by the main operating system or other third-party applications. Certain applications like the end-to-end encrypted signal messenger can make use of SGX to pair users to each other both securely and privately.

TME/MKTME

Total Memory Encryption (TME) and Multi-Key Total Memory Encryption (MKTME) encrypt all memory instead of a limited section like SGX does. TME offers a single encryption key for all memory, while MKTME delivers full memory encryption with support for multiple keys, such as one key per encrypted VM.

SESS

AMD's Silicon-Embedded Security Subsystem (SESS) is an embedded security processor in the I/O die of the processor. A feature unique to AMD, this hardware root of trust helps protect confidentiality and integrity of data with virtually zero impact to system performance.

SESS delivers a number of benefits including:

- Secure memory encryption with no changes in software through a simple BIOS setting
- 509 encryption keys available for secure encrypted virtualization
- AES-128 encryption engines built into the memory controllers
- CPU cores that actively isolate different memory sources
- Support of secure guest migration
- Attestation handling capability
- Secure boot process with protection against booting down-level software

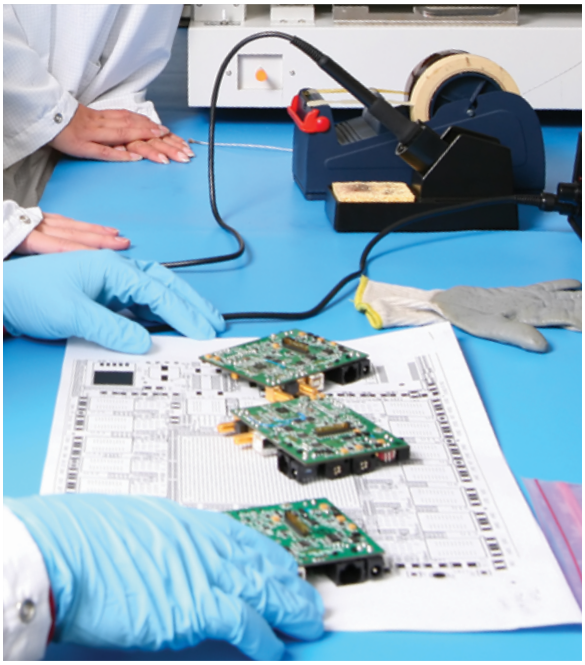
TSME

AMD's Transparent Secure Memory Encryption (SME) is a stricter subset of SME that encrypts all memory by default and doesn't require applications to support it in their own code. This makes it more useful for legacy applications that can no longer be expected to modify their code but can still reap the benefits of data encryption. An extension of SME is Memory Guard, which protects a system's data against cold boost attacks.

SEV

AMD's Secure Encrypted Virtualization (SEV) is an extension of SME that encrypts the memory of each VM with individual encryption keys. This allows VMs to stay completely isolated from one another. AMD developed this solution while working on security protocols for the Microsoft Xbox and Sony PlayStation consoles.

After providing an overview of current server CPU processor technology, it's now time to focus on specific use cases where the practical application of the technology can be used to addressed specific challenges.



UTILIZING PCIE LANES, NOT PCIE SWITCHES IN OPTIMIZING PERFORMANCE AND COSTS

PCIe provides the necessary high-speed links to peripherals and memory banks that are required to properly run applications. As the maximum number of PCIe lanes becomes occupied on a CPU processor, additional hardware known as PCIe switches becomes necessary to add to the configuration.

The three most common reasons that PCIe switches are added to a configuration include:

1. Lane Swapping
2. Port expansion and fanout
3. Bridging

1. LANE SWAPPING

A good analogy for lane swapping is that it's similar to having a box full of cables with none having the proper end to match a necessary device. PCIe host adapters such as CPUs come configured in only one manner, for example, one x16 (sixteen lanes per device). But suppose two sets of x8 or eight sets of x2 are required. A PCIe switch can perform the necessary lane swapping to connect your devices. Although this is accomplished through the addition of a PCIe switch hardware, the architecture could easily be embedded on the CPU processor with the decoders being in peripherals or coprocessors.

2. PORT EXPANSION / FANOUT

The term fanout is used to describe a situation when more PCIe connections are required in a configuration than are available on the CPU processor, SoC, MCU, Southbridge or multi-I/O controller.

While most manufacturers design a limited number of PCIe ports on their CPU processors, some only offer one. This makes the additional PCIe switch hardware a necessity for port expansion.

Practical examples of using fanout for configuration improvements include the addition of host bus adapters, where the CPU/SoC uses the switch to talk to local resources or bus/backplane-based resources. A PCIe switch can be used between a CPU processor and two memory controllers (SSD or solid state drives, RAID or redundant array of independent disks, etc.) or non-volatile memory host (NVMe) devices like SSD to switch between different memory banks or arrays. This increases the density and improves speed through memory striping.

3. NON-TRANSPARENT BRIDGE (NTB)

In many applications there is a need to interconnect two independent PCI domains. A non-transparent bridge (NTB) enables this inter-domain communication, facilitating communication between devices in different switch partitions. This ability enables both hosts and end points to initiate transactions to other hosts and/or end points in another switch partition.

MORE PCIE LANES ON A CPU PROCESSOR NEGATES SWITCHES, REDUCING HARDWARE COSTS

Modern server CPU processors are now coming standard with up to 128 PCIe lanes. This negates the need for additional hardware like PCIe adapter cards and switches which can add an estimated $9,000 to the cost of a server configuration not to mention complexity. **Currently, AMD is the only chip manufacturer to offer the new PCIe 4.0 standard.**

One of the main benefits of PCIe 4.0 is that it doubles the maximum throughput of the previous 3.0 standard, improving the maximum data transfer rate of 16Gbps to nearly 31.5Gbps. The number of PCIe lanes (x1, x4, x8 or x16) has stayed the same, meaning that there is now twice the bandwidth per lane compared to PCIe 3.0. This means that a x8 PCIe 4.0 slot will provide similar performance to a x16 PCIe 3.0 slot, analogous to doing more with less.

If your server configuration relies primarily on storage devices to do heavy lifting, you'll notice definite improvements with PCIe 4.0. This helps greatly with I/O-bound applications like VMs.

Cloud applications, climate research, AI development — all require high-speed access to storage in order to crunch data quickly, reduce latency and avoid bottlenecks. The extra bandwidth provided by PCIe 4.0 also allows for the connection of more PCIe devices. While PCIe 4.0 is backwardly compatible with previous generations of the standard, in order to realize the full benefit of this new technology a PCIe 4.0 device must be connected to a PCIe 4.0 motherboard with a compatible CPU processor.

By adopting the PCIe 4.0 standard through new hardware, one way enterprises can decrease costs and increase margins is through the adoption of high-speed solid-state drives (SSD). SSD is a nonvolatile media that stores persistent data on flash memory. There are two essential parts to an SSD drive — a NAND flash memory and a flash controller optimized to deliver high read-write performance in sequential as well as random data fetching. SSDs have no moving parts to break or spool up or down, as is the case with hard disk drives (HDD) with rotating magnetic media. SSDs provide distinct performance advantages which include speed, weight, durability and energy consumption over older HDD drives.

HOW MODERN CPU PROCESSORS CAN HELP REDUCE COSTS BY LOWERING POWER CONSUMPTION

In many applications there is a need to interconnect two independent PCI domains. A non-transparent bridge (NTB) enables this inter-domain communication, facilitating communication between devices in different switch partitions. This ability enables both hosts and EPs to initiate transactions to other hosts and/or EPs in another switch partition.

Data centers can now pack more processing power into less real estate, but high-density computing environments can be a large drain on operating budgets for several reasons:

1. Expanding power demands
2. Increasing power costs
3. Excessive heat

With thoughtful planning, even a small data center can save tens of thousands of dollars by making smart choices in IT hardware, management practices, power and cooling infrastructure. The three-year utility savings from an energy-efficient server can almost cover the purchase price of the server itself. Couple this strategy with energy-efficient power and cooling systems, and **a midsized data center with 1,500 servers could save millions of dollars in power consumption costs** while reducing the organization's carbon footprint.

One of the best ways to reduce power consumptions costs is to focus on the server's CPU processor. **More than 50%** of the power required to operate a server is utilized by the CPU. Power-management features offered by CPU manufacturers can optimize power consumption by dynamically switching among multiple performance states that vary frequency and voltage based on CPU utilization — without having to reset the server.

When the CPU is operating at low utilization, the power-management feature can minimize wasted energy by dynamically ratcheting down processor power states through lower voltage and frequency when peak performance isn't required. Adaptive power management reduces power consumption without compromising processing capability. If the server CPU operates near maximum capacity most of the time, this feature offers less of an advantage, but it can produce significant savings when CPU utilization is variable. **If a data center with 1,000 servers reduced CPU energy consumption by 20%, this would translate into an annual savings of nearly $200,000.**

A number of server CPUs on the market provide this capability, but it's not always enabled. If your current CPUs lack this capability, strongly consider it when making future server purchases.

CPU manufacturers are continuously developing more energy-efficient chipsets with increased processing capabilities that can handle higher loads of data with less power. One of these technologies is the 7nm photolithography process used in the manufacturing of CPU processors. The photolithography process employs powerful light sources to etch an image of the CPU onto a piece of silicon. The exact method of how this is accomplished is referred to as the process node and is measured by how small the billions of transistors can be made.

Overall, smaller transistors are more energy efficient, they can do more calculations without generating as much heat, which is one of the limiting factors for CPU performance. It also allows for smaller die sizes, which reduces costs and can increase density at the same sizes, this means more cores per CPU processor. 7nm CPUs are twice as dense as 14nm nodes, which allows manufactures to release 64 core server CPUs. **This is a massive improvement over older 14nm processors which were roughly limited to a maximum of 32 cores and not nearly as energy efficient.**

With the increased efficiency of 7nm photolithography process, more cores are able to be designed into a single server CPU processor. One 64-core processor with 128 threads in a single socket configuration can now handle the processing requirements that were previously addressed by two 32-core processors in a dual-socket configuration. The benefits of eliminating one processor and using one less socket include more simplified server configurations, less heat generation and reduced energy consumption. A properly configured single-socket server can deliver about a 30% TCO advantage over a mainstream two-socket server. AMD is currently touting its EPYC 7702 line of server CPU processors as two-socket features and performance running on a one-socket budget.

MORE PROCESSOR CORES EQUAL BETTER VALUE

When it comes to handling VMs, server CPU processors with faster cores will often come out ahead in the TCO equation for software that is licensed on a per-core basis. This is because the faster CPUs can better utilize the software license. Choosing CPU processors with faster cores also results in better performance for each license, which reduces the need for additional licenses and the overall cost of the server platform. High-speed, multi-core processors are the best choices for hyperconverged infrastructure (HCI), high-performance computing (HPC) and relational database applications.

But with the changes in licensing structures that many software companies including VMs are implementing on multi-core processors, where can real value be derived? The answer is in functionality of the server and its physical footprint. A single server running one or more sockets of processors with high core counts can easily deliver the performance of multiple lower core count systems. This requires less power to operate, less maintenance and oversight by IT staff, less required space and a strong savings over purchasing additional system hardware.

FINDING THE RIGHT TECHNOLOGY PARTNER TO MAXIMIZE YOUR HARDWARE POTENTIAL

Avnet Integrated offers unique technology solutions to companies worldwide, enabling them to meet the needs of their customers while increasing profitability and reducing risks. What's more, we're a global leader in integration and professional services including expertise in installation, warranties, maintenance and even data migration.

Across our 10 global technology campuses, our engineers work with leading companies to identify and validate the perfect hardware solutions using the latest server technologies. We handle every aspect from design to delivery — including supply chain management, solution integration and testing, custom branding and packaging, and drop shipping to your customers and installing your solution.

TAKEAWAYS

There are a number of factors that drive cost savings in the server market, but choosing the right CPU is paramount for efficiency, performance and achieving the lowest TCO. The latest features in modern server CPUs like PCIe 4.0, 64-core architecture and advanced power management deliver multiple benefits including increased performance, enhanced speed and cost savings.

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