ERRATA

January 6, 2025

Products Affected:

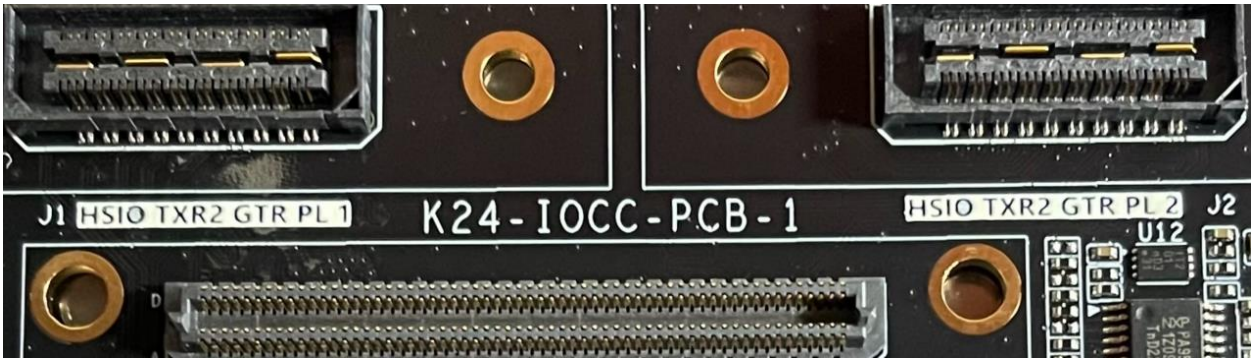
K24 Development Kit – Revision 1

Introduction:

Thank you for your interest in the Tria K24 Development Kit. Although Tria has made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification. Be aware that any of the optional workarounds requiring physical modifications to the board are done at the user's own risk, and Tria is not liable for poorly performed rework.

Identifying Affected Boards:

The K24 Development Kits affected by these errata can be identified by the PCB Revision listed in silkscreen on the top of the K24 IO Carrier Card PCB. The PCB Revision of the K24 IO Carrier Card is listed in silkscreen and can be found on the top side of the board between the HSIO connectors and the topmost connector of the K24 System-On-Module. The current production revision is "K24-IOCC-PCB-1". Boards that are at this production revision are affected.



Board Top Side View

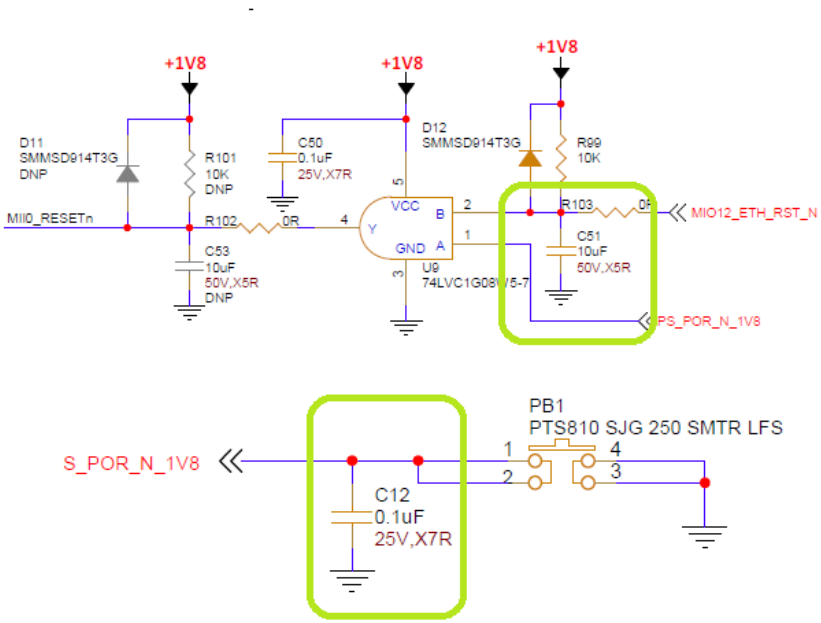
Errata:

Ethernet Reliability Issues

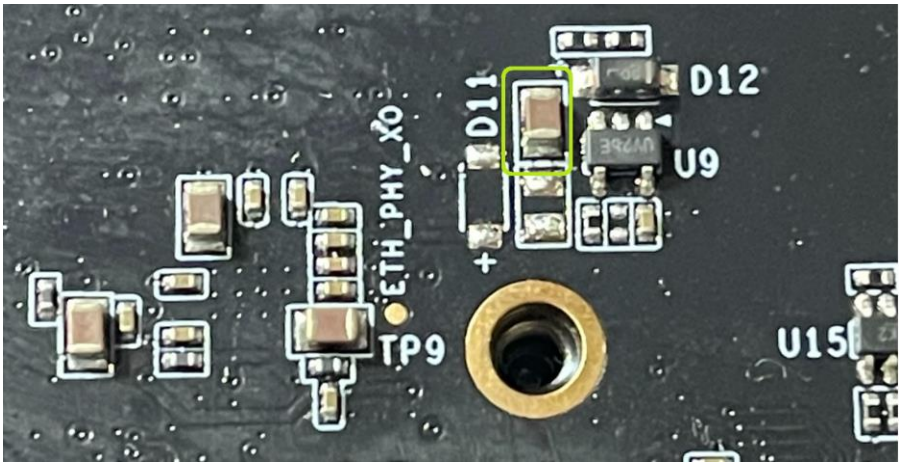
Applications Affected – Designs implementing Ethernet.

Description – There appears to be a reliability issue with the Ethernet during reset. In the cases where the Ethernet reliability issue occurs, software may not properly detect the Ethernet PHY.

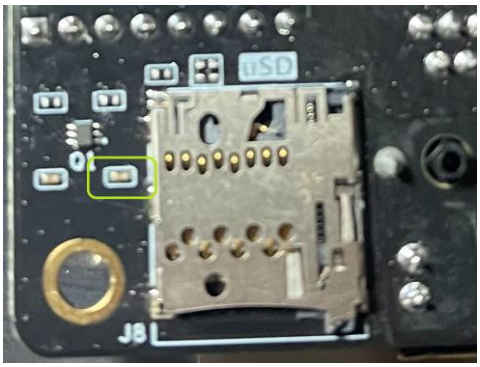
Workaround – To overcome the reliability issues with Ethernet, there are a couple of recommendations. First, it has been found that removing capacitors C12 and C51 from the K24 IO Carrier Card yielded a more reliable Ethernet reset signal.



Capacitors to Remove



C51 Location on Board Bottom Side – Green Box



C12 Location on Board Bottom Side – Green Box

If user is not comfortable or capable of making the modifications to remove the two capacitors from the printed circuit board, they should contact customize@avnet.com to get the board repaired. Please reference Ethernet Capacitor Removal for K24 Development Kit.

Also, there is software control of the Ethernet Reset that is required to be generated. Depending on the implementation of Ethernet, the user can provide software control to the Ethernet reset signal by utilizing the MIO12_ETH_RST_N signal that is attached to the processor via GPIO control of MIO Pin 12. MIO Pin 12 maps to the K24 System-On-Module to physical pin K20:

PACKAGE_PIN K20 - MIO12_FWUEN_C2M_L - Bank 500 - PS_MIO12

For Linux applications using the KSZ9131 PHY drivers, a reset pin can be added as follows in the device tree (DTS):

```
--- a/recipes-bsp/device-tree/files/k24-iocc/system-bsp.dtsi
+++ b/recipes-bsp/device-tree/files/k24-iocc/system-bsp.dtsi
@@ -31,12 +31,23 @@
    nvmem-cells = <&mac_address>;
    nvmem-cell-names = "mac-address";
    phy-handle = <&phy0>;
-   phy0: phy@7 {
-      reg = <0x7>;
-      ti,rx-internal-delay = <0x5>;
-      ti,tx-internal-delay = <0x5>;
-      ti,fifo-depth = <0x1>;
+   mdio {
+       compatible = "snps,dwmac-mdio";
+       #address-cells = <1>;
+       #size-cells = <0>;
+       phy0: phy@7 {
+               compatible = "ethernet-phy-id0022.1642",
+                                       "ethernet-phy-ieee802.3-c22";
+               reg = <7>;
+               eee-broken-100tx;
+               eee-broken-1000t;
+              reset-assert-us = <1000>;
+              /* RESET_N signal rise time ~100ms */
+              reset-deassert-us = <120000>;
+              reset-gpios = <&gpio 12 GPIO_ACTIVE_LOW>;
+       };
    };
+
 };

 /* QSPI partitions are defined with petalinux-config and described in system.conf.dtsi */
(END)
```

Ethernet PHY DTS Settings for KSZ9131 PHY

With the two capacitors removed and the reset pin added for software control of the Ethernet reset it is found that the Ethernet interfaces functions in a reliable fashion.

Examples of the Ethernet reset will be captured in an upcoming BSP release.

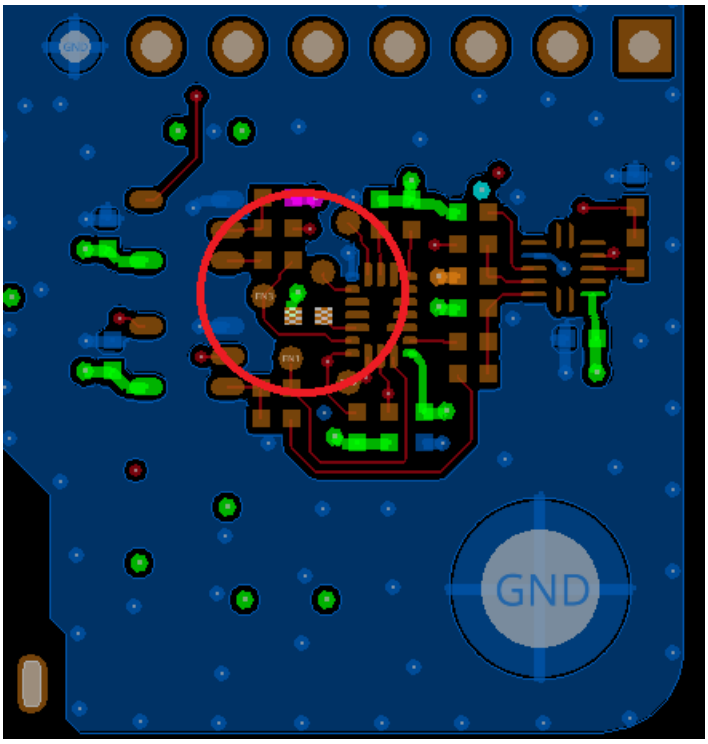
Board Power Down Via Button

Applications Affected – Any requiring board to be powered down via push button PB7

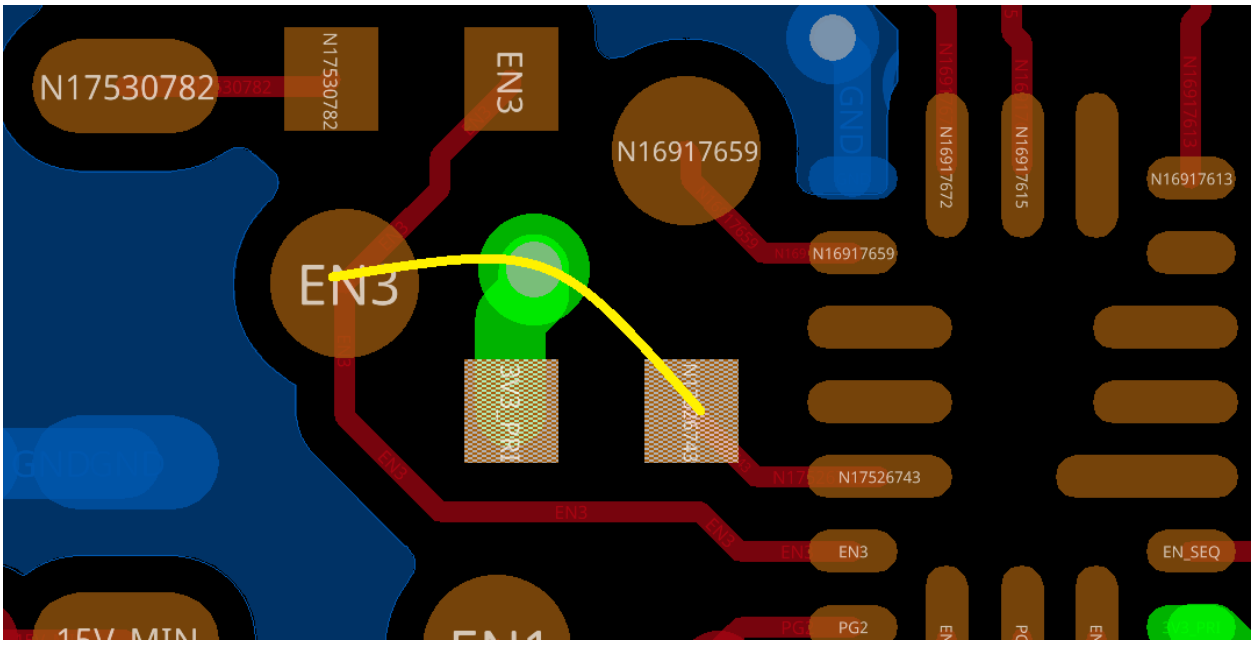
Description – There is an issue with the implementation of the on/off sequencer U22 (SLG7TD43741VTR) that prevents the board from completing it's power down sequence following the long depress of push button PB7. This failure mode is indicated by the PG LED D26 remaining illuminated no matter how long push button PB7 is depressed.

Workaround – A user can power-off the board by removing the power supply Type-C Cable from jack J11.

Physical Workaround - To get the proper power down functionality, resistor R334 needs to be removed and a wire needs to be added from TP44 (EN3) to R334 signal pad. In essence this shorts EN3 to PG3 on U22.



R334 Location on Board Bottom Side – Red Circle



Wire from TP44 (EN3 Test point) and R334 Signal Pad on Board Bottom Side – Yellow Line

New Errata:

If new errata are discovered it will be posted to the K24 Development Kit product page, under the Technical Documents tab: http://avnet.me/K24-DK

Additional Support:

For additional support, please review the discussions and post your questions in the K24 Development Kit Forum located here: http://avnet.me/K24-DK-forum

Alternatively, you can also reach out to your local Avnet Field Application Engineer (FAE) for support.

Revision History:

Date	Version	Revision
6-Jan-25	1.0	Initial Release