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LFPAK MOSFET thermal resistance - simulation, test and optimization of PCB layout

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application note

Document information

Information	Content
Keywords	thermal resistance, LFPAK
Abstract	This application note explains the parameter thermal resistance from junction to ambient and how it can be reduced by careful PCB layout.

1. Introduction

Nexperia MOSFET data sheets contain a parameter $R_{th(j-a)}$ which is the thermal resistance from junction to ambient. This is a guide to how much heat can be dissipated from the device to its surroundings in a typical application. For a surface-mounted device such as an LFPACK MOSFET this is highly dependent on the type of Printed Circuit Board (PCB) on which it is mounted. The type of material, the thickness of copper and the shape of the copper footprint all contribute to $R_{th(j-a)}$.

This application note looks at the structure of an LFPACK MOSFET and the way it is mounted on a PCB. It uses thermal modelling techniques to analyse how heat, generated inside the device, is transferred to its surroundings. Various circuit layouts are considered and tested so that developers can use a value for $R_{th(j-a)}$ that closely reflects practical applications.

2. Definition of thermal resistance $R_{th(j-a)}$

$R_{th(j-a)}$ is the thermal resistance from the active surface of the silicon crystal to the surrounding environment. It is a value that represents the net effect of all the possible series and parallel paths from the semiconductor junction to ambient and includes heat transfer by means such as conduction, convection and radiation.

$R_{th(j-a)}$ is defined as the temperature difference between junction and ambient that transfers one watt of power to the environment. It is given by:

$$R_{th(j-a)} = \frac{T_j - T_a}{P} \quad (1)$$

where $R_{th(j-a)}$ is measured in K/W

T_j is the junction temperature (°C)

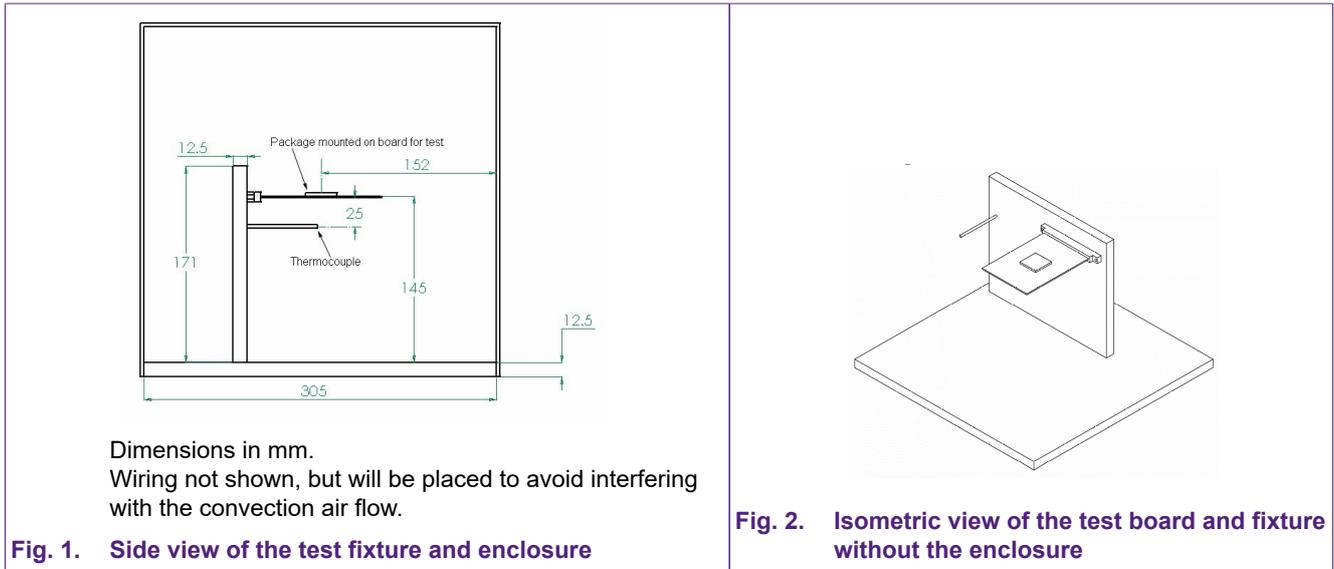
T_{amb} is the ambient temperature (°C)

P is the heating power dissipated inside the MOSFET (W)

2.1. Test method

The method used to measure $R_{th(j-a)}$ is defined by JEDEC standard 51-1 and 51-2A. The approach is a static implementation, meaning heating power is applied on continuous basis while monitoring the junction temperature. The formula for $R_{th(j-a)}$ shown above can be used once a known power is applied and steady state is reached. The Device Under Test (DUT) is soldered to a FR4 test board and placed in the geometric centre of the test enclosure as shown in [Fig. 1](#) and [Fig. 2](#). The enclosure comprises a 305 mm cube made from low thermal conductivity materials such as cardboard, polycarbonate, polypropylene, wood, etc.

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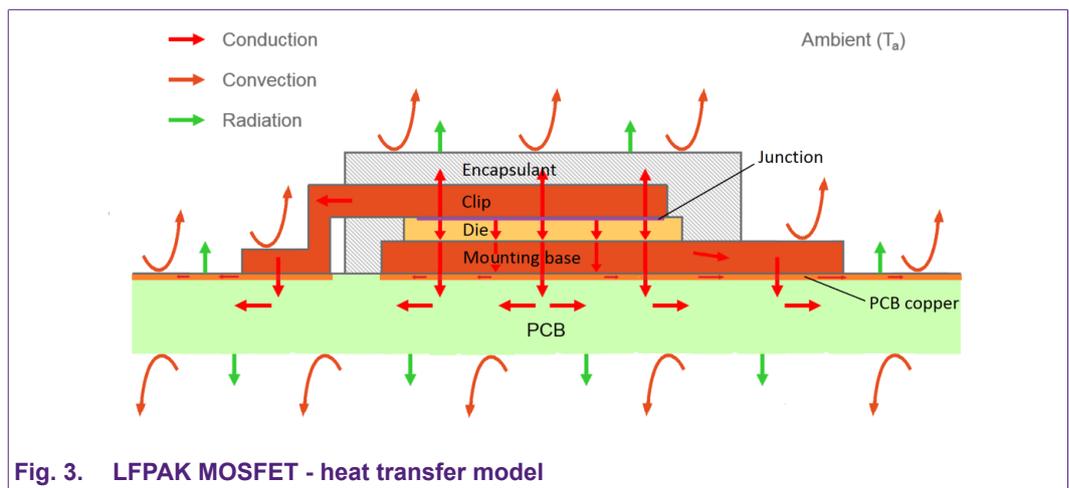
2.2. Heat transfer in the JEDEC enclosure

Within the JEDEC enclosure, heat is transferred from the DUT to the PCB and surroundings by three basic mechanisms; conduction, convection, and radiation.

Conduction is the process by which heat transfers from high temperature regions to low temperature regions that are in contact with each other. Fig. 3 shows how heat is transferred from the semiconductor junction to the copper clip and from the clip to the encapsulant. Also, from the junction through the silicon die to the mounting base, and from the mounting base to the PCB.

Convection refers to the heat transfer process caused by displacement of air surrounding the test fixture. The movement is caused by the tendency of hotter and therefore less dense air to rise, and colder, denser air to sink under the influence of gravity, which consequently results in transfer of heat.

Radiation does not depend on contact as heat conduction and convection do. Thermal radiation is when an object loses energy in the form of electromagnetic radiation in the infrared part of the spectrum. In the example shown in Fig. 3, heat is radiated from the surfaces of the MOSFET and the PCB into the space inside the box.



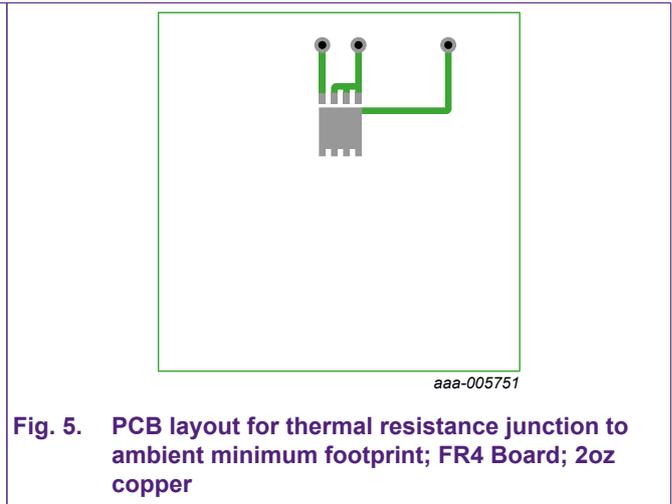
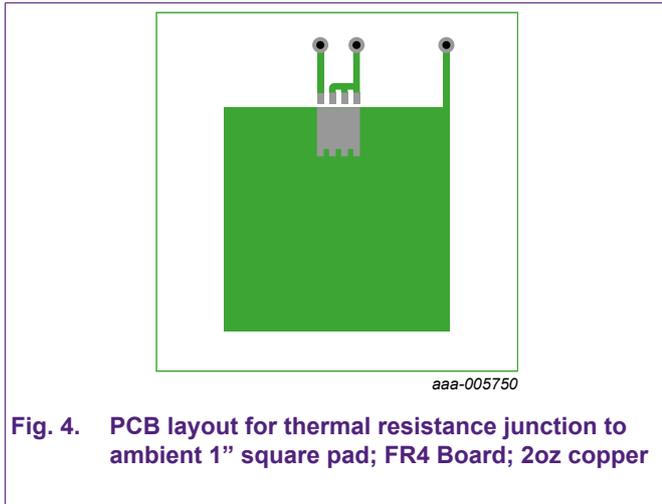
The measured thermal resistance of a MOSFET, $R_{th(j-a)}$, depends upon the package size, the material properties and the internal structure of the device. It also depends on the PCB that is used in the test fixture. Modern surface-mount MOSFETs are designed to use the PCB as a heat sink and rely on the copper traces to spread the heat over a large area to assist with cooling.

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Nexperia power MOSFET data sheets usually specify two values for $R_{th(j-a)}$ – one with a minimum footprint that conforms with the JEDEC standard, and another with a 25.4 mm (1") square of 70 μm thick (2 oz) copper on the top surface. See [Table 1](#) also [Fig. 4](#) and [Fig. 5](#) below.

Table 1. Thermal characteristics

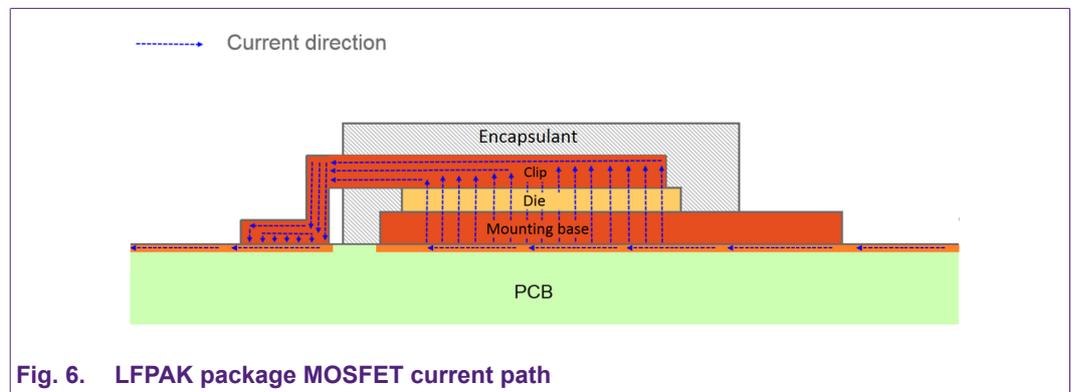
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 4	-	50	-	K/W
		Fig. 5	-	125	-	K/W



3. MOSFET drain-source current path

Modern power MOSFETs have an on-state resistance in the order of milliohms and surface-mount variants are capable of switching hundreds of amps. In these cases consideration must be given to the Joule heating effect, i.e. induced heat due to current flowing through the conductor, in this case current through the device and the PCB traces.

[Fig. 6](#), below, shows the current path through a LFPAK MOSFET. The clip is attached directly to the semiconductor junction and at low current it acts as a heat sink, conducting heat away from the junction to the PCB. At high current, however, it becomes heated by its own resistance and requires cooling by being connected to a cooling surface connected to the source terminal.



4. PCB layout optimization

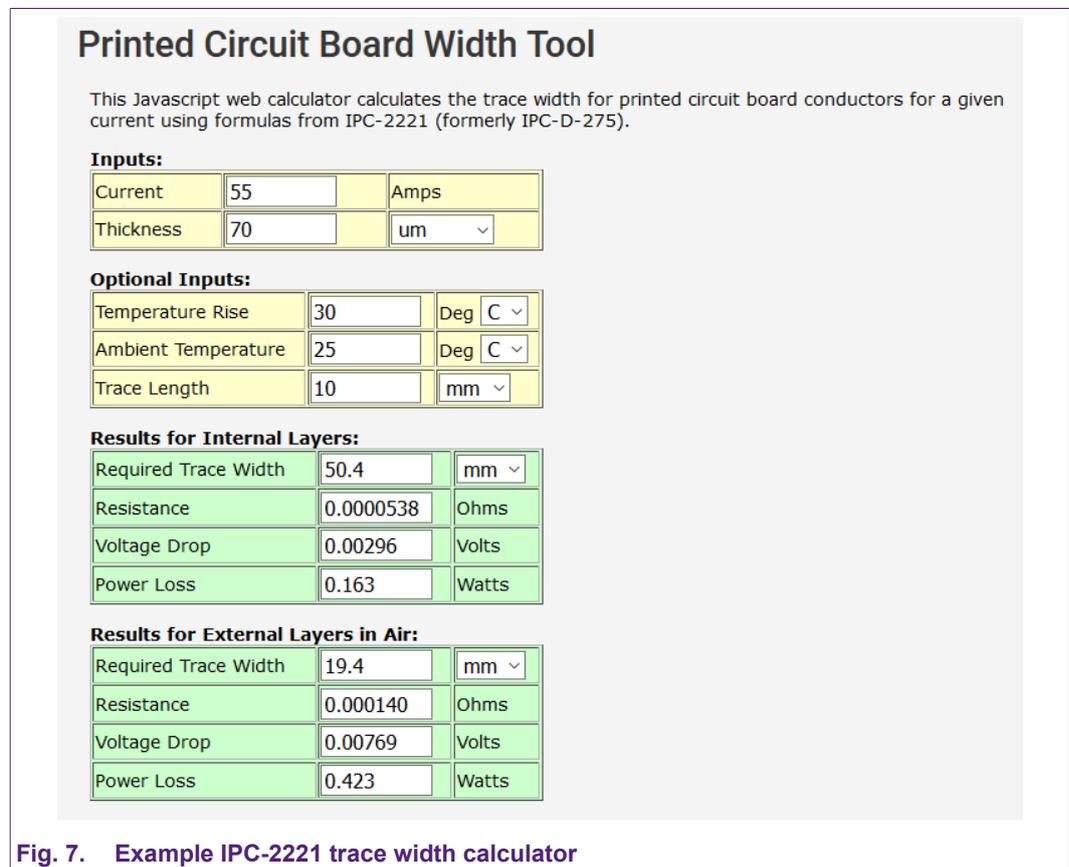
4.1. PCB trace width calculation

To examine the heating effect of the PCB trace let us consider as an example a Nexperia LFPK MOSFET; PSMN1R0-30YLD. This has an on-state resistance $R_{DSon} = 1 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$).

At a typical current of 55 A, the simplified power dissipation, given by I^2R will be $55^2 \times 0.001 = 3 \text{ W}$. This power can be dissipated with the appropriate PCB layout applying the right amount of copper to spread the heat.

Many PCB manufacturers websites include a trace width calculation tool based on the IPC-2221 Generic Standard on Printed Board Design. Using an IPC-2221 trace width calculator we can determine the size of trace required to carry 55 A.

Assuming 70 μm (2 oz) thick copper and allowing for manageable 30 $^\circ\text{C}$ rise in the trace temperature, [Fig. 7](#) shows that a trace almost 20 mm wide is required.



4.2. PCB layout simulations

A number of thermal simulations have been carried out using a PSMN1R0-30YLD as an example to find the optimum PCB layout that extracts the maximum amount of heat from the device and therefore gives the lowest possible value for $R_{th(j-a)}$. All the simulations were on a 25.4 mm square of 70 μm thick copper. The MOSFET was fully turned on with a constant current that produced a 3 W power loss in the device.

The investigation examined different positions of the MOSFET within the copper square. It also considered allocating different percentages of the copper square to the source and drain.

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Finally, it examined the heating effect of trace width on the temperature of the MOSFET and the consequences for $R_{th(j-a)}$ measurement.

Test layout 1

In [Fig. 8](#) the device is mounted on the edge of a 25.4 mm square copper pad.

$R_{th(j-a)} = 41.8 \text{ K/W}$ according to the simulation result.

This layout assumes that the main heat transfer path is from the junction, through the silicon die to the mounting base. All of the copper pad is allocated to cooling the mounting base. We see from the thermal profile that very little heat reaches parts of the copper furthest away from the MOSFET and these contribute little to the cooling. The source trace is very hot because of inefficient cooling of the source pins. This is evidently not an optimum solution resulting in a relatively high value for $R_{th(j-a)}$.

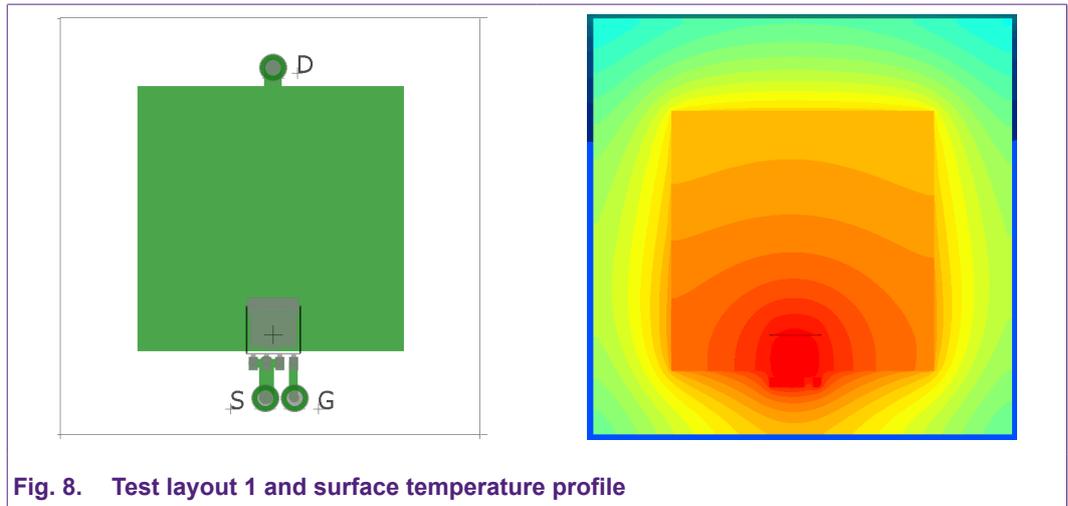


Fig. 8. Test layout 1 and surface temperature profile

Test layout 2

The test layout of [Fig. 9](#) shows the MOSFET mounted in the middle of the 25.4 mm copper square with the copper area divided equally between source and drain.

The simulation result gives: $R_{th(j-a)} = 39.1 \text{ K/W}$

Placing the device in the middle of the copper has improved the cooling and reduced the thermal resistance. However, the copper area connected to the drain tab is hotter than that connected to the source pins which suggest that more heat flows through the drain tab. Selecting the proper ratio of source to drain copper is important to obtain the optimum $R_{th(j-a)}$ value.

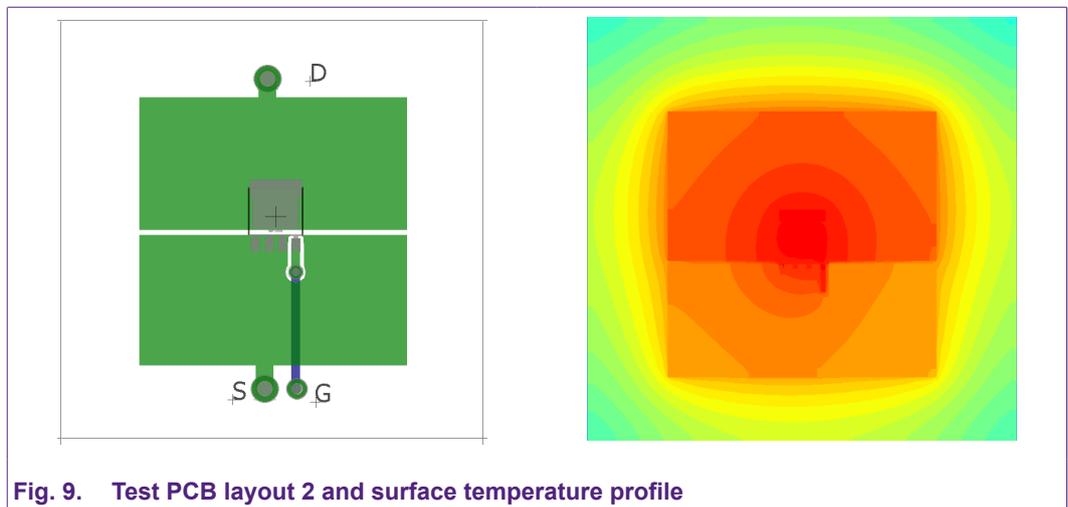


Fig. 9. Test PCB layout 2 and surface temperature profile

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Test layouts 3, 4 and 5

In [Fig. 10](#), [Fig. 11](#) and [Fig. 12](#) different layouts examine the effect of various trace widths for the source connection.

Layout 3 has the MOSFET located in the centre of the copper pad and the Joule heating effect of the source trace is not considered

The simulated result gives: $R_{th(j-a)} = 38.6 \text{ K/W}$.

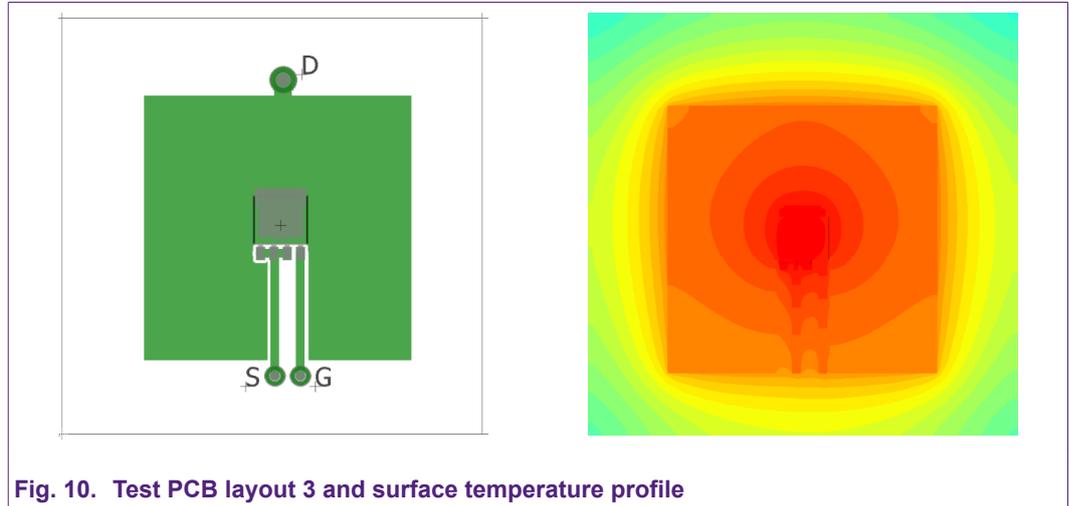


Fig. 10. Test PCB layout 3 and surface temperature profile

However in a practical working circuit when low R_{DSon} MOSFETs are fitted, the drain-source current can reach tens or even hundreds of amperes, and the heat generated in the PCB traces cannot be neglected.

Layout 4 shows what happens when the Joule heating of the source trace is taken into account. In this case the trace width is 0.8 mm. The power loss in the MOSFET is 3 W as before, but the power loss in the trace is 8.8 W. [Fig. 11](#) shows the rise in temperature of the source trace which is higher than the die temperature of the MOSFET and is therefore heated significantly.

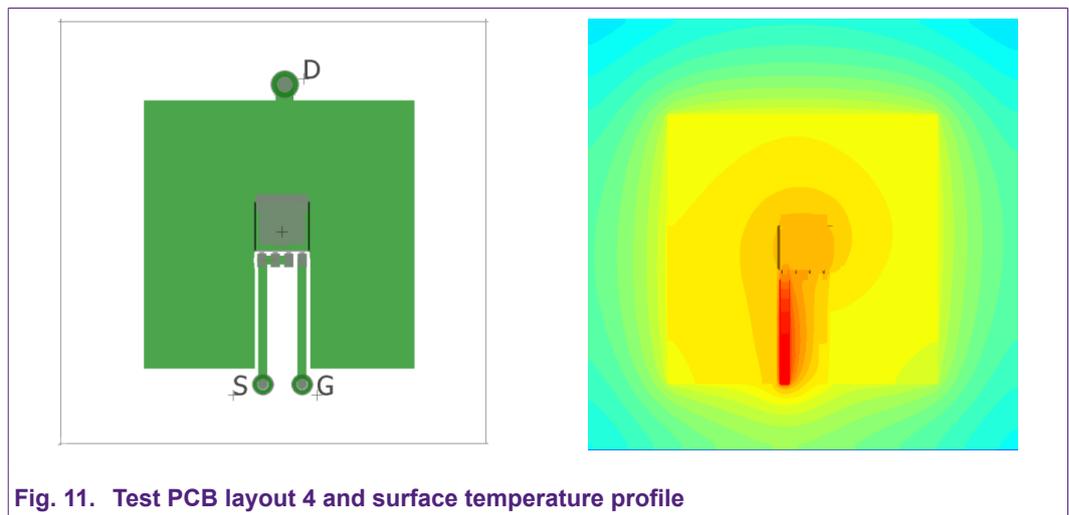


Fig. 11. Test PCB layout 4 and surface temperature profile

Layout 5 has the source trace increased to 3 mm. The test conditions are the same as in layout 4. This time the power loss in the source trace is reduced to 2.4 W but [Fig. 12](#) shows that the temperature still exceeds that of the die.

The simulated result gives: $R_{th(j-a)} = 56.7 \text{ K/W}$.

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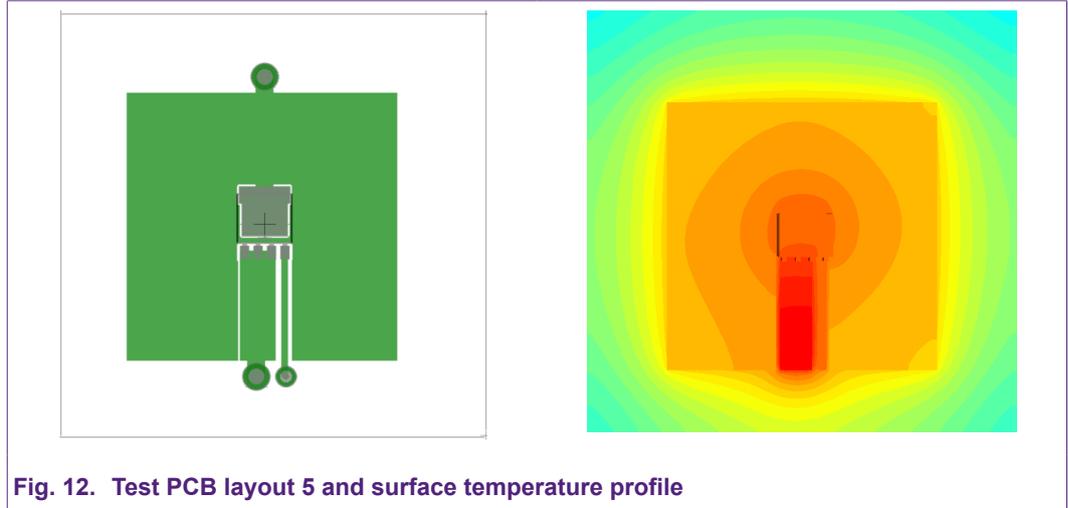


Fig. 12. Test PCB layout 5 and surface temperature profile

We can deduce from test layouts 4 and 5 that in a practical application involving an LFPACK MOSFET careful consideration must be given to trace thickness and width so that the Joule heating of the current path does not contribute to the heating of the MOSFET.

Optimal PCB layout - layout 6

Layout 6, shown in Fig. 13, attempts to optimise the copper traces to obtain the lowest possible $R_{th(j-a)}$. Approximately 1/3 of the 25.4 mm copper pad is allocated to the source pins whilst the width of the source trace is a maximum.

The simulation result gives: $R_{th(j-a)} = 37.1 \text{ K/W}$.

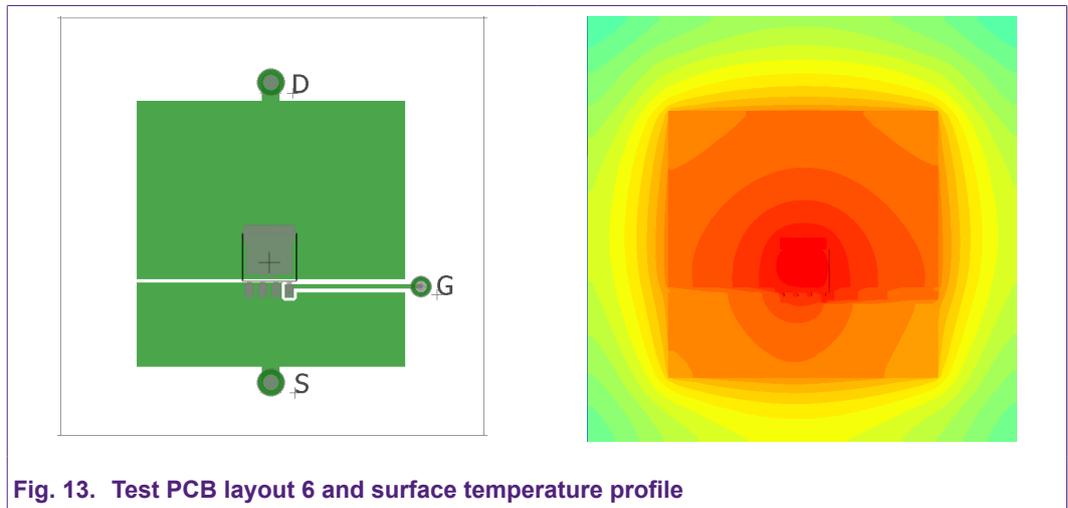


Fig. 13. Test PCB layout 6 and surface temperature profile

5. Conclusion

NEXPERIA LFPAC MOSFETs are designed to handle high levels of current, 300 A in the case of PSMN1R0-30YLD and in excess of 400 A for packages such as LFPAC88. To take full advantage of the MOSFET's ability to handle these levels of current, designers are faced with the challenge of dissipating the resulting power through the PCB and therefore care must be taken in the design of the layout.

A larger amount of copper and a larger area used under the MOSFET's drain tab will provide better thermal performance and thus better power dissipation. Perhaps less obvious is the PCB layout/trace for source pins and the importance of the amount/area of copper used. LFPAC packages provide a good thermal path from the junction to the source pins as they use one piece copper-clip (i.e. not two pieces of copper soldered together or copper-ribbon combination). It is therefore very important, for an efficient thermal design to consider a layout with the right amount and area of copper for the source pins.

As shown in this application note the best $R_{th(j-a)}$ can be achieved when this layout approach is applied. Another important factor to consider is the width and thickness necessary for PCB traces providing the electrical connections to the MOSFETs, in order to handle the high currents.

6. Revision history

Table 2. Revision history

Revision number	Date	Description
1.0	20200720	Initial version.

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