MICROCHIP

PolarFire® SoC FPGAs

Architecture, Applications, Security Features, Design Environment, Design Hardware

Microchip extends its leadership in low-power FPGAs and SoC FPGAs with the cost-optimized PolarFire® SoC family. PolarFire SoC FPGAs deliver up to 50% lower power than equivalent SRAM SoC FPGAs. PolarFire SoC is built upon the award winning, non-volatile PolarFire FPGA platform and features a five-core Linux® capable processor subsystem based on the RISC-V ISA.

The RISC-V CPU micro-architecture implementation is a simple 5 stage, single issue, in-order pipeline that doesn't suffer from the Meltdown and Spectre exploits found in common out-of-order machines. All five CPU cores are coherent with the memory subsystem allowing a versatile mix of deterministic real time systems and Linux in a single multi-core CPU cluster.

With Secure Boot built-in, innovative Linux and real-time modes, a large Flexible L2 memory subsystem and a rich set of embedded peripherals, PolarFire SoC is ideally suited for secure, power-efficient compute in a wide range of applications within smart embedded vision, wireline access networks, cellular infrastructure, aerospace and defense, industrial automation, automotive and Internet of Things (IoT).

Addressing Key Market Opportunities

Communications

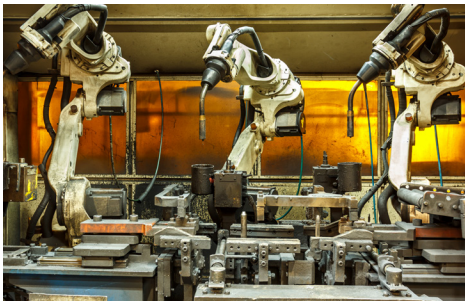
- Significantly improving network capacity and coverage with limited spectrum and CAPEX
- Growing IoT with minimal energy consumption
- Lowering physical and carbon footprint

Defense

- Providing battlefield portability and increased mission life
- Increasing automation in vehicles and weaponry
- Enhancing operator situational awareness
- Increasing cybersecurity
- Ensuring supply chain security

Industrial Automation

- Expanding factory automation networks
- Growing number of M2M sensors and nodes
- Securing decentralized computing
- Improving portability
- Achieving cyber security
- Improving functional safety



Smart Embedded Vision

- Delivering 4K video and smart imaging
- Applying AI/ML
- Applying imaging to portable products
- Extending battery life
- Eliminating thermal fans and heatsinks
- Achieving secure surveillance

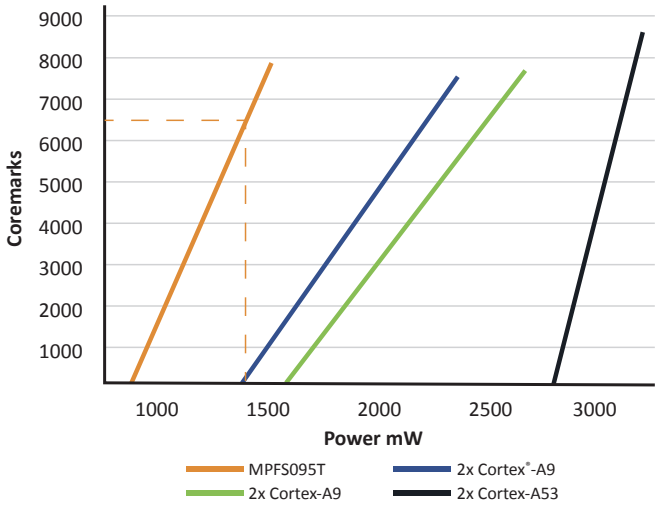
Automotive

- Delivering determinism to driver-assist systems
- Increasing vehicle automation
- Growing AI/ML implementations
- Lowering power consumption

Internet of Things

- Ensuring lowest power, most secure, edge and gateway devices
- Enabling data processing at the edge, distributed networking systems
- Increasing IoT automation and networking
- Delivering maximum performance with lowest carbon footprint

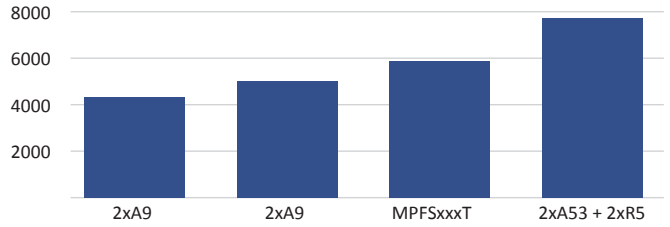
Lowest Power and Superior Performance



PolarFire SoC delivers significant power saving while outperforming SRAM based SoC FPGAs.

- PolarFire SoC offers
  - 6.5k Coremarks @ 1.3W while similar sized SRAM based SoC FPGAs deliver 0
  - Up to 60% lower power
  - More FPGA memory and DSP resources
- PolarFire SoC is the only mid-range SoC FPGA to offer
  - DDR3/4, LPDDR3/4 support
  - 12.7 Gbps transceivers
  - Cost efficient SGMII for GbE
  - 2× PCIe® Gen 2 (×1, ×2, ×4)
  - Smallest formfactor solutions starting from 11 mm × 11 mm in a FCSG325 package.

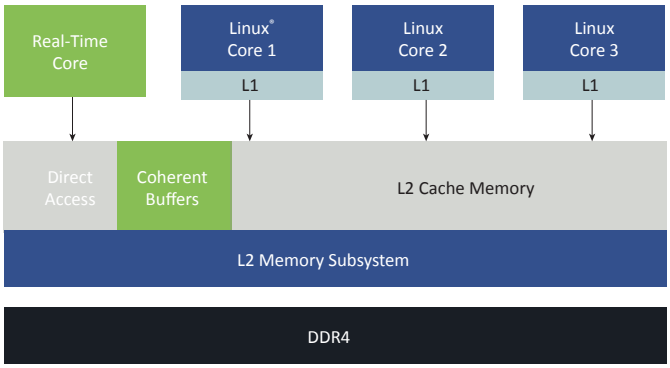
Microprocessor Subsystem Performance



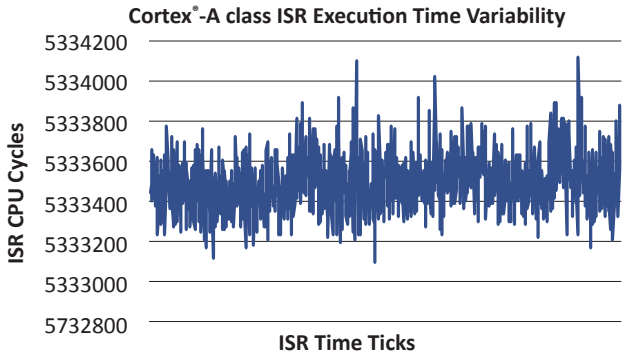
PolarFire SoC delivers more or similar total DMIPS compared to competitive SRAM based SoC FPGAs.

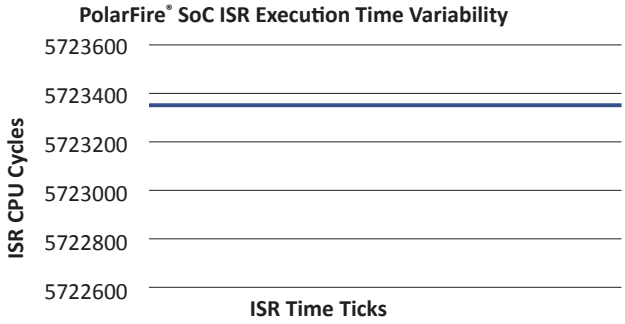
- Large 2 MB L2 Cache
  - Increases system performance for rich OS
  - Deterministic mode for real-time
- AMBA switch with built-in quality of service
- PolarFire SoC's RISC-V cores are configurable as an application processor or a real-time processor and delivers max performance in either configuration

Determinism (AMP Mode)



- L1 and L2 configurable as a deterministic memory
- Disable/enable branch predictors
- 5 stage in-order pipeline
- Run a rich OS and hard real-time in a coherent CPU cluster





Smallest Form Factors

PolarFire SoC FPGAs offer best-in-class form factors at 25k, 95k, 160k and 250k LEs.

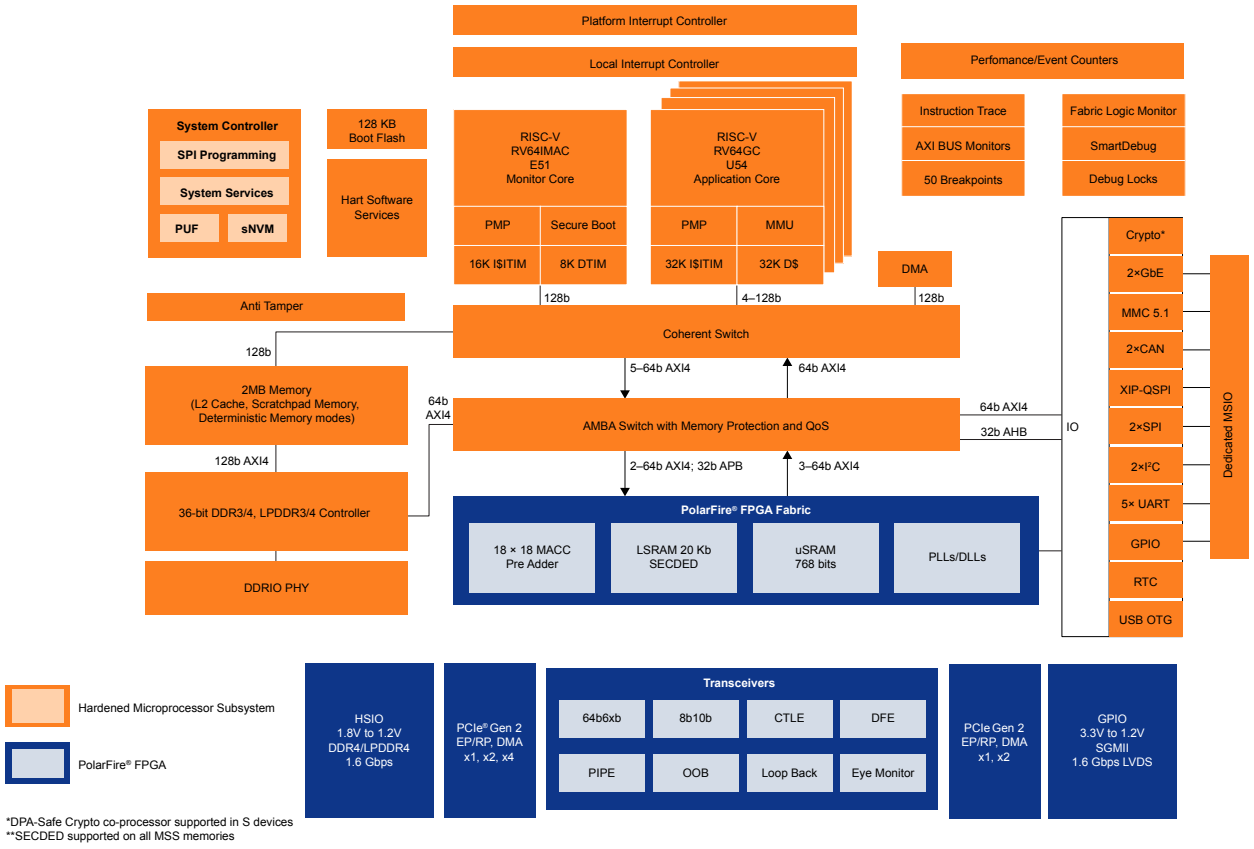
- **FCSG325:** 11 mm × 11 mm, Pitch 0.5 mm
- **FCSG325:** 11 mm × 14.5 mm, Pitch 0.5 mm
- **FCSG536:** 16 mm × 16 mm, Pitch 0.5 mm
- **FCVG484:** 19 mm × 19 mm, Pitch 0.8 mm
- **FCVG784:** 23 mm × 23 mm, Pitch 0.8 mm
- **FCG1152:** 35 mm × 35 mm, Pitch 1 mm

Mid-Range FPGA Platform Optimized for Low Power

- High-speed serial connectivity with built-in multi-gigabit/multi-protocol transceivers from 250 Mbps to 12.7 Gbps
- Up to 461k logic elements consisting of a 4-input Look-Up Table (LUT) with a fracture-able D-type flip-flop
- Up to 31.6 Mb of RAM
- Power optimized transceivers
- Up to 1420 18 × 18 multiply accumulate blocks with hardened pre-adders
- Integrated dual PCIe for up to ×4 Gen 2 Endpoint (EP) and Root Port (RP) designs
- High-Speed I/O (HSIO) supporting up to 1600 Mbps DDR4/LPDDR4, 1333 Mbps DDR3L, DDR3/LPDDR3 memories with integrated I/O gearing
- General Purpose I/O (GPIO) supporting 3.3V built-in CDR to support SGMII for serial gigabit Ethernet, and 1600 Mbps LVDS I/O speed with integrated I/O gearing logic
- Instant on, non-volatile technology offers 50% lower power vs. equivalent SRAM FPGAs
- Up to 50% lower power

Versatile, Low-Power Multi-Core RISC-V CPU Sub-System

- 64-bit multi-core CPU cluster
- Linux and real-time in a deterministic and coherent CPU cluster
- Integrated DDR3/4, LPDDR3/4 controller and phy
- Defense grade secure boot
- Spectre and meltdown immune
- Physically unclonable function
- Physical memory protection
- SECDED on all memories
- Low static power
- Low-power CPU cluster
- Smallest form factors 11 × 11, 16 × 16, 19 × 19



*DPA-Safe Crypto co-processor supported in S devices
**SECDED supported on all MSS memories

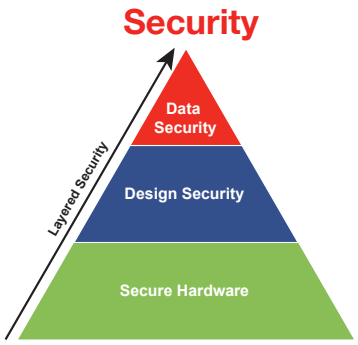
Cyber Security is the #1 Concern for Connected Devices on the Network Edge

It is not enough for today's demanding applications to meet the functional requirements of their design—they must do so in a secured way. Security starts during silicon manufacturing and continues through system deployment and operations. Microchip's PolarFire SoC FPGAs represent the industry's most advanced secure programmable FPGAs.

Security Features	PolarFire SoC	Competitor 1	Competitor 2	Competitor 3
TRNG	Hard-IP (SP800-90A CTR_DRBG-256; SP800-90B (draft) NRBG)	☒	☒	Soft-IP
AES	AES-128/192/256 (ECB, CBC, CTR, OFB, CFB, GCM, KeyWrap)	AES-256 (CBC)	AES-256 (CBC)	AES-256 (ECB, GCM)
SHA	SHA-1/224/256/384/512, Key Tree	SHA-256	SHA-256	SHA-384
HMAC	HMAC-SHA-1/224/256/384/512; GMAC-AES; CMAC-AES	HMAC-SHA2-256	HMAC-SHA2-256	☒
RSA	SigGen (ANSI X9.31, PKCS v1.5), SigVer (ANSI X9.31, PKCS v1.5)-1024/1536/2048/3072/4096	Soft-RSA –(2048) SigGen(PKCS v1.5), SigVer (PKCS v1.5)	Soft-RSA –(2048) SigGen(PKCS v1.5), SigVer (PKCS v1.5)	Software library - RSA primitive (2048)
ECDSA	KeyGen, KeyVer, SigGen & SigVer - NIST & Brainpool (P256/384/521) KAS - ECC CDH, PKG, PKV	☒	☒	☒
FFC	KAS - DH, DSA SigGen & SigVer (1024/1536/2048/3072/4096)	☒	☒	☒
Tamper Sense	Voltage, Temperature, Clock Frequency, Clock Glitch, Active Mesh	☒	☒	Only Voltage & Temperature
PUF	PUF protection for Secure Key storage (Secure Boot and Data communication)	☒	☒	For secure boot key
Bitstream Protection	DPA resistant Encrypted bit-stream programming	☒	☒	✓
DPA Resistance	DPA resistant hard crypto co-processor supporting all above Crypto algorithms	☒	☒	☒

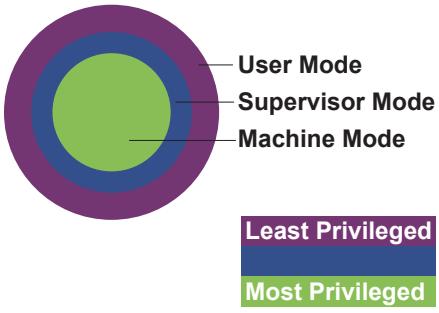
Defense Grade Security

- Secure Hardware
  - Secure wafer sort and packaging
  - Spectre and Meltdown immune CPUs
- Design security
  - DPA-resistant bitstream programming
  - Anti-tamper
  - DPA-resistant secure boot
- Data security
  - CRI DPA countermeasures pass through license
  - DPA-resistant crypto-coprocessor

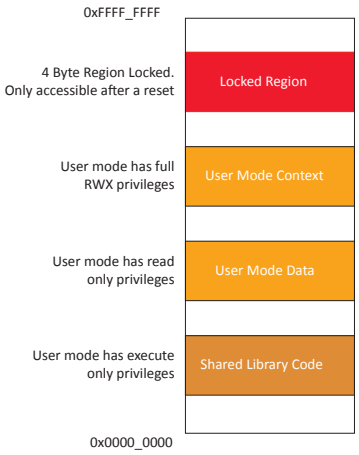


PolarFire SoC Physical Memory Protection

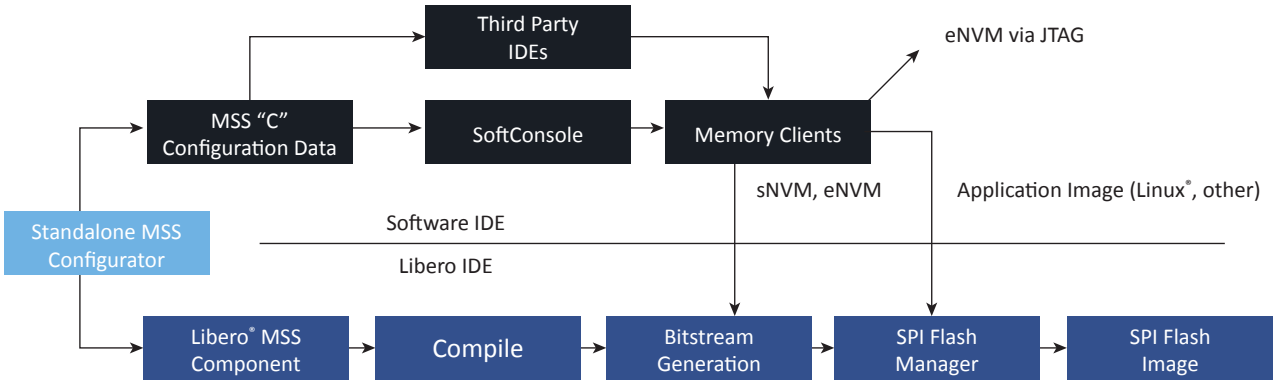
PolarFire SoC has Physical Memory Protection (PMP) implemented in each of the processor cores. PMP is used to enforce (read, write, execute) restrictions on less privileged modes. PolarFire SoC can restrict access rights of un-trusted user mode software.



PMP Implementation in PolarFire SoC



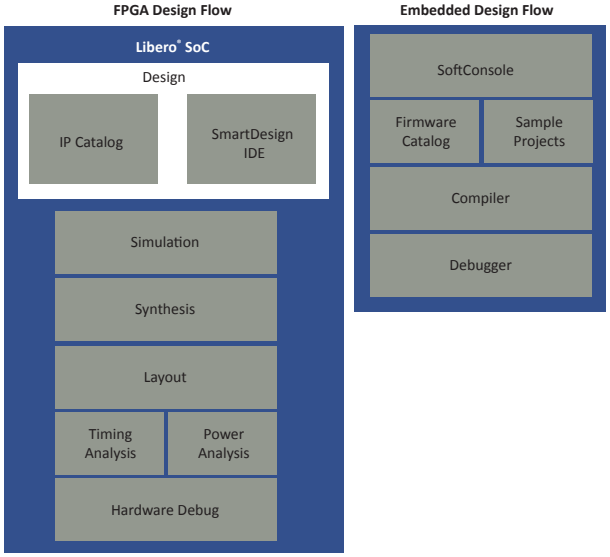
Design Flow and Tools



MSS Configurator

PolarFire SoC MSS Configurator is the tool to configure the processor subsystem and generate a Libero® component.

- Presets for SMP Linux, Real-time and AMP modes
- Generates C data structures to initialize the memory map for the embedded environment
- Generates a Libero MSS component for the FPGA design



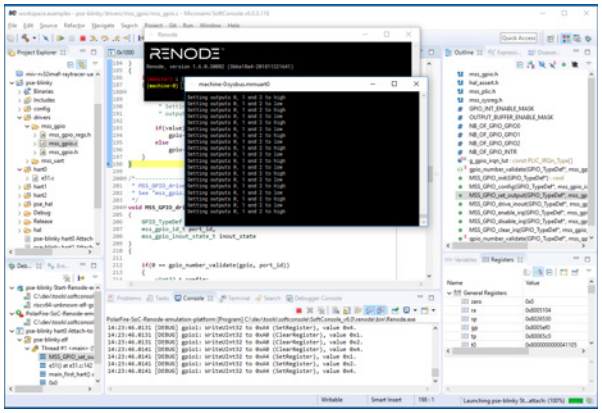
Libero SoC Design Suite

Microchip enhances design productivity by providing an extensive suite of proven and optimized IP cores for use with Microchip FPGAs and SoCs. Our extensive suite of IP cores covers all key markets and applications. Our cores are organized as either Microchip-developed DirectCores or third-party developed CompanionCores. Most Direct-Cores are available for free within the Libero SoC Design Suite and include common communications interfaces, peripherals, and processing elements.

SoftConsole

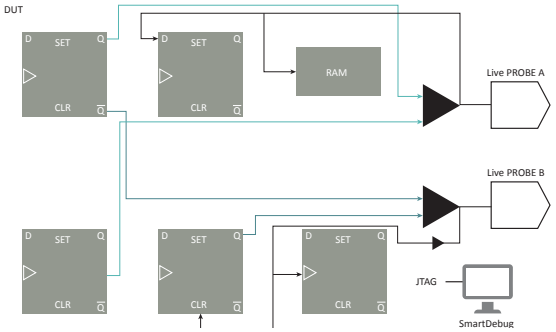
Microchip's SoftConsole is a free, Eclipse-based development environment for rapid development of bare-metal and RTOS based embedded firmware. SoftConsole supports development and debug for all Microchip FPGAs (with soft CPUs) and SoC FPGAs.

SoftConsole 6.x also integrates Antmicro's Renode emulation platform that supports Mi-V soft-CPUs and PolarFire SoC models.



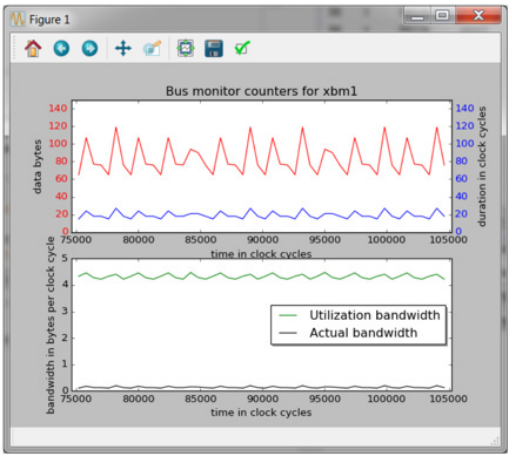
SmartDebug

SmartDebug offers the equivalent of an oscilloscope inside Microchip FPGAs and SoCs. SmartDebug features a tool called LiveProbes that enables an engineer to see any two nodes inside the FPGA, on external pins, without requiring recompilation of a design. Nodes can be quickly selected and modified, and the real-time signals can be seen externally immediately. This SmartDebug capability can cut debug time significantly. In addition, the SmartBERT module allows customers to configure and monitor the built-in PMA tester.



Trace, Bus Monitors and Software Debug

SoftConsole integrates an interactive GUI tool that provides a convenient and user-friendly way to configure debug modules, analyze trace and counter data, load and debug embedded software and view system state.



Trace

PolarFire SoC supports instruction trace for individual cores. Trace data support is available over Ethernet, JTAG and to the FPGA Fabric.

Dynamic AXI Bus Monitor

Dynamic AXI Bus Monitors can be used to monitor the traffic over an AXI bus, interpret bus protocol, identify transactions of interest using filters and initiate actions. PolarFire SoC supports Dynamic Bus Monitors that are passive and run-time configurable. Dynamic bus monitors are available on two AXI busses.

- The L2 cache bus monitor can be used to monitor the traffic to the L2 cache
- The AMBA switch bus monitor can be used to monitor traffic between the processor, fabric, peripherals and the DDR controller.

Performance Monitors

PolarFire SoC includes performance monitors that can be activated upon transaction events. The supported metrics include bus cycles, transactions, duration, bytes, beats, latency, hesitancy and bus concurrency. The performance monitors include:

- 2× 40-bit event counting CSRs
- 2× event selector CSRs
- Multiple event-selects per counter

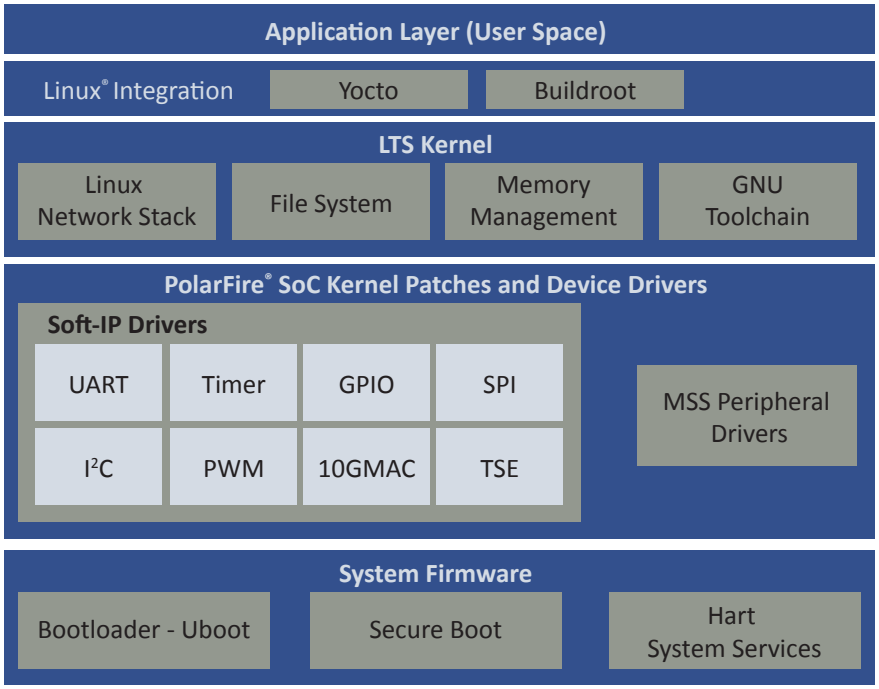
Machine Hardware Performance Monitor Event Register	
Instruction Commit Events, `mhpeventX[7:0] = 0`	
Bits	**Meaning**
8	Exception taken
9	Integer load instruction retired
10	Integer store instruction retired
11	Atomic memory operation retired
12	System instruction retired
13	Integer arithmetic instruction retired
14	Conditional branch retired
15	JAL instruction retired
16	JALR instruction retired
17	Integer multiplication instruction retired
18	Integer division instruction retired
19	Floating-point load instruction retired
20	Floating-point store instruction retired
21	Floating-point addition retired
22	Floating-point multiplication retired
23	Floating-point fused multiply-add retired
24	Floating-point division or square-root retired
25	Other floating-point instruction retired
Microarchitectural Events, `mhpeventX[7:0] = 1`	
Bits	**Meaning**
8	Load-use interlock
9	Long-latency interlock
10	CSR read interlock
11	Instruction cache/ITIM busy
12	Data cache/DTIM busy
13	Branch direction misprediction
14	Branch/jump target misprediction
15	Pipeline flush from CSR write
16	Pipeline flush from other event
17	Integer multiplication interlock
18	Floating-point interlock
Memory System Events, `mhpeventX[7:0] = 2`	
Bits	**Meaning**
8	Instruction cache miss
9	Data cache miss or memory-mapped I/O access
10	Data cache writeback
11	Instruction TLB miss
12	Data TLB miss

Software Debug

PolarFire SoC supports up to 10 hardware breakpoints/watchpoints per core with instruction and data address matches. SoftConsole's debug environment may be used for software debug.

Linux SDK

Microchip's PolarFire SoC's Linux SDK is available in Yocto and Buildroot environments. The SDK comes with support for system firmware that handles Secure system boot, Secure bootloader, Crypto services and inter-CPU messaging. The SDK includes driver support for all the Microprocessor sub-system peripherals and common Soft-IPs supported for the FPGA fabric.



PolarFire SoC Real-Time Operating Systems

Microchip extends support for various open-source and commercial Real-Time Operating Systems (RTOS) for PolarFire SoC. Users may choose to use Microchip's free eclipse based SoftConsole development environment or third-party environments to develop their baremetal/RTOS based embedded firmware. Open-source RTOS ports on PolarFire SoC are available as example projects. Commercial RTOSs that include advanced scheduling, memory management and file systems are available from corresponding vendors. The following open-source and commercial RTOS's have been ported on PolarFire SoC.

amazon freeRTOS

µC/OS™ RTOS and Stacks

NUCLEUS

VxWorks

THREADX

Zephyr™

Mi-V Ecosystem is Part of the Larger RISC-V Ecosystem Tailored for PolarFire SoC

Porting embedded applications can be a chore, after all no two SoCs are identical. The effort to port from one SoC to another is the same regardless of the underlying ISA. Linux abstracts the ISA away from the developer and our Yocto and BuildRoot projects help customers fork for their own projects. Mi-V Ecosystem consists of partners providing various solutions that can help you jumpstart your designs.

Operating Systems

yocto PROJECT

BuildRoot Making Embedded Linux Easy

FreeBSD

RTOS

amazon freeRTOS

µC/OS™ RTOS and Stacks

THREADX

VxWorks

NUCLEUS

Zephyr™

Compilers

AdaCore

GCC

IAR SYSTEMS

Green Hills® SOFTWARE

Mentor® A Siemens Business

Middleware

wolfSSL

0x5 HEX-Five

SECURE RF

Mi-V Design Partners and SoM Vendors

antmicro

aries embedded

DornerWorks

trenz electronic

SUNDANCE DSP INC

ENCLUSTRA FPGA SOLUTIONS

DIGITAL CORE TECHNOLOGIES QUALITY BY DESIGN

EMDALO TECHNOLOGIES Embedded Intelligent Systems

Features and Packaging Overview of the PolarFire SoC FPGA Family

Extended Commercial (0°C to 100°C) and Industrial (–40°C to 100°C) Temperature Support for all Die Package Combinations – RoHS only.

	Features	MPFS025T	MPFS095T	MPFS160T	MPFS250T	MPFS460T
FPGA Fabric	k Logic Elements (4LUT + DFF)	23	93	161	254	461
	Math Blocks (18 × 18 MACC)	68	292	498	784	1420
	LSRAM Blocks (20K bit)	84	308	520	812	1460
	uSRAM Blocks (64 × 12)	204	876	1494	2352	4260
	Total RAM Mbits	1.8	6.7	11.3	17.6	31.6
	uPROM Kbits	194	387	415	470	553
	User DLL's/PLL's	8 each	8 each	8 each	8 each	8 each
High Speed IO	250 Mbps to 12.5 Gbps SERDES Lanes	4	4	8	16	20
	PCIe Gen2 End Points/Root Ports	2	2	2	2	2
Total FPGA IO	HSIO+GPIO	108	276	312	372	468
Total MSS IO	MSS IO	136	136	136	136	136
MSS DDR	Data Bus	16	32	32	32	32
	Type (Size, Pitch)	MSS IO/HSIO/GPIO/XCVRs				
Packaging	FCSG325 (11 × 11, 11 × 14.5*, 0.5 mm)	102/32/48/2	102/32/48/2	102/32/48/2*		
	FCSG536 (16 × 16, 0.5 mm)		136/60/108/4	136/60/108/4	136/60/108/4	
	FCVG484 (19 × 19, 0.8 mm)	136/60/48/4	136/60/84/4	136/60/84/4	136/60/84/4	
	FCVG784 (23 × 23, 0.8 mm)		136/144/132/4	136/144/168/8	136/144/180/8	
	FCG1152 (35 × 35, 1.0 mm)				136/144/228/16	136/180/288/20

PolarFire SoC IP Portfolio

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PolarFire SoC Soft-IPs

- Bus Interface
  - AXI, AHB, AHBL, APB3, interconnects and bridges
- Memory interface
  - SRAM, QDR II+, DDR3, LPDDR3, DDR4, MMC
- Communication
  - JESD204BRX, JESD204BTX, RSDEC, RSENC, LiteFast, EDAC, CPRI v6.1, TCAM
- Security
  - DES, 3DES, Crypto and Tamper configurators
- DSP/Math
  - FIR, LNSQRT, DDS, Complex Multiplier, FFT, CIC
- Soft-CPUs
  - MiV_RV32IMAF_L1_AHB, MiV_RV32IMA_L1_AHB, MIV_RV32IMA_L1_AXI, JTAG, BootStrap
- Peripherals
  - PWM, PCS, UART, GPIO, I2C, MDIO, SPI, RMII, Timer, DMA, LSM, SmartBERT, Core429, SGMII, TSE, PCIF, 10GBASE-R, 10GBASE-KR, XAUI, USXGMII, 1553BRT, SDITX/RX (SD/HD/3G), UHD_SDITX/RX (6G/12G)

PolarFire SoC Imaging and Video IP

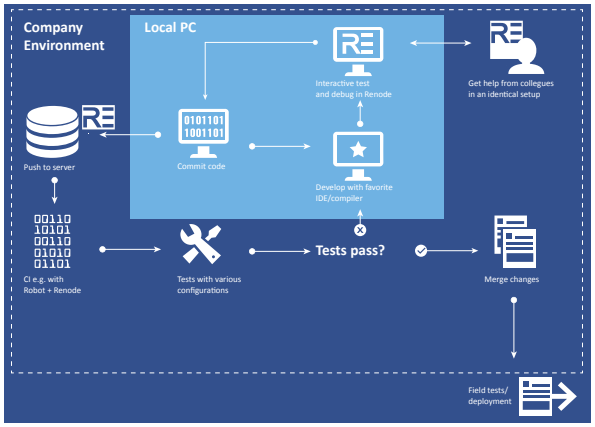
- Bayer conversion (4K resolution)
- Video DMA
- Video scalar (4K resolution)
- Alpha blending
- Color space (YCbCr, RGB)
- Image sharpening filter
- Display enhancement (brightness/contrast/hue)
- Image edge detection
- Display controller (4K resolution)
- Pattern generator
- MIPI CSI-2 receiver decoder
- (Up to 1.5 Gbps per lane ×4 lanes, 4Kp60)
- MIPI CSI-2 Tx
- (Up to 1 Gbps per lane ×4 lanes, 4Kp30)
- HDMI 2.0 (Rx 1080p60, Tx 4kp60)
- SLVS-EC (supports 2.3 Gbps per lane ×2 lanes in RAW8 data type)
- CoaXpress v1.1 (6.25 Gbps down, 20.83 Mbps up connections, host and device IP)

Renode PolarFire SoC Emulation Platform

Antmicro's Renode emulation platform is integrated within SoftConsole 6.x development environment and supports microchip's RISC-V based Mi-V soft CPUs and PolarFire SoC models.

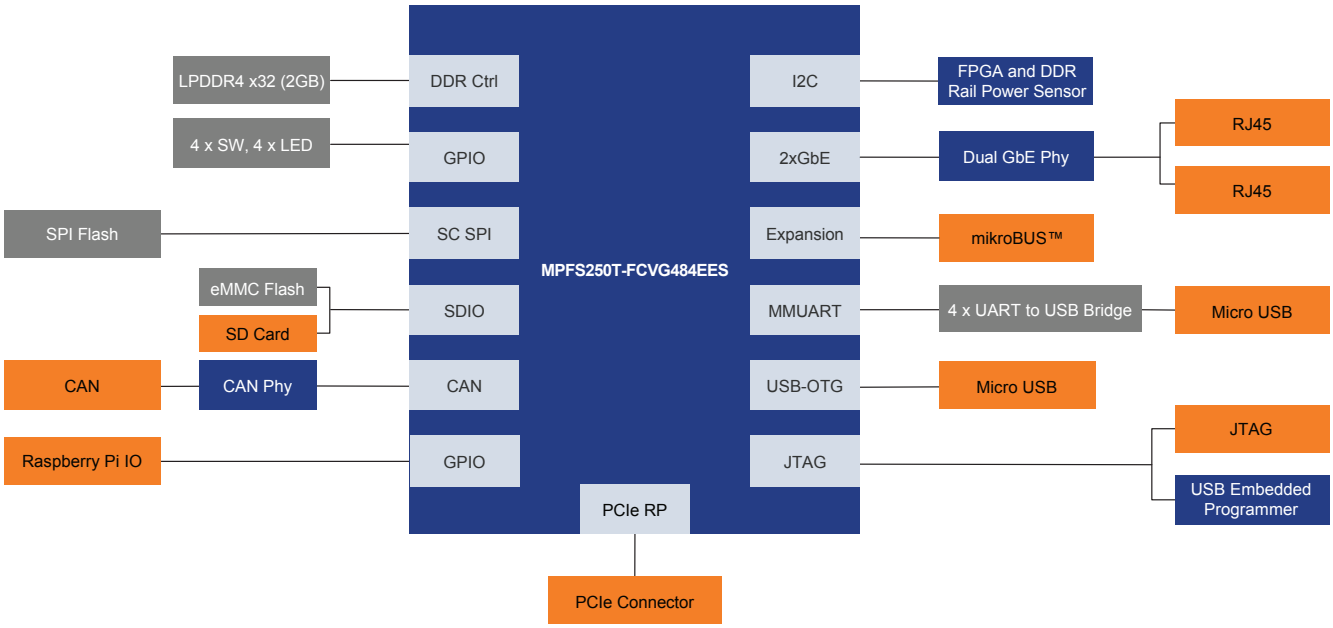
Renode is an opensource platform that offers

- A test-driven software development methodology
- Multiple connected virtual devices (multi-node) setups within the same simulated environment
- A high productive programming platform using C#
- Full visibility of simulated platform
- Unlimited integration and easy bundling



PolarFire SoC Icicle Kit Features (Part number MPFS-ICICLE-KIT-ES)

- PolarFire SoC MPFS250T-FCVG484EES
  - 254k LE non-volatile fabric
  - 784 – 18 × 18 math blocks
  - 5 – core RISC-V CPU subsystem (1xRV64IMAC, 4xRV64GC)
  - Secure boot
  - 4× 12.7 Gbps SERDES
  - FCVG484 package (19 × 19 mm, 0.8 mm pitch)
- Memory
  - LPDDR4 x 32
- Storage
  - QSPI Flash
  - eMMC Flash
- Connectivity
  - 2× GbE
- Expansion Ports
  - Raspberry Pi
  - mikroBUS™
- Interfaces
  - PCIe
  - USB 2.0
  - UART
  - SPI
  - I²C
  - CAN
- Sensor
  - Power sensor



Questions about PolarFire SoC, email PolarFireSoC@microchip.com

Support

Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit www.microchip.com:

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If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.

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