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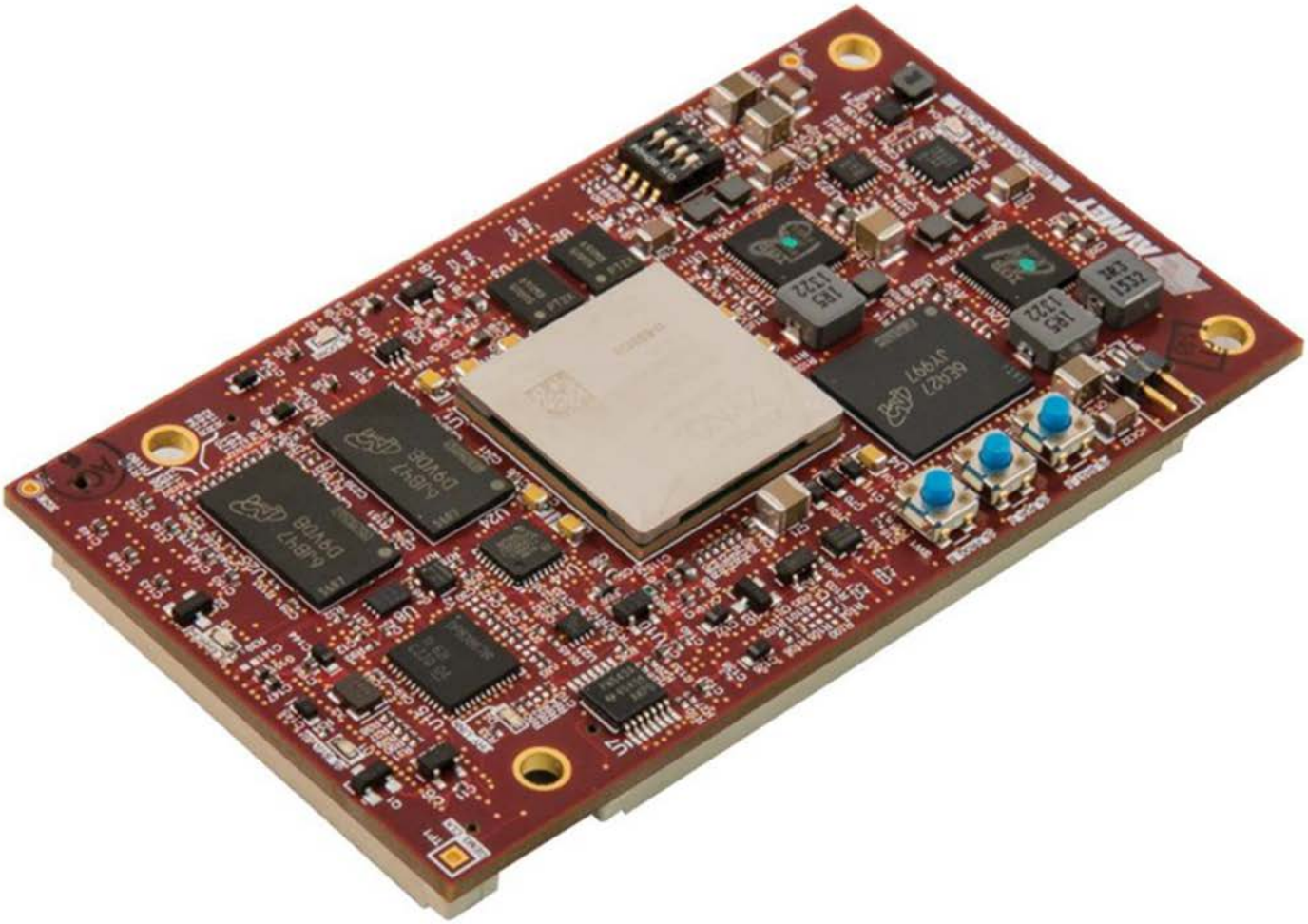

UltraZed™-EG SOM Hardware User Guide

Version 1.1

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1.0	12/7/2016	Initial Release
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Contents

1 Introduction

The UltraZed™-EG SOM (System-On Module) is a low cost System-On-Module targeted for broad use in many applications. The features provided by the UltraZed-EG System-On-Module consist of:

- Xilinx XCZU3EG-1SFVA625 MPSoC
  - Pin Compatible with the 2EG, 2CG, and 3CG MPSoC devices in the same package
  - Primary configuration Options = eMMC or QSPI Flash
  - Auxiliary primary configuration options via End User Carrier Card
    - JTAG
    - microSD Card
- Memory
  - DDR4 SDRAM (2GB, x32)
  - Dual QSPI Flash (64MB)
  - eMMC Flash (8GB, x8)
  - I2C EEPROM (2Kb)
- Interfaces
  - Gigabit Ethernet PHY (Connector required on End User Carrier Card)
  - USB 2.0 ULPI PHY (Connector required on End User Carrier Card)
  - One 100-pin JX Micro Header
  - Two 140-pin JX Micro Headers
  - I2C I/O Expander
  - Two Channel I2C Switch/MUX
- PS Reference Clock Input
  - 33.333 MHz OSC
- Power
  - On-Board 5-Output Voltage Regulators
  - Full Power Sequencing Pre-Programmed
  - Support for Zynq UltraScale+® PS Low Power Mode
  - Bank I/O Voltage Rails and GTR Transceiver Voltage Rails are powered from End User Carrier Card via JX Micro Headers
- Pertinent URLs
  - SOM: http://ultrazed.org/product/ultrazed-EG
  - Starter Kit: http://ultrazed.org/product/ultrazed-eg-starter-kit
  - Carrier Card: http://ultrazed.org/product/ultrazed-io-carrier-card

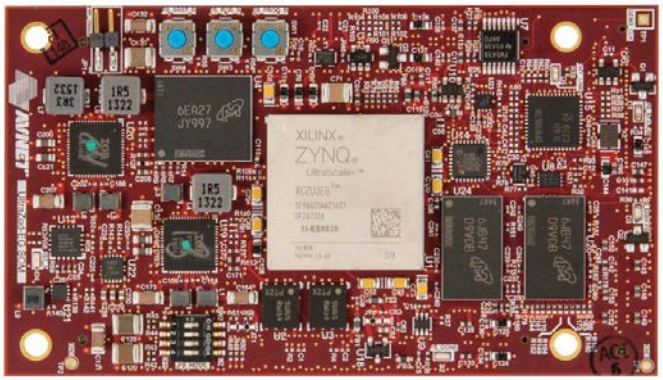


Figure 1 – UltraZed-EG SOM

The following figure is a high level block diagram of the UltraZed-EG SOM and the peripherals attached to the Zynq UltraScale+ MPSoC Processing Sub-System and Programmable Logic Sub-System.

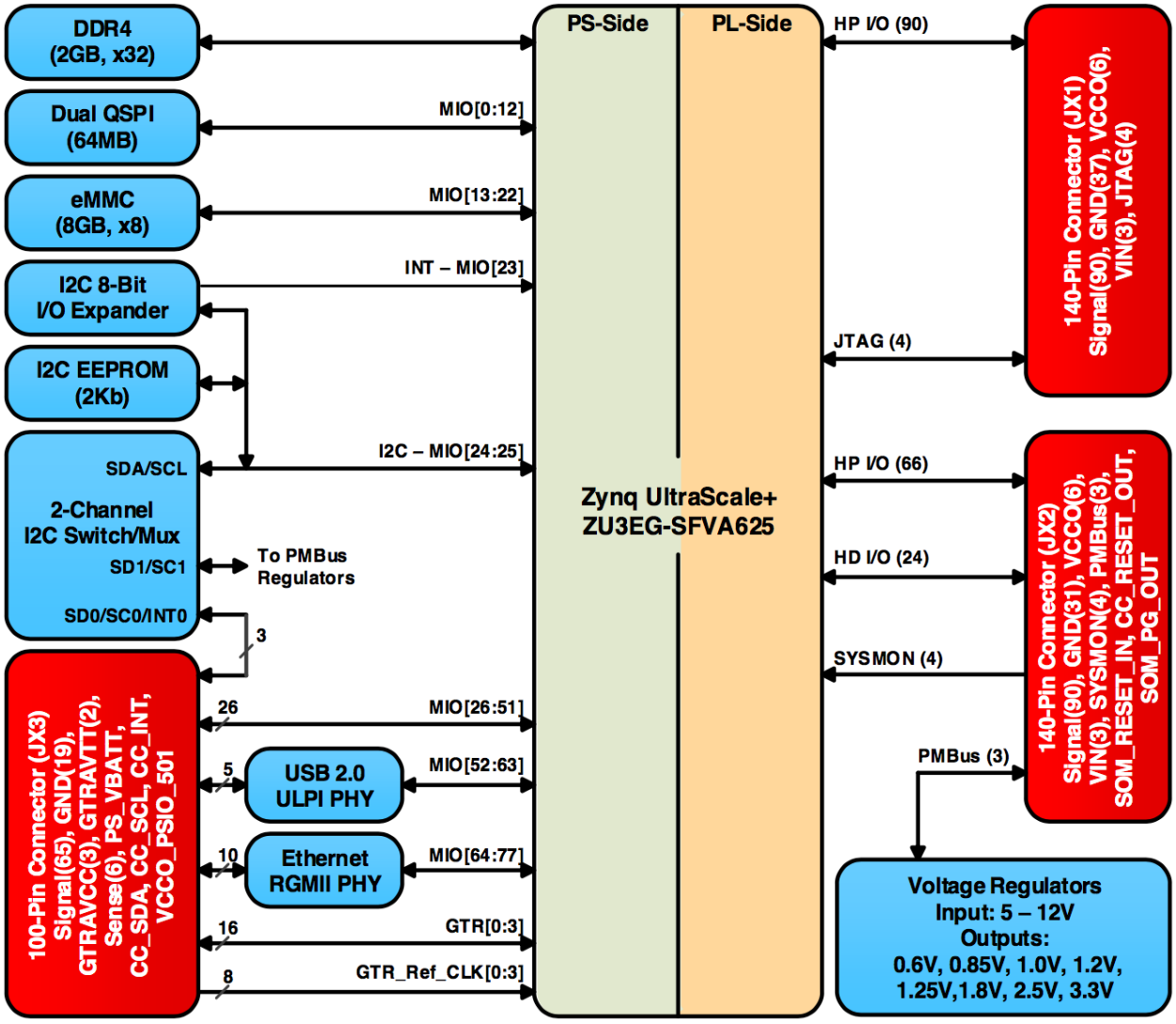


Figure 2 – UltraZed-EG SOM Block Diagram

2 Functional Description

2.1 Zynq UltraScale+ MPSoC

The UltraZed-EG SOM includes a Xilinx Zynq UltraScale+ MPSoC. The devices capable of being populated on the UltraZed-EG SOM are the XCZU2EG-1SFVA625 or XCZU3EG-1SFVA625 MPSoC. The UltraZed- EG SOM also supports the 2CG and 3CG MPSoC device as well as both extended and industrial temperature grade options as well as all of the speed grade options offered by Xilinx.

NOTE: Please contact your local Avnet FAE in regards to currently available options or custom device options for the UltraZed-EG SOM.

2.2 Memory

Zynq UltraScale+ contains a hardened PS memory interface unit. The memory interface unit includes a dynamic memory controller and static memory interface modules. The UltraZed-EG SOM takes advantage of these interfaces to provide system RAM as well as two different non-volatile memory sources.

2.2.1 DDR4

The UltraZed-EG SOM includes two Micron **MT40A512M16JY-083E IT:B** (96-pin BGA package) DDR4 memory components creating a 512M x 32-bit interface, totalling 2 GB of random access memory. The DDR4 memory is connected to the hard memory controller in the PS of the Zynq UltraScale+ MPSoC via its Bank 504 PS Memory Interface. The Bank 504 PS Memory Interface incorporates both the DDR controller and the associated PHY, including its own set of IOs.

Speeds of up to 2,133 Mbps for DDR4 is supported. The DDR4 interface is designed to use 1.2V SSTL-compatible inputs.

DDR4 Termination is utilized on the UltraZed-EG SOM and configured for fly-by routing topology. Additionally the board trace lengths are matched, compensating for the internal package flight times of the Zynq UltraScale+ MPSoC SFVA625 package, to meet the requirements listed in the Xilinx PCB Design and Pin Planning Guide (UG583).

All single-ended signals are routed with 50 ohm trace impedance. Differential signals are set to 90 ohms trace impedance. Several signals are terminated through 40 ohms resistors to +DDR4_VTT. Each DDR4 chip has its own 240-ohm pull-down on ZQ.

NOTE: +DDR4_VREF is not the same as +DDR4_VTT.

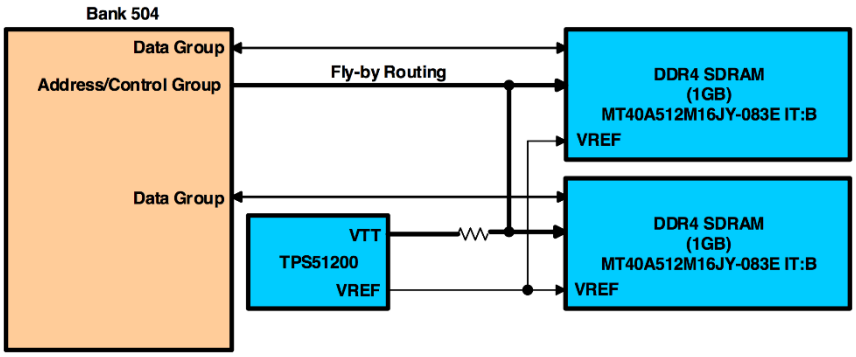


Figure 3 – DDR4 Block Diagram

Signal Name	Description	Bank 504 MPSoC Pin	DDR4 Pin
PS_DDR_A0	DDR Address Input	U25	P3
PS_DDR_A1	DDR Address Input	Y25	P7
PS_DDR_A2	DDR Address Input	AB25	R3
PS_DDR_A3	DDR Address Input	AA25	N7
PS_DDR_A4	DDR Address Input	V25	N3
PS_DDR_A5	DDR Address Input	AC25	P8
PS_DDR_A6	DDR Address Input	W21	P2
PS_DDR_A7	DDR Address Input	AB22	R8
PS_DDR_A8	DDR Address Input	Y20	R2
PS_DDR_A9	DDR Address Input	AA20	R7
PS_DDR_A10	DDR Address Input	AB23	M3
PS_DDR_A11	DDR Address Input	AD24	T2
PS_DDR_A12	DDR Address Input	AC23	M7
PS_DDR_A13	DDR Address Input	AE24	T8
PS_DDR_A14	DDR Address / RAS Input	AC24	L2
PS_DDR_A15	DDR Address / CAS Input	AD23	M8
PS_DDR_A16	DDR Address / WE_N Input	Y21	L8
PS_DDR_BA0	DDR Bank Address Inputs	W22	N2
PS_DDR_BA1	DDR Bank Address Inputs	V20	N8
PS_DDR_BG0	DDR Bank Group Address Inputs	V19	M2
PS_DDR_CKE0	DDR Clock Enable Input	T24	K2
PS_DDR_CK0_P	DDR Clock Device 0 Pair	AA23	K7
PS_DDR_CK0_N	DDR Clock Device 0 Pair	AA24	K8
PS_DDR_CS0_N	DDR Chip Select Input	T25	L7
PS_DDR_ACT_N	DDR Activate Command Input	V18	L3
PS_DDR_ALERT_N	DDR Alert Output	U23	P9
PS_DDR_ODT0	DDR On-Die Termination	V24	K3
PS_DDR_PARITY	DDR Command/Address Parity	V23	T3
PS_DDR_RAM_RST_N	DDR Active Low Reset Input	U21	P1
PS_DDR_ZQ	ZQ Calibration Reference	U22	F9
PS_DDR_DQ0	DDR Data Byte 0	AB15	U24-G2
PS_DDR_DQ1	DDR Data Byte 0	AE15	U24-F7
PS_DDR_DQ2	DDR Data Byte 0	AC15	U24-H3
PS_DDR_DQ3	DDR Data Byte 0	AE14	U24-H7
PS_DDR_DQ4	DDR Data Byte 0	AD13	U24-H2
PS_DDR_DQ5	DDR Data Byte 0	AC13	U24-H8
PS_DDR_DQ6	DDR Data Byte 0	AB13	U24-J3
PS_DDR_DQ7	DDR Data Byte 0	AA13	U24-J7
PS_DDR_DM0	DDR Data Byte 0 Data Mask	AA14	U24-E7
PS_DDR_DQS0_P	DDR Data Byte 0 Data Strobe Pair	AC14	U24-G3
PS_DDR_DQS0_N	DDR Data Byte 0 Data Strobe Pair	AD14	U24-F3
PS_DDR_DQ8	DDR Data Byte 1	AC16	U24-A3
PS_DDR_DQ9	DDR Data Byte 1	AB16	U24-B8
PS_DDR_DQ10	DDR Data Byte 1	AD16	U24-C3
PS_DDR_DQ11	DDR Data Byte 1	AE16	U24-C7
PS_DDR_DQ12	DDR Data Byte 1	AE19	U24-C2
PS_DDR_DQ13	DDR Data Byte 1	AD18	U24-C8
PS_DDR_DQ14	DDR Data Byte 1	AB18	U24-D3

Signal Name	Description	Bank 504 MPSoC Pin	DDR4 Pin
PS_DDR_DQ15	DDR Data Byte 1	AC18	U24-D7
PS_DDR_DM1	DDR Data Byte 1 Data Mask	AB17	U24-E2
PS_DDR_DQS1_P	DDR Data Byte 1 Data Strobe Pair	AD17	U24-B7
PS_DDR_DQS1_N	DDR Data Byte 1 Data Strobe Pair	AE17	U24-A7
PS_DDR_DQ16	DDR Data Byte 2	W18	U25-G2
PS_DDR_DQ17	DDR Data Byte 2	Y19	U25-F7
PS_DDR_DQ18	DDR Data Byte 2	AA19	U25-H3
PS_DDR_DQ19	DDR Data Byte 2	W16	U25-H7
PS_DDR_DQ20	DDR Data Byte 2	AA18	U25-H2
PS_DDR_DQ21	DDR Data Byte 2	AA15	U25-H8
PS_DDR_DQ22	DDR Data Byte 2	Y16	U25-J3
PS_DDR_DQ23	DDR Data Byte 2	Y15	U25-J7
PS_DDR_DM2	DDR Data Byte 2 Data Mask	W17	U25-E7
PS_DDR_DQS2_P	DDR Data Byte 2 Data Strobe Pair	Y17	U25-G3
PS_DDR_DQS2_N	DDR Data Byte 2 Data Strobe Pair	AA17	U25-F3
PS_DDR_DQ24	DDR Data Byte 3	AE20	U25-A3
PS_DDR_DQ25	DDR Data Byte 3	AD19	U25-B8
PS_DDR_DQ26	DDR Data Byte 3	AB20	U25-C3
PS_DDR_DQ27	DDR Data Byte 3	AC19	U25-C7
PS_DDR_DQ28	DDR Data Byte 3	AE21	U25-C2
PS_DDR_DQ29	DDR Data Byte 3	AB21	U25-C8
PS_DDR_DQ30	DDR Data Byte 3	AE22	U25-D3
PS_DDR_DQ31	DDR Data Byte 3	AD22	U25-D7
PS_DDR_DM3	DDR Data Byte 3 Data Mask	AD21	U25-E2
PS_DDR_DQS3_P	DDR Data Byte 3 Data Strobe Pair	AC20	U25-B7
PS_DDR_DQS3_N	DDR Data Byte 3 Data Strobe Pair	AC21	U25-A7
+DDR4_VREF	DDR Reference voltage	-	VREFCA
+DDR4_VTT	DDR Termination voltage	-	-

Table 1– DDR4 Connections

NOTE: (U24 or U25 indicates DDR4 Device Reference Designator)

2.2.2 Dual Parallel (x8) QSPI Flash

The UltraZed-EG SOM features two 4-bit SPI (quad-SPI) serial NOR flash devices organized in a dual parallel configuration. The **Micron MT25QU256ABAIEW7-0SIT** QSPI Flash devices are used on the UltraZed-EG SOM. The Multi-I/O SPI Flash memory is used to provide non-volatile boot, application code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem (bitstream).

The Quad-SPI Flash connects to the Zynq UltraScale+ MPSoC PS QSPI interface. This requires connection to specific pins in MIO Bank 500, specifically MIO[0:12] as outlined in the Zynq UltraScale+ TRM (Technical Reference Manual, UG1085). Quad-SPI feedback mode is used, thus the CLK_FOR_LPBK signal tied to MIO[6] is left floating. This allows a QSPI clock frequency greater than FQSPICLK2.

The Zynq UltraScale+ MPSoC peripheral used to control the QSPI flash devices is named QSPI. The QSPI devices can be operated up to 166MHz depending on the operating mode and the possible performance of the QSPI controller in the MPSoC. The QSPI flash devices are physically connected to the QSPI controller in the PS of the Zynq UltraScale+ MPSoC via Bank 500.

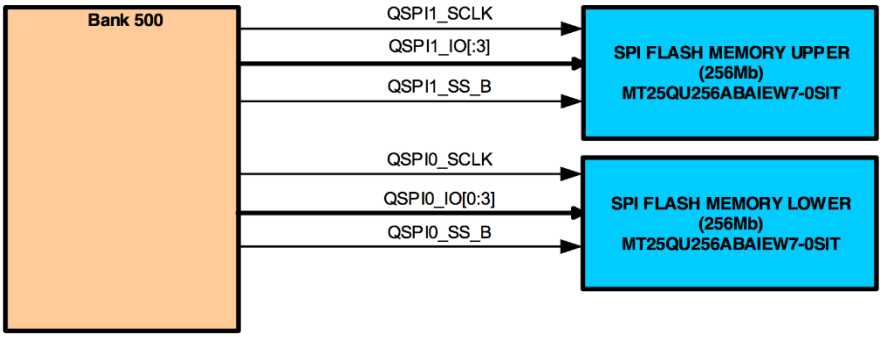


Figure 4 – Dual QSPI Block Diagram

Signal Name	Description	MPSoC Pin	MIO	Quad-SPI Pin
MIO0_QSPI0_SCLK	Lower QSPI Serial Clock	V10	MIO 0	U2-6
MIO1_QSPI0_IO1	Lower QSPI Data [1]	W11	MIO 1	U2-2
MIO2_QSPI0_IO2	Lower QSPI Data [2]	V11	MIO 2	U2-3
MIO3_QSPI0_IO3	Lower QSPI Data [3]	W9	MIO_3	U2-7
MIO4_QSPI0_IO0	Lower QSPI Data [0]	Y9	MIO_4	U2-5
MIO5_QSPI0_SS_B	Lower QSPI Select	AA10	MIO_5	U2-1
FLOAT (NC)	Loopback Clock	Y10	MIO_6	-
MIO7_QSPI1_SS_B	Upper QSPI Select	Y11	MIO_7	U3-1
MIO8_QSPI1_IO0	Upper QSPI Data [0]	AC10	MIO_8	U3-5
MIO9_QSPI1_IO1	Upper QSPI Data [1]	AB10	MIO_9	U3-2
MIO10_QSPI1_IO2	Upper QSPI Data [2]	W12	MIO_10	U3-3
MIO11_QSPI1_IO3	Upper QSPI Data [3]	AE10	MIO_11	U3-7
MIO12_QSPI1_SCLK	Upper QSPI Serial Clock	AB11	MIO_12	U3-6

Table 2 – Quad-SPI Flash Pin Assignment and Definitions

NOTE: (U2 or U3 indicates QSPI Device Reference Designator)

2.2.3 eMMC x8 Flash (Multi-Media Controller)

The UltraZed-EG SOM features a Micron MTFC8GAKAJCN-4M IT eMMC Multi Media Controller and NAND Flash IC. The eMMC is used to provide non-volatile user data storage and/or primary or secondary boot storage.

The relevant device attributes are:

- 8GB (default) - Optional densities available via customization
- Industrial temperature range (-40C to +85C)
- 8-bit data interface

The Zynq UltraScale+ MPSoC peripheral used to control the eMMC flash device is named **SD0**. The eMMC flash device can be operated up to 52MHz and is physically connected to the PS of the Zynq UltraScale+ MPSoC via Bank 500. The eMMC I/O has direct connections to the Zynq UltraScale+ MIO through the PS_MIO [13:22] pins.

The UltraZed-EG SOM end-user is capable of issuing a soft reset, **P0_EMMC0_RST_N**, to the eMMC flash device via an on board two-wire serial interface. The active low reset is assigned to Port 0 of the Texas Instruments TCA9534 I/O expander. The I/O expander is attached to an I2C peripheral on the Zynq UltraScale+ device. For further information on the I/O expander and its connections, please locate the I/O expander section within this hardware user guide.

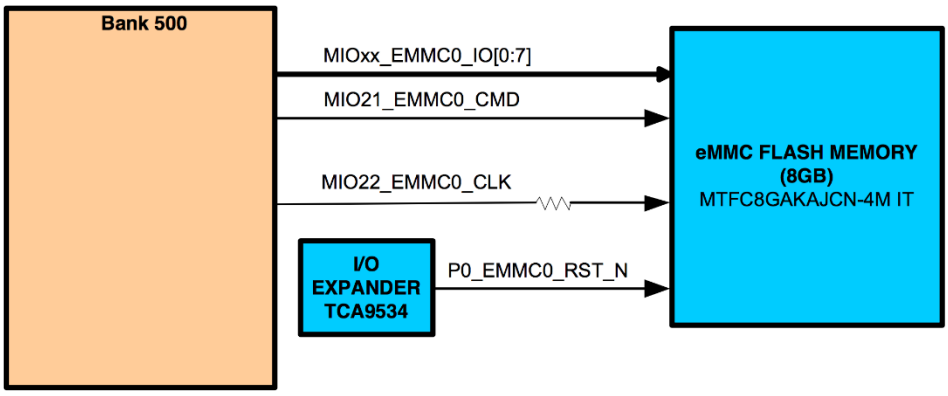


Figure 5 – eMMC Block Diagram

Signal Name	Description	MPSoC Pin	MIO	eMMC Pin
MIO13_EMMC0_IO0	EMMC Data IO [0]	Y12	MIO_13	A3
MIO14_EMMC0_IO1	EMMC Data IO [1]	AC11	MIO_14	A4
MIO15_EMMC0_IO2	EMMC Data IO [2]	W13	MIO_15	A5
MIO16_EMMC0_IO3	EMMC Data IO [3]	V13	MIO_16	B2
MIO17_EMMC0_IO4	EMMC Data IO [4]	AD11	MIO_17	B3
MIO18_EMMC0_IO5	EMMC Data IO [5]	AB12	MIO_18	B4
MIO19_EMMC0_IO6	EMMC Data IO [6]	AE11	MIO_19	B5
MIO20_EMMC0_IO7	EMMC Data IO [7]	AA12	MIO_20	B6
MIO21_EMMC0_CMD	EMMC Command	AD12	MIO_21	M5
MIO22_EMMC0_CLK	EMMC Clock	W14	MIO_22	M6

Table 3 – eMMC Pin Assignment and Definitions

NOTE: EMMC18 Boot Mode: MODE PINS [3:0] – 0x6

2.2.4 SFVA625 Device Package Delay Compensation for Memory Interfaces

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the each of the memory interfaces signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.3 GTR Transceivers

The UltraZed-EG SOM has four multi-gigabit transceiver lanes that reside on Bank 505 of the Zynq UltraScale+ MPSoC device. These transceivers can be used to interface to multiple high speed interface protocols such as PCI Express, Serial ATA, USB3.0, and Display Port. The associated high speed protocol MAC layers are hardened macros that exist in the PS subsystem of the Zynq UltraScale+ MPSoC device so additional Intellectual Property (IP) or targeted devices are not necessary to complete the various interfaces.

The Zynq UltraScale+ MPSoC is enabled with four GTR transceivers which are capable of a transceiver data rates up to 6.0 Gbps. Four differential MGT reference clock inputs are available to support the GTR transceiver lanes. The multi-gigabit transceiver lanes and their associated reference clocks are connected to the end-user carrier board via the JX3 Micro Header.

The UltraZed-EG SOM is capable of implementing up to a PCIe x4 interface as the physical design of the GTRs are each length tuned from the Zynq UltraScale+ MPSoC device to the JX3 connector taking into account the device package delays. The MPSoC device net length report provided by Xilinx and the PCB net length report provided by Avnet can be used to determine the required delay for each implemented interface on the end-user carrier card.

The table below shows the connections between the Zynq UltraScale+ MPSoC device and the JX3 Micro Header.

PS IO Name	Package Pin Number	Net Name	JX3 Connector
PS_MGTRRXN0_505	M25	GTR_RX0_N	JX3.28
PS_MGTRRXN1_505	H25	GTR_RX1_N	JX3.20
PS_MGTRRXN2_505	D25	GTR_RX2_N	JX3.12
PS_MGTRRXN3_505	B25	GTR_RX3_N	JX3.6
PS_MGTRRXP0_505	M24	GTR_RX0_P	JX3.26
PS_MGTRRXP1_505	H24	GTR_RX1_P	JX3.18
PS_MGTRRXP2_505	D24	GTR_RX2_P	JX3.10
PS_MGTRRXP3_505	B24	GTR_RX3_P	JX3.4
PS_MGTRTXN0_505	K25	GTR_TX0_N	JX3.23
PS_MGTRTXN1_505	F25	GTR_TX1_N	JX3.15
PS_MGTRTXN2_505	C23	GTR_TX2_N	JX3.9
PS_MGTRTXN3_505	A23	GTR_TX3_N	JX3.3
PS_MGTRTXP0_505	K24	GTR_TX0_P	JX3.21
PS_MGTRTXP1_505	F24	GTR_TX1_P	JX3.13
PS_MGTRTXP2_505	C22	GTR_TX2_P	JX3.7
PS_MGTRTXP3_505	A22	GTR_TX3_P	JX3.1
PS_MGTREFCLK0N_505	L23	GTR_REFCLK0_N	JX3.40
PS_MGTREFCLK0P_505	L22	GTR_REFCLK0_P	JX3.38
PS_MGTREFCLK1N_505	J23	GTR_REFCLK1_N	JX3.35
PS_MGTREFCLK1P_505	J22	GTR_REFCLK1_P	JX3.33
PS_MGTREFCLK2N_505	G23	GTR_REFCLK2_N	JX3.34
PS_MGTREFCLK2P_505	G22	GTR_REFCLK2_P	JX3.32
PS_MGTREFCLK3N_505	E23	GTR_REFCLK3_N	JX3.29
PS_MGTREFCLK3P_505	E22	GTR_REFCLK3_P	JX3.27
PS_MGTRREF_505	K22	GTR_RREF	-

Table 4 – Bank 505 GTR Pin Assignments

2.3.1 SFVA625 Device Package Delay Compensation for GTR Transceiver Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the each of the GTR transceiver signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.4 USB 2.0 OTG

The Zynq UltraScale+ MPSoC contains a hardened PS USB 2.0 controller. The UltraZed-EG SOM takes advantage of one of the two available PS USB 2.0 controllers to provide USB 2.0 On-The-Go signalling to the JX3 connector.

An external PHY with an 8-bit ULPI interface is implemented. A Microchip USB3320 Standalone USB Transceiver Chip is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. VDDIO for this device can be 1.8V or 3.3V, and on the UltraZed-EG SOM VDDIO is powered at 1.8V. The PHY is connected to MIO Bank 502 which is also powered at 1.8V. This is critical since a level translator cannot be used as it would impact the ULPI timing between the PHY and the Zynq UltraScale+ MPSoC device.

Additionally, the USB3320 must clock the ULPI interface which requires a 24 MHz crystal or oscillator (configured as ULPI Output Clock Mode). On the UltraZed-EG SOM, the 24 MHz oscillator is an Abracon ASDMB CMOS oscillator, ASDMB-24.000MHZ-LY-T.

The physical USB connector is not populated on the UltraZed-EG SOM. The SOM is designed to have the physical USB connector reside on the end-user carrier card. The four USB connector signals (USB_OTG_P, USB_OTG_N, USB_ID and USB_OTG_CPEN) and USB_OTG_VBUS are connected to the JX3 Micro Header. The table below shows the connections of these signals at JX3.

Signal Name	JX3 Pin
USB_OTG_N	47
USB_OTG_P	45
USB_ID	51
USB_OTG_CPEN	48
USB_OTG_VBUS	50

Table 5 – USB 2.0 JX3 Pin Assignments

The USB0 peripheral is used on the PS, connected through MIO [52-63] in MIO Bank 502. The USB Reset signal is active-low and connected to the I/O expander via Port 1, **P1_USB0_RST_N**. Either of the push button resets, **PS_POR_B** or **PS_SRST_B** will also generate the active-low USB Reset signal.

The UltraZed-EG SOM, with additional circuitry on an end-user carrier card, can be configured to operate in Host Mode (OTG) or Device Mode. With a standard connection to an end-user carrier card (no power supply used to provide USB power to the connector) the device will operate in Device Mode. Using the USB_OTG_CPEN signal on JX3 allows the user to control an external power source for USB_OTG_VBUS on the end-user carrier card. Other considerations need to be made to accommodate Host Mode. Refer to the Avnet UltraZed-EG I/O Carrier Card design for an example design for configuring the end-user carrier card for either Host Mode or Device Mode.

Signal Name	Description	MPSoC Bank	MIO	USB3320 Pin
DATA[7:0]	USB Data lines	MIO Bank 502	52:63	D[7:0]
CLKOUT	USB Clock	MIO Bank 502		1
DIR	ULPI DIR output signal	MIO Bank 502		31
STP	ULPI STP input signal	MIO Bank 502		29
NXT	ULPI NXT output signal	MIO Bank 502		2
REFSEL[2:0]	USB Chip Select	N/C	N/C	8,11,14
DP	DP pin of USB Connector			18
DM	DM pin of USB Connector			19
ID	Identification pin of the USB connector			23
RESET_B	Active-Low Reset	MIO Bank 502	N/C	27**

Table 6 – USB 2.0 Pin Assignment and Definitions

*** Connected through AND-gates with PS_POR_B, PS_SRST_B, and P1_USB0_RST_N from the I/O expander*

2.4.1 SFVA625 Device Package Delay Compensation for USB2.0 Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the USB2.0 signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.5 10/100/1000 Ethernet PHY

The UltraZed-EG SOM provides a single 10/100/1000 Ethernet port. The Zynq UltraScale+ MPSoC contains hardened PS Gigabit Ethernet MAC (GEM) controllers. The UltraZed-EG SOM takes advantage of one of the available PS GEM controllers to provide RGMII Ethernet signalling to the JX3 connector. The Texas Instruments DP83867 device is used to implement this interface. The 10/100/1000 Ethernet PHY connect to the Zynq UltraScale+ MPSoC device through Bank 502.

The physical RJ45 connector and magnetics is not populated on the UltraZed-EG SOM. The SOM is designed to have the physical RJ45 connector and magnetics reside on the end-user carrier card. The RJ45 connector signals are connected to the JX3 Micro Header. The table below shows the connections of these signals to the JX3 Micro Header.

Signal Name	JX3 Pin
ETH_MD1_P	57
ETH_MD1_N	59
ETH_MD2_P	56
ETH_MD2_N	58
ETH_MD3_P	63
ETH_MD3_N	65
ETH_MD4_P	62
ETH_MD4_N	64
ETH_PHY_LED0	53
ETH_PHY_LED1	52

Table 7 – 10/100/1000 Ethernet JX3 Pin Assignments

The next table shows the pin assignments to Bank 502 of the Zynq UltraScale+ MPSoC device for the 10/100/1000 Ethernet Port.

Ethernet PHY Signals	MPSoC Pin
MIO77_GEM3_MDIO	H19
MIO76_GEM3_MDC	H20
MIO74_GEM3_RX_D3	G20
MIO73_GEM3_RX_D2	F20
MIO72_GEM3_RX_D1	E20
MIO71_GEM3_RX_D0	E19
MIO75_GEM3_RX_CTL	F19
MIO70_GEM3_RX_CLK	C20
MIO68_GEM3_TX_D3	G18
MIO67_GEM3_TX_D2	H18
MIO66_GEM3_TX_D1	D19
MIO65_GEM3_TX_D0	A20
MIO69_GEM3_TX_CTL	B20
MIO64_GEM3_TX_CLK	F18
GEM3_RST_N	N/C

Table 8 – 10/100/1000 Ethernet MPSoC Pin Assignments

The GEM3 peripheral is used on the PS, connected through MIO [64-77] in MIO Bank 502. The Ethernet Reset signal is active-low and connected to the I/O expander via Port 2, P2_GEM3_RST_N. Either of the push button resets, **PS_POR_B** or **PS_SRST_B** will also generate the active-low Ethernet Reset signal.

The UltraZed-EG SOM also contains an active-low Ethernet PHY interrupt/power down signal that is connected to the I/O expander via Port 3, **P3_GEM3_PWDN_N**. By default, the end-user can assert this control signal to enable the Power Down mode of operation for the Gigabit Ethernet PHY. Alternatively, if the pin is programmed as an interrupt output, interrupts will be asserted low to the I/O Expander. The latter requires register access to the Gigabit Ethernet PHY as well as a software polling mechanism for the I/O Expander to identify interrupt activity.

A high-level block diagram of the 10/100/1000 Ethernet interface is shown in the following figure.

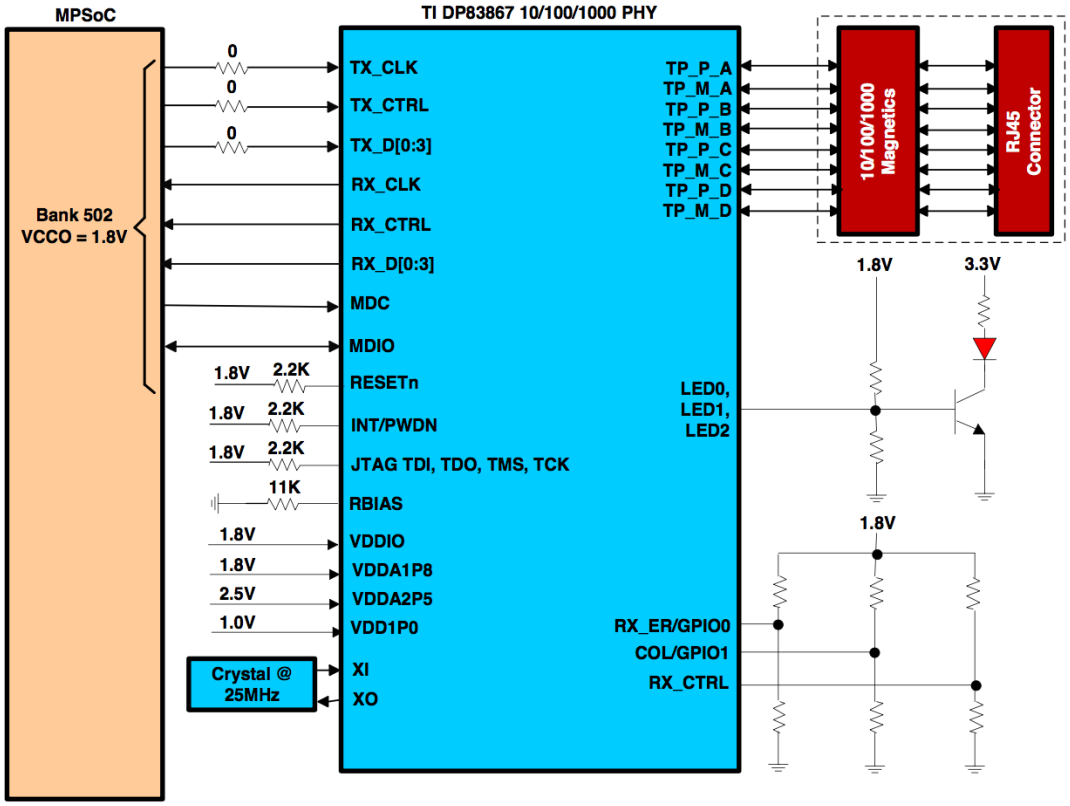
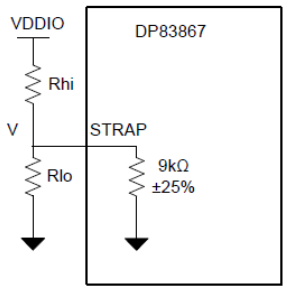


Figure 6 – 10/100/1000 Ethernet Interface Implementation

2.5.1 Ethernet PHY Strapping Resistors

The **Texas Instruments DP83867** device that is utilized to implement the 10/100/1000 Ethernet PHY functionality contains many setup options that can be implemented through strapping resistors physically on the PCB rather than through register accesses in software. These strapping resistors allow the 10/100/1000 Ethernet PHYs to be active without user interaction.

The following figure shows the strapping circuit and the possible resistor combinations that set the proper mode.



Strap Resistor Ratios

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Figure 7 – PHY Strapping Circuit and Modes

The following table lists the various strapping options that are available for the 10/100/1000 Ethernet PHY on the UltraZed-EG SOM and the default mode that they are strapped too. For a definition of what other options are available by changing the default mode settings, please refer to the **Texas Instruments DP83867** data sheet.

PHY1 Strap Function	PHY1 Pin Name	Mode Set	Function Value
PHYADD[1:0]	RX_D0	2	“01”
PHYADD[3:2]	RX_D2	1	“00”
EEE Disable / Autoneg Disable	RX_CTRL	3	“10”
RGMII Clock Skew RX[0]	GPIO_0	1	“0”
RGMII Clock Skew RX[2:1]	GPIO_1	2	“01”
RGMII Clock Skew TX[1:0]	LED_2	3	“10”
SPEED_SEL / RGMII Clock Skew TX[2]	LED_1	1	“00”
Mirror Enable / SGMII Enable	LED_0	1	“00”

Table 9 – 10/100/1000 Ethernet PHY Strapping Configuration

This set PHY1 ADDRESS to “0001”, RGMII RX Clock Skew to “001” for 1.0ns skew, RGMII TX Clock Skew to “001” for 1.0ns skew, and SPEED SEL to “0” for Tri-Mode Ethernet.

2.5.2 Ethernet PHY LEDs

The UltraZed-EG SOM contains a single Ethernet PHY controlled LED, the LINK LED. On board the end- user carrier card or within the RJ45 Ethernet Jack on the end-user carrier card, two additional Ethernet PHY controlled LED signal are provided, SPEED and ACTIVITY.SPEED and ACTIVITY LEDs need to be implemented on the end-user carrier card. Care must be taken when implementing these LEDs as the signals being driven onto the JX3 connector by the Ethernet PHY are at 1.8V and that may not be enough to illuminate the LEDs in an RJ45 jack or other on-board LED circuitry. A recommendation for the end-user carrier card would be to implement a circuit similar to the LINK LED that exists on the UltraZed-EG SOM.

2.5.3 SFVA625 Device Package Delay Compensation for 10/100/1000 Ethernet Interface

The Zynq UltraScale+ MPSoC device package delay is accommodated for in the layout of the Gigabit Ethernet signal trace lengths. The average of min and max values for package delay is utilized to compensate for the flight time caused by the delay associated with this package.

2.6 I2C I/O Expander

The UltraZed-EG SOM uses a **Texas Instruments TCA9534PWR** (**16-pin TSSOP**) I2C and SMBUS Low- Power I/O Expander. The Zynq UltraScale+ MPSoC controller required for I2C is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 10 – I2C1 TRM Pin Mapping

Each of the ports of the I2C I/O Expander represents functions different control functions like resets and power down. The following tables describes the connections and functionality of the ports of the I2C I/O Expander.

I/O Expander Name	I/O Expander Pin	Function	Net Name
A0	1	ADDRESS	GND
A1	2	ADDRESS	GND
A2	3	ADDRESS	GND
P0	4	P-PORT	P0_EMMC0_RST_N
P1	5	P-PORT	P1_USB0_RST_N
P2	6	P-PORT	P2_GEM3_RST_N
P3	7	P-PORT	P3_GEM3_PWDN_N
GND	8	GROUND	GND
P4	9	P-PORT	P4_I2CMUX_INT_N
P5	10	P-PORT	P5_PMBUS_ALERT_N
P6	11	P-PORT	P6_I2CMUX_RST_N
P7	12	P-PORT	P7_CC_RST_N
INT_N	13	INTERRUPT	MIO23_INT_N
SCL	14	SERIAL CLOCK	MIO24_I2C1_SCL
SDA	15	SERIAL DATA	MIO25_I2C1_SDA
VCC	16	POWER	+VCCO_PSIO0_500

Table 11 – Texas Instruments TCA9534 Pin Mapping

I/O Name	Function	Direction	Active-State	Net Name
P0	eMMC Soft Reset	OUTPUT	LOW	P0_EMMC0_RST_N
P1	USB 2.0 ULPI PHY Soft Reset	OUTPUT	LOW	P1_USB0_RST_N
P2	Gigabit Ethernet PHY Soft Reset	OUTPUT	LOW	P2_GEM3_RST_N
P3	Gigabit Ethernet Power-Down	OUTPUT	LOW	P3_GEM3_PWDN_N
P4	2-Ch I2C Switch/Mux Interrupt	INPUT	LOW	P4_I2CMUX_INT_N
P5	PMBUS Alert #	INPUT	LOW	P5_PMBUS_ALERT_N
P6	2-Ch I2C Switch/Mux Soft Reset	OUTPUT	LOW	P6_I2CMUX_RST_N
P7	Carrier Card Reset	OUTPUT	LOW	P7_CC_RST_N

Table 12 – eMMC Pin Assignment and Definitions

The following figure describes the addressing required to access the I2C I/O Expander. Please see the appropriate device datasheet for further details regarding accessing this device.

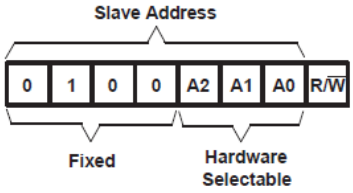


Figure 8 – I2C I/O Expander Addressing

2.7 I2C Switch/Multiplexer

The UltraZed-EG SOM uses a Texas Instruments TCA9543APWR (14-pin TSSOP) Serial Bus Switch/MUX with Interrupt. The Zynq UltraScale+ MPSoC controller required for I2C is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 13 – I2C1 TRM Pin Mapping

The I2C Switch/MUX allows for selection of control of the end-user carrier card two-wire serial interface or alternatively one could select the PMBUS interface that is tied to the UltraZed-EG SOM main multi-output power supplies as well as any device that may exist on the end-user carrier card PMBUS through the JX2 connector. The two-wire serial interface on the Zynq UltraScale+ MPSoC is used as the serial source for to the TCA9543A.The following table shows the connections to the TCA9543A device.

SWITCH/MUX Name	SWITCH/MUX Pin	Function	Net Name
A0	1	ADDRESS	GND
A1	2	ADDRESS	GND
RESET_N	3	RESET	P6_I2CMUX_RST_N
INT0_N	4	INTERRUPT0	CC_INT_N
SD0	5	SERIAL DATA0	CC_SDA
SC0	6	SERIAL CLOCK0	CC_SCL
GND	7	GROUND	GND
INT1_N	8	INTERRUPT1	N/C
SD1	9	SERIAL DATA1	PMBUS_SDA
SC1	10	SERIAL CLOCK1	PMBUS_SCL
INT_N	11	INTERRUPT	P4_I2CMUX_INT_N
SCL	12	SERIAL CLOCK	MIO24_I2C1_SCL
SDA	13	SERIAL DATA	MIO25_I2C1_SDA
VCC	14	POWER	+2.5V

Table 14 – Texas Instruments TCA9543A Pin Mapping

The following table should provide a clearer understanding of how the TCA9543A is expected to function in the system.

Switch/MUX Channel	Usage	Notes
Master Channel (SDA/SCL/INT)	This channel is connected to the PS I2C port, MIO [24:25] and operated at 1.8V. The master **INT_N** output is connected to the P4 port of the I2C 8-bit I/O expander.	Pulled-up to 1.8V on the SOM
Slave Channel 0 (SD0/SC0/INT0)	This channel is connected to the JX3 connector (**CC_SDA**, **CC_SCL**, and **CC_INT_N** signals) to allow slave I2C devices on the Carrier Card to be virtually placed on the same PS I2C bus (MIO [24:25]) as the I2C devices on the UltraZed-EG SOM so that software can use a single PS I2C core to communicate with all I2C devices in the system.	Pulled-up to 1.8V, 2.5V, or 3.3V on the Carrier Card
Slave Channel 1 (SD1/SC1/INT1)	This channel is connected to the PMBus (**PMBUS_SDA** and **PMBUS_SCL** signals) of the UltraZed-EG SOM PMBus voltage regulators and used to control all PMBus voltage regulators on the UltraZed-EG SOM as well as the Carrier Card (the PMBus is connected to the Carrier Card via JX2 connector). This feature will allow the PS to control/monitor the PMBus voltage regulators on the UltraZed-EG SOM as well as the Carrier Card for the purpose of power management and/or measurements.	Pulled-up to 3.3V on the SOM The unused slave channel 1 **INT1_N** input must be pulled up to the VCC (2.5V) rail.

Table 15 – I2C MUX/SWITCH Channel Usage

The following figure describes the addressing required to access the I2C Switch/MUX. Please see the appropriate device datasheet for further details regarding transactions to and from this device.

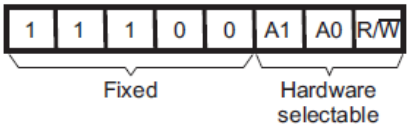


Figure 9 – I2C Switch/MUX Addressing

2.7.1 End-User Carrier Card I2C Interface

The UltraZed-EG SOM provides a master two-wire serial bus (**CC_SDA**, **CC_SCL**, and **CC_INT_N**) to the end-user carrier card via the JX3 connector so that software can communicate with all I2C devices on the UltraZed-EG SOM as well as the slave I2C devices on the end-user carrier card using a single two-wire serial interface.

The end-user carrier card two-wire serial interface is connected to channel 0 of the 2-channel switch/mux device. End-user carrier cards can drive the **INT0_N** of the channel 0 via **CC_INT_N**, if they so desire. The **CC_INT_N** (an **active low** signal) is not specific to the I2C interface and can be used as a general-purpose interrupt from end-user carrier cards to the UltraZed-EG SOM. If not used, the **CC_INT_N** signal is to be pulled up to 1.8V, 2.5V, or 3.3V on the Carrier Card. Since channel 0 I2C bus is dedicated to the end-user carrier card, two-wire serial devices with any address can reside on this bus without conflicting with the I2C devices on the UltraZed-EG SOM.

Switch/MUX Name	Switch/MUX Pin	Function	Net Name	JX3 Connector
INT0_N	4	INTERRUPT0	CC_INT_N	JX3.68
SD0	5	SERIAL DATA0	CC_SDA	JX3.41
SC0	6	SERIAL CLOCK0	CC_SCL	JX3.44

Table 16 – Carrier Card I2C Net Mapping

2.7.2 PMBUS Interface

A PMBus is used on the UltraZed-EG SOM to program/control/monitor all on-board PMBus voltage regulators. The UltraZed-EG SOM has access to the end-user carrier card PMBus signals via the JX2 connector (**PMBUS_SDA, PMBUS_SCL, and P5_PMBUS_ALERT_N** signals).

After the initial programming of all PMBus voltage regulators, the UltraZed-EG SOM can drive the PMBus (via channel 1 of the I2C switch/mux and P5 port of the I2C 8-bit I/O expander) in order to control/monitor the PMBus voltage regulators on the UltraZed-EG SOM for the purpose of power management and/or measurements. If the PMBus is implemented on the end-user carrier card, the UltraZed-EG SOM PMBus can monitor/control the end-user carrier card PMBus voltage regulators as well.

NOTE: If not used, the UltraZed-EG SOM PMBus interface must be left unconnected on the end-user carrier cards so that the UltraZed-EG SOM can still control/monitor its on-board PMBus regulators.

PMBUS Name	JX2 Connector
PMBUS_SDA	JX2.11
PMBUS_SCL	JX2.12
P5_PMBUS_ALERT_N	JX2.35

Table 17 – PMBUS JX2 Connector Mapping

The following figure shows how the PMBus will be connected on the UltraZed-EG SOM and the UltraZed IO Carrier Card from Avnet.

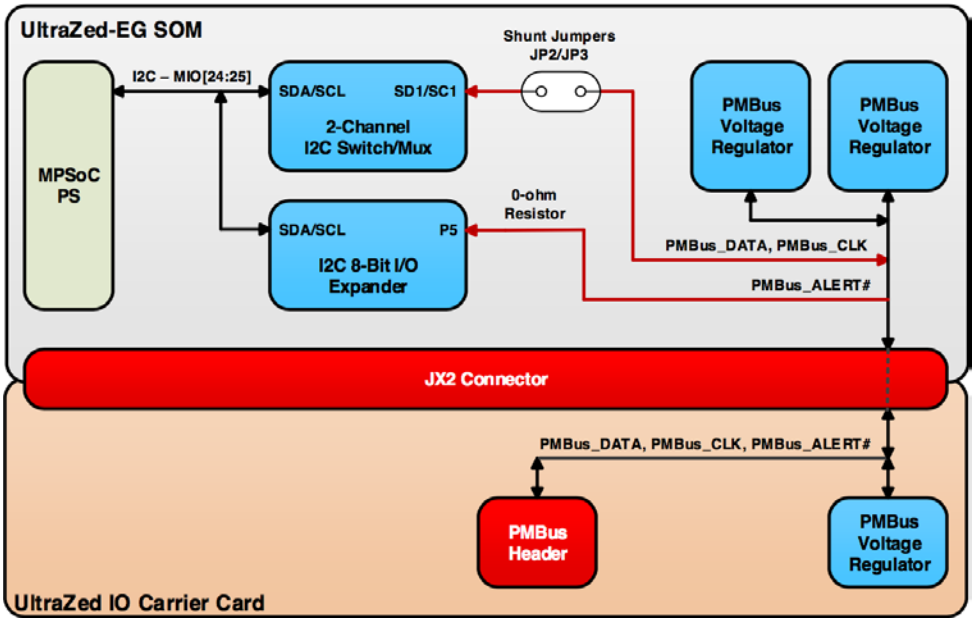


Figure 10 – PMBUS Connections

2.8 I2C EEPROM

The UltraZed-EG SOM uses an **Atmel AT34C02D-MAHM** 2-Kbit I2C EEPROM device. The Zynq UltraScale+ MPSoC controller required for serial access is named I2C1 and it exists at MIO [25:24].

IO Name	TRM Signal Name	Net Name
PS_MIO24	SCL_OUT	MIO24_I2C1_SCL
PS_MIO25	SDA_OUT	MIO25_I2C1_SDA

Table 18 – I2C1 TRM Pin Mapping

The following table describes the connections to the I2C EEPROM

EEPROM Name	EEPROM Pin	Function	Net Name
A0	1	ADDRESS INPUT	GND
A1	2	ADDRESS INPUT	GND
A2	3	ADDRESS INPUT	GND
VSS	4	GROUND	GND
SDA	5	SERIAL ADDR/DATA	MIO25_I2C1_SDA
SCL	6	SERIAL CLOCK	MIO24_I2C1_SCL
WP	7	WRITE PROTECT	GND
VCC	8	POWER	+VCCO_PSIO0_500

Table 19 – Atmel AT34C02D Pin Mapping

The following figure describes the addressing required to access the I2C EEPROM. Please see the appropriate device datasheet for further details regarding transactions to and from this device.

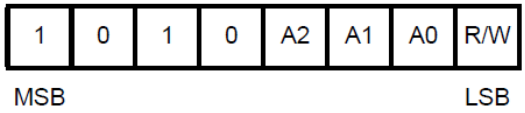


Figure 11 – I2C EEPROM Addressing

2.9 PS General Purpose Interrupt

The UltraZed-EG SOM contains a general purpose interrupt IO that is attached to PS MIO[23]. This interrupt signal will contain a pull-up to +VCCO_PSIO0_500. The interrupt output (INT#) of the Texas Instruments TCA9534 device is connected to the PS MIO [23].

IO Name	Net Name
PS_MIO23	MIO23_INT_N

Table 20 – PS Interrupt Pin Mapping

2.10 User I/O

2.10.1 PS MIO User Pins

The UltraZed-EG SOM provides 26 end-user PS MIO pins directly from Bank 501 of the Zynq UltraScale+ MPSoC to the JX3 Connector. The 26 PS MIO pins connect to the Zynq UltraScale+ Processor Sub-System for the implementation of peripherals such as USB, SPI, SDIO, CAN, UART, and I2C. These I/O pins can also be used as general purpose I/O to connect push buttons, LEDs and/or switches to the UltraZed-EG SOM from the end-user carrier card.

The VCCO for Bank 501 is set via pin 67 on the JX3 connector. VCCO for Bank 501 can be set to 1.8V, 2.5V, and 3.3V depending on what peripheral/circuitry may need to be implemented on the end-user carrier card.

NOTE: The Bank 501 PS MIO interface to the JX3 connector is provided in a master table that documents all of the JX Connections to the Zynq UltraScale+ MPSoC. See Section 2.13.2 JX connector master table.

2.10.2 PL IO User Pins

The UltraZed-EG SOM provides 24 user PL IO pins from Bank 26, 52 user PL IO pins from bank 64, 52 user PL IO pins from Bank 65, and 52 user PL IO pins from Bank 66 of the Zynq UltraScale+ MPSoC. The 180 PL IO pins on the UltraZed-EG SOM connect to the Zynq UltraScale+ Programmable Logic Sub-System for user implementation of most any feasible interface.

The PL IO pins are routed with matched lengths to each of the JX connectors by the Bank they are associated with. The matched pairs, noted by “DP” in the net name may be used as either single ended I/O or differential pairs depending on the end users design requirements.

Bank 26 is a high density bank that contains 24 single ended signals. The I/O supply voltage for the high density bank is +VCCO_HD_26 and the supply voltage range is +1.2V to +3.3V.

Bank 64, Bank 65, and Bank 66 IO are high performance banks that contain a mix of single ended signals and differential pairs. The I/O supply voltage for Bank 64, Bank 65, and Bank 66 can be individually controlled. The I/O supply voltages for Bank 64, Bank 65, and Bank 66 are +VCCO_HP_64, +VCCO_HP_65, and +VCCO_HP_66. The I/O supply voltage range for these high performance banks are +1.0V to +1.8V.

Use of these signals for various interfaces depends on the bank voltages assigned. The end-user carrier card is responsible for providing the appropriate bank voltages to the VCCO pins for Bank 26, Bank 64, Bank 65, and Bank 66 depending on what interface is being implemented.

PL I/O Bank 64, Bank 65, and 66 contains 52 I/O per bank capable of up to 24 differential pairs per bank with additional single ended signals. Differential LVDS pairs on a -1 speed grade device are capable of 1250Mbps of DDR data. Each differential pair from Bank 64, Bank 65, and Bank 66 is isolated by a power or ground pin. Additionally, 4 differential pairs per bank I/O can used to connect clock inputs.

It is recommended that any custom interface to be designed and run through the Vivado tool suite for a sanity check on place and route and timing closure in advance of end-user carrier card manufacturing.

NOTE: The Bank 26, Bank 64, Bank 65, and Bank 66 PL IO interface to the JX1 and JX2 connectors is provided in a master table that documents all of the JX Connections to the Zynq UltraScale+ MPSoC. See Section 2.13.2 for the JX connector master table.

2.11 Clock Sources

The UltraZed-EG SOM connects a dedicated 33.3333 MHz clock source to the Zynq UltraScale+ MPSoC PS to act as a system reference clock. An ABRACON ASDMB-33.333MHZ-LC-T or similar oscillator with 40-ohm series termination is used.

Zynq UltraScale+ MPSoC provides a built-in Real-Time Clock (RTC). A 32.768 KHz crystal is connected to the PS bank 503 **PS_PADI** and **PS_PADO** pins for the RTC. The on-chip RTC will use the **VCC_PSBATT** pin (provided by the end-user carrier card via JX3 connector) for the backup battery. Carrier Cards will drive the **VCC_PSBATT** pin with a 1.5V battery.

MIO Name	Package Pin Number	Net Name	JX3 Connector
PS_PADI	K17	PS_PADI	-
PS_PADO	K19	PS_PADO	-
VCC_PSBATT	N19	PS_VBATT	JX3.46

Table 21 – RTC Crystal Pin Assignments

2.12 Control Signal Sources

2.12.1 Power-On Reset (PS_POR_N) and Carrier Card Reset (CC_RESET_OUT_N)

The Zynq UltraScale+ MPSoC PS supports an external power-on reset signal. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. On UltraZed-EG SOM, this signal is labelled **PS_POR_B** and it is connected to push button, **SW3**. To stall Zynq UltraScale+ MPSoC boot-up, this signal should be held low. No other signal (**PS_SRST_B**, **PROGRAM_B**, or **INIT_B**) is capable of doing this as in other Xilinx FPGA architectures. Toggling SW3 should illuminate the **POR_RST_B** LED.

NOTE: By default, the **SW3** push button is **NOT** populated on production level UltraZed-EG SOMs.

The power-on-reset, **PS_POR_B**, is capable of resetting the end-user carrier card thru an open drain signal on the JX2 connector, **CC_RESET_OUT_N**. The UltraZed-EG SOM end-user is also capable of issuing a soft reset, **P7_CC_RST_N**, to the end-user carrier card via an on board two-wire serial interface. The soft reset is capable of resetting the end-user carrier card thru the same open drain signal on the JX2 connector, **CC_RESET_OUT_N**. The end-user carrier card is required to pull-up the **CC_RESET_OUT_N** signal to a voltage level suitable to the circuitry on the end-user carrier card that requires this reset signal.

The active low reset, **P7_CC_RST_N**, is assigned to Port 7 of the Texas Instruments TCA9534 I/O expander. The I/O expander is attached to an I2C peripheral on the Zynq UltraScale+ device. For further information on the I/O expander and its connections, please locate the I/O expander section within this hardware user guide.

NOTE: A custom end-user carrier card should design the on-board power solution to account for the bring up time of the individual power supplies and devise a method to ensure that power is valid prior to the booting of the Zynq UltraScale+ device. The custom end-user carrier card should use the SOM_PG_OUT signal to enable the on-board power supplies.

NOTE: The time required for all power rails to be stable is approximately 400ms.

2.12.2 PS_PROG_B, PS_DONE, PS_INIT_B, PUDC_B, POR_OVERRIDE, and ERROR

PS_INIT_B, PS_PROG_B and **PUDC_B** have pull-up resistors to appropriate voltages applied.

The **PS_PROG_B** signal is capable of being activated by push button, **SW1**. The **PUDC_B** and **PORT_OVERRIDE** signals can be pulled high (default) or low through a resistor jumper.

NOTE: By default, the **SW1** push button is **NOT** populated on production level UltraZed-EG SOMs.

There are several status LEDs on the UltraZed-EG SOM. There is a blue DONE LED indicator. When configuration is complete **PS_DONE** will go high illuminating the blue DONE LED. There is a green ERROR STATUS LED indicator and a red ERROR OUT LED indicator that will illuminate indicating that configuration did not complete properly via signal from **PS_ERROR_STATUS** and **PS_ERROR_OUT**.

2.12.3 Processor Subsystem Reset (PS_SRST_B) and SOM Reset (SOM_RESET_IN_N)

The system reset, labelled **PS_SRST_B**, resets the processor as well as erases all debug configurations.

On UltraZed-EG SOM, this signal is labelled **PS_SRST_B** and it is connected to push button, **SW4**. The UltraZed-EG SOM end-user is also capable of being issued an external system reset from the end-user carrier card via the JX2 Connector signal **SOM_RESET_IN_N**.

The active-low external system resets, **SW4** or **SOM_RESET_IN_N** allows the user to reset all of the functional logic within the device without disturbing the debug environment. Toggling **SW4** should illuminate the POR_RST_B LED. The SOM_RESET_IN signal should have a minimum pulse width of 3 PS_CLK cycles (90ns).

NOTE: By default, the **SW4** push button is **NOT** populated on production level UltraZed-EG SOMs.

NOTE: This signal cannot be asserted while the boot ROM is executing following a power-on reset (PS_POR_B). If PS_SRST_B is asserted while the boot ROM is running through a power-on reset sequence it will trigger a lock-down event preventing the boot ROM from completing. To recover from lockdown the device either needs to be power cycled or PS_POR_B needs to be asserted.

2.13 Expansion Headers

2.13.1 Micro Headers

The UltraZed-EG SOM features three Micro Headers for connection to end-user carrier cards. The three Micro Headers consist of two 140-pin connectors and one 100-pin connector.

The JX1 and JX2 connectors are the main interface to PL signals for the end-user carrier card. The JX1 and JX2 connectors also provide access to dedicated JTAG signals, various power rails, system monitor signals, PMBUS interface, and control signals. The JX3 connector interfaces to peripheral interfaces such as the GTR MGTs, Gigabit Ethernet, USB 2.0, and Bank 501 PS MIO. The JX3 connector also contains various power rails, the end-user carrier card I2C interface, as well as voltage sense signals for the end- user carrier card power supply feedback.

The connectors are TE 0.8mm Free Height Connectors with 100 Positions or 140 Positions Dual Row, Board-to-Board Vertical Plugs. These have variable stack heights making it easy to connect to a variety of expansion or system boards depending on the end-user requirements. Each pin is capable of carrying 500mA of current and support I/O speeds in excess of what Zynq UltraScale+ MPSoC can deliver.

The tables listed below show the connection types to the JX Micro Headers.

Micro Header JX1			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 64 Single Ended I/Os	Zynq UltraScale+ Bank 64	4
	Bank 65 Single Ended I/Os	Zynq UltraScale+ Bank 65	2
	Bank 64 Differential Pair I/Os	Zynq UltraScale+ Bank 64	48
	Bank 65 Differential Pair I/Os	Zynq UltraScale+ Bank 65	36
JTAG	JTAG_TMS	Zynq UltraScale+ Bank 503	4
	JTAG_TDI		
	JTAG_TCK		
	JTAG_TDO		
Power	GND	Carrier Card	37
	VIN		3
	VCCO_HP_64		3
	VCCO_HP_65		3
		Total	**140**

Table 22 – Micro Header JX1 Summary

Micro Header JX2			
Interface	**Signal Name**	**Source**	**Pins**
PL	Bank 26 Single Ended I/Os or Differential Input Pairs	Zynq UltraScale+ Bank 26	24
	Bank 65 Single Ended I/Os	Zynq UltraScale+ Bank 65	2
	Bank 66 Single Ended I/Os	Zynq UltraScale+ Bank 66	4
	Bank 65 Differential Pair I/Os	Zynq UltraScale+ Bank 65	12
	Bank 66 Differential Pair I/Os	Zynq UltraScale+ Bank 66	48
Control	PMBUS	Carrier Card or UltraZed-EG SOM	3
	SOM_PG_OUT	UltraZed-EG SOM	1
	CC_RESET_OUT_N	UltraZed-EG SOM	1
	SOM_RESET_IN	Carrier Card	1
SYSMON	SYMON_V_N SYSMON_V_P SYSMON_DX_N SYSMON_DX_P	Zynq UltraScale+ Bank 0	4
Power	GND	Carrier Card	31
	VIN		3
	VCCO_HD_26		3
	VCCO_HP_66		3
		Total	**140**

Table 23 – Micro Header JX2 Summary

Micro Header JX3			
Interface	**Signal Name**	**Source**	**Pins**
GTR	Bank 505 Differential Pair I/Os	Zynq UltraScale+ Bank 505	24
PS	Bank 501 PS MIO	Zynq UltraScale+ Bank 501	26
Comm	USB2.0 PHY Interface	UltraZed-EG SOM	4
	Gigabit Ethernet PHY Interface		10
	CC I2C BUS		3
Power	GND	Carrier Card	19
	MGTRAVCC		3
	MGTRAVTT		2
	VCCO_PSIO_501		1
	PS_VBATT		1
	USB_OTG_VBUS		1
	Voltage Feedback Sense Pins	UltraZed-EG SOM	6
		Total	**100**

Table 24 – Micro Header JX3 Summary

2.13.2 JX Connector Master Table

The following tales list the UltraZed-EG SOM JX Connectors connections in master tables targeting each connector.

Zynq Pin Number	UltraZed-EG Net Name	JX1 Pin Number		UltraZed-EG Net Name	Zynq Pin Number
K16	JTAG_TCK	1	2	JTAG_TMS	L18
L17	JTAG_TDO	3	4	JTAG_TDI	L15
L6, P5, U4	VCCO_HP_65	5	6	VCCO_HP_64	AA6, AB9, V7
L6, P5, U4	VCCO_HP_65	7	8	JX1_HP_DP_01_P	Y7
AB8	JX1_HP_DP_00_P	9	10	JX1_HP_DP_01_N	AA7
AB7	JX1_HP_DP_00_N	11	12	VCCO_HP_64	AA6, AB9, V7
L6, P5, U4	VCCO_HP_65	13	14	JX1_HP_DP_03_P	AC9
AA9	JX1_HP_DP_02_P	15	16	JX1_HP_DP_03_N	AC8
AA8	JX1_HP_DP_02_N	17	18	VCCO_HP_64	AA6, AB9, V7
N/A	GND	19	20	JX1_HP_DP_05_P	AD9
AD6	JX1_HP_DP_04_P	21	22	JX1_HP_DP_05_N	AE9
AD5	JX1_HP_DP_04_N	23	24	GND	N/A
N/A	GND	25	26	JX1_HP_DP_07_P	AD8
AE7	JX1_HP_DP_06_P	27	28	JX1_HP_DP_07_N	AD7
AE6	JX1_HP_DP_06_N	29	30	GND	N/A
N/A	GND	31	32	JX1_HP_DP_09_P	W1
AA4	JX1_HP_DP_08_P	33	34	JX1_HP_DP_09_N	Y1
AA3	JX1_HP_DP_08_N	35	36	GND	N/A
N/A	GND	37	38	JX1_HP_DP_11_P	AB2
W4	JX1_HP_DP_10_P	39	40	JX1_HP_DP_11_N	AB1
Y4	JX1_HP_DP_10_N	41	42	GND	N/A
N/A	GND	43	44	JX1_HP_DP_13_P	AB6
W3	JX1_HP_DP_12_P	45	46	JX1_HP_DP_13_N	AC6
W2	JX1_HP_DP_12_N	47	48	GND	N/A
N/A	GND	49	50	JX1_HP_DP_15_P	AE4
Y2	JX1_HP_DP_14_P	51	52	JX1_HP_DP_15_N	AE3
AA2	JX1_HP_DP_14_N	53	54	GND	N/A
N/A	GND	55	56	JX1_HP_DP_17_P	AD4
AD1	JX1_HP_DP_16_P	57	58	JX1_HP_DP_17_N	AD3
AE1	JX1_HP_DP_16_N	59	60	GND	N/A
N/A	GND	61	62	JX1_HP_DP_19_GC_P	AB3
AB5	JX1_HP_DP_18_GC_P	63	64	JX1_HP_DP_19_GC_N	AC3
AC4	JX1_HP_DP_18_GC_N	65	66	GND	N/A
N/A	GND	67	68	JX1_HP_DP_21_GC_P	Y5
W6	JX1_HP_DP_20_GC_P	69	70	JX1_HP_DP_21_GC_N	AA5
Y6	JX1_HP_DP_20_GC_N	71	72	GND	N/A
N/A	GND	73	74	JX1_HP_DP_23_P	W8
AD2	JX1_HP_DP_22_P	75	76	JX1_HP_DP_23_N	W7
AE2	JX1_HP_DP_22_N	77	78	GND	N/A
N/A	GND	79	80	JX1_HP_DP_25_P	R7
T5	JX1_HP_DP_24_P	81	82	JX1_HP_DP_25_N	T7
T4	JX1_HP_DP_24_N	83	84	GND	N/A
N/A	GND	85	86	JX1_HP_DP_27_P	T3

Zynq Pin Number	UltraZed-EG Net Name	JX1 Pin Number		UltraZed-EG Net Name	Zynq Pin Number
U6	JX1_HP_DP_26_P	87	88	JX1_HP_DP_27_N	U2
U5	JX1_HP_DP_26_N	89	90	GND	N/A
N/A	GND	91	92	JX1_HP_DP_29_P	U3
P3	JX1_HP_DP_28_P	93	94	JX1_HP_DP_29_N	V3
P2	JX1_HP_DP_28_N	95	96	GND	N/A
N/A	GND	97	98	JX1_HP_DP_31_P	U1
N1	JX1_HP_DP_30_P	99	100	JX1_HP_DP_31_N	V1
P1	JX1_HP_DP_30_N	101	102	GND	N/A
N/A	GND	103	104	JX1_HP_DP_33_P	K4
J7	JX1_HP_DP_32_P	105	106	JX1_HP_DP_33_N	J4
J6	JX1_HP_DP_32_N	107	108	GND	N/A
N/A	GND	109	110	JX1_HP_DP_35_P	K6
L7	JX1_HP_DP_34_P	111	112	JX1_HP_DP_35_N	K5
K7	JX1_HP_DP_34_N	113	114	GND	N/A
N/A	GND	115	116	JX1_HP_DP_37_GC_P	M3
N4	JX1_HP_DP_36_GC_P	117	118	JX1_HP_DP_37_GC_N	L3
N3	JX1_HP_DP_36_GC_N	119	120	GND	N/A
N/A	GND	121	122	JX1_HP_DP_39_P	R2
N5	JX1_HP_DP_38_P	123	124	JX1_HP_DP_39_N	R1
M5	JX1_HP_DP_38_N	125	126	GND	N/A
N/A	GND	127	128	JX1_HP_DP_41_P	L2
M6	JX1_HP_DP_40_P	129	130	JX1_HP_DP_41_N	K2
L5	JX1_HP_DP_40_N	131	132	VIN	N/A
N/A	VIN	133	134	JX1_HP_SE_01	AC1
V4	JX1_HP_SE_00	135	136	JX1_HP_SE_03	AC5
V5	JX1_HP_SE_02	137	138	JX1_HP_SE_05	L4
M7	JX1_HP_SE_04	139	140	VIN	N/A

Table 25 – JX1 Connector Master Table

Zynq Pin Number	UltraZed-EG Net Name	JX2 Pin Number		UltraZed-EG Net Name	Zynq Pin Number
P12	SYSMON_V_N	1	2	SYSMON_DX_N	R12
N13	SYSMON_V_P	3	4	SYSMON_DX_P	R13
N/A	GND	5	6	GND	N/A
H10	JX2_HD_SE_00_P	7	8	JX2_HD_SE_01_P	C10
H9	JX2_HD_SE_00_N	9	10	JX2_HD_SE_01_N	B10
N/A	PMBus_SDA	11	12	PMBus_SCL	N/A
B11	JX2_HD_SE_02_P	13	14	JX2_HD_SE_03_P	B12
A10	JX2_HD_SE_02_N	15	16	JX2_HD_SE_03_N	A12
D5, E8, G4	VCCO_HP_66	17	18	VCCO_HD_26	D10, F11
E11	JX2_HD_SE_04_GC_P	19	20	JX2_HD_SE_05_GC_P	F9
E10	JX2_HD_SE_04_GC_N	21	22	JX2_HD_SE_05_GC_N	E9
D5, E8, G4	VCCO_HP_66	23	24	VCCO_HD_26	D10, F11
D9	JX2_HD_SE_06_GC_P	25	26	JX2_HD_SE_07_GC_P	D11
C9	JX2_HD_SE_06_GC_N	27	28	JX2_HD_SE_07_GC_N	C11
D5, E8, G4	VCCO_HP_66	29	30	VCCO_HD_26	D10, F11
E12	JX2_HD_SE_08_P	31	32	JX2_HD_SE_09_P	G12
D12	JX2_HD_SE_08_N	33	34	JX2_HD_SE_09_N	F12
N/A	PMBus_ALERT_N	35	36	CC_RESET_OUT_N	N/A
H11	JX2_HD_SE_10_P	37	38	JX2_HD_SE_11_P	G10
G11	JX2_HD_SE_10_N	39	40	JX2_HD_SE_11_N	F10
N/A	SOM_PG_OUT	41	42	SOM_RESET_IN_N	N/A
N/A	GND	43	44	JX2_HP_DP_01_P	A3
D2	JX2_HP_DP_00_P	45	46	JX2_HP_DP_01_N	A2
D1	JX2_HP_DP_00_N	47	48	GND	N/A
N/A	GND	49	50	JX2_HP_DP_03_P	H4
C1	JX2_HP_DP_02_P	51	52	JX2_HP_DP_03_N	H3
B1	JX2_HP_DP_02_N	53	54	GND	N/A
N/A	GND	55	56	JX2_HP_DP_05_P	G3
G2	JX2_HP_DP_04_P	57	58	JX2_HP_DP_05_N	F3
F2	JX2_HP_DP_04_N	59	60	GND	N/A
N/A	GND	61	62	JX2_HP_DP_07_P	F4
E2	JX2_HP_DP_06_P	63	64	JX2_HP_DP_07_N	E4
E1	JX2_HP_DP_06_N	65	66	GND	N/A
N/A	GND	67	68	JX2_HP_DP_09_P	C6
B7	JX2_HP_DP_08_P	69	70	JX2_HP_DP_09_N	B6
A7	JX2_HP_DP_08_N	71	72	GND	N/A
N/A	GND	73	74	JX2_HP_DP_11_GC_P	E6
D7	JX2_HP_DP_10_GC_P	75	76	JX2_HP_DP_11_GC_N	E5
D6	JX2_HP_DP_10_GC_N	77	78	GND	N/A
N/A	GND	79	80	JX2_HP_DP_13_GC_P	D4
C4	JX2_HP_DP_12_GC_P	81	82	JX2_HP_DP_13_GC_N	D3
C3	JX2_HP_DP_12_GC_N	83	84	GND	N/A
N/A	GND	85	86	JX2_HP_DP_15_P	C5
A9	JX2_HP_DP_14_P	87	88	JX2_HP_DP_15_N	B5
A8	JX2_HP_DP_14_N	89	90	GND	N/A
N/A	GND	91	92	JX2_HP_DP_17_P	H1
C8	JX2_HP_DP_16_P	93	94	JX2_HP_DP_17_N	G1
B8	JX2_HP_DP_16_N	95	96	GND	N/A

Zynq Pin Number	UltraZed-EG Net Name	JX2 Pin Number		UltraZed-EG Net Name	Zynq Pin Number
N/A	GND	97	98	JX2_HP_DP_19_P	G7
A6	JX2_HP_DP_18_P	99	100	JX2_HP_DP_19_N	F7
A5	JX2_HP_DP_18_N	101	102	GND	N/A
N/A	GND	103	104	JX2_HP_DP_21_P	G8
H6	JX2_HP_DP_20_P	105	106	JX2_HP_DP_21_N	F8
G6	JX2_HP_DP_20_N	107	108	GND	N/A
N/A	GND	109	110	JX2_HP_DP_23_P	B3
G5	JX2_HP_DP_22_P	111	112	JX2_HP_DP_23_N	B2
F5	JX2_HP_DP_22_N	113	114	GND	N/A
N/A	GND	115	116	JX2_HP_DP_25_P	J3
K1	JX2_HP_DP_24_P	117	118	JX2_HP_DP_25_N	J2
J1	JX2_HP_DP_24_N	119	120	GND	N/A
N/A	GND	121	122	JX2_HP_DP_27_GC_P	P4
R6	JX2_HP_DP_26_GC_P	123	124	JX2_HP_DP_27_GC_N	R4
R5	JX2_HP_DP_26_GC_N	125	126	GND	N/A
N/A	GND	127	128	JX2_HP_DP_29_P	P7
M2	JX2_HP_DP_28_P	129	130	JX2_HP_DP_29_N	P6
M1	JX2_HP_DP_28_N	131	132	VIN	N/A
N/A	VIN	133	134	JX2_HP_SE_01	E7
D8	JX2_HP_SE_00	135	136	JX2_HP_SE_03	H5
A4	JX2_HP_SE_02	137	138	JX2_HP_SE_05	T2
U7	JX2_HP_SE_04	139	140	VIN	N/A

Table 26 – JX2 Connector Master Table

Zynq Pin Number	UltraZed-EG Net Name	JX3 Pin Number		UltraZed-EG Net Name	Zynq Pin Number
A22	GTR_TX3_P	1	2	GND	N/A
A23	GTR_TX3_N	3	4	GTR_RX3_P	B24
N/A	GND	5	6	GTR_RX3_N	B25
C22	GTR_TX2_P	7	8	GND	N/A
C23	GTR_TX2_N	9	10	GTR_RX2_P	D24
N/A	GND	11	12	GTR_RX2_N	D25
F24	GTR_TX1_P	13	14	GND	N/A
F25	GTR_TX1_N	15	16	GND	N/A
N/A	GND	17	18	GTR_RX1_P	H24
N/A	GND	19	20	GTR_RX1_N	H25
K24	GTR_TX0_P	21	22	GND	N/A
K25	GTR_TX0_N	23	24	GND	N/A
N/A	GND	25	26	GTR_RX0_P	M24
E22	GTR_REFCLK3_P	27	28	GTR_RX0_N	M25
E23	GTR_REFCLK3_N	29	30	GND	N/A
F22, H22	MGTRAVCC	31	32	GTR_REFCLK2_P	G22
J22	GTR_REFCLK1_P	33	34	GTR_REFCLK2_N	G23
J23	GTR_REFCLK1_N	35	36	MGTRAVTT	A24, B22, D22
F22, H22	MGTRAVCC	37	38	GTR_REFCLK0_P	L22
F22, H22	MGTRAVCC	39	40	GTR_REFCLK0_N	L23
N/A	CC_SDA	41	42	MGTRAVTT	A24, B22, D22
N/A	GND	43	44	CC_SCL	N/A
N/A	USB_OTG_P	45	46	PS_VBATT	N19
N/A	USB_OTG_N	47	48	USB_OTG_CPEN	N/A
N/A	GND	49	50	USB_OTG_VBUS	N/A
N/A	USB_ID	51	52	ETH_PHY_LED1	N/A
N/A	ETH_PHY_LED0	53	54	GND	N/A
N/A	GND	55	56	ETH_MD2_P	N/A
N/A	ETH_MD1_P	57	58	ETH_MD2_N	N/A
N/A	ETH_MD1_N	59	60	GND	N/A
N/A	GND	61	62	ETH_MD4_P	N/A
N/A	ETH_MD3_P	63	64	ETH_MD4_N	N/A
N/A	ETH_MD3_N	65	66	GND	N/A
G14, E13, D15	VCCO_PSIO_501	67	68	CC_INT_N	N/A
H13	MIO_26	69	70	MIO_27	G13
H14	MIO_28	71	72	MIO_29	B13
A13	MIO_30	73	74	MIO_31	C13
N/A	MGTRAVCC_Sense	75	76	MGTRAVTT_Sense	N/A
D13	MIO_32	77	78	MIO_33	F13
E14	MIO_34	79	80	MIO_35	F14
D14	MIO_36	81	82	MIO_37	H15
N/A	VCCO_HP_66_Sense	83	84	VCCO_HD_26_Sense	N/A
C14	MIO_38	85	86	MIO_39	A14
G15	MIO_40	87	88	MIO_41	A15
F15	MIO_42	89	90	MIO_43	B15
N/A	VCCO_HP_65_Sense	91	92	VCCO_HP_64_Sense	N/A
E15	MIO_44	93	94	MIO_45	H16
C15	MIO_46	95	96	MIO_47	B16
C16	MIO_48	97	98	MIO_49	G16
E16	MIO_50	99	100	MIO_51	D16

Table 27 – JX3 Connector Master Table

Signal Name	ZU3EG Bank	Voltage Domain	I/O Usage
JX1_HP_DP_[00:23]_P/N	64	VCCO_HP_64	Single-Ended or Differential I/O
JX1_HP_DP_[24:41]_P/N	65	VCCO_HP_65	Single-Ended or Differential I/O
JX1_HP_SE_[00:03]	64	VCCO_HP_64	Single-Ended
JX1_HP_SE_[04:05]	65	VCCO_HP_65	Single-Ended
JX2_HP_DP_[00:23]_P/N	66	VCCO_HP_66	Single-Ended or Differential I/O
JX2_HP_DP_[24:29]_P/N	65	VCCO_HP_65	Single-Ended or Differential I/O
JX2_HD_SE_[00:11]_P/N	26	VCCO_HD_26	Single-Ended or Differential Input
JX2_HP_SE_[00:03]	66	VCCO_HP_66	Single-Ended
JX2_HP_SE_[04:05]	65	VCCO_HP_65	Single-Ended
GTR_TX[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
GTR_RX[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
GTR_REFCLK[0:3]_P/N	505	MGTRAVCC / MGTRAVTT	Differential I/O
MIO_[26:51]	501	VCCO_PSIO_501	Single-Ended

Table 28 – JX Connector Signal Decoder

The following descriptions are provided to aid in determining the type of signal in the JX connector master table:

Pins in **Red** are Power or Ground signals.
Pins in **Blue** are dedicated signals.
Pins in **Black** are multi-function/general-purpose pins.
Pins in **Black** with **_GC** designators are multi-function/general-purpose pins or Global Clock inputs.
HP_DP stands for High Performance Differential Pairs
HP_SE stands for High Performance Single-Ended
HD_SE stands for High Density Single-Ended.
HD_SE signals can be used as Single-Ended or Differential Inputs.

2.13.3 Powering the PL Banks (SOM_PG_OUT)

The UltraZed-EG SOM does not power the PL VCCIO banks. This is required to be provided by the end- user carrier card. This gives the end-user carrier card the flexibility to control the I/O bank voltages depending on the interfaces the end-user decides to implement.

The Zynq UltraScale+ MPSoC has 4 PL I/O banks that are each capable of being powered separately by the end-user carrier card. The UltraZed-EG SOM provides an active-high **SOM_PG_OUT** signal to the end- user carrier card. The end-user carrier card shall not provide power to the PL VCCIO pins on the JX connectors until the **SOM_PG_OUT** signal becomes active.

2.14 Configuration Modes

The Zynq UltraScale+ MPSoC device uses a multi-stage boot process that supports both non-secure and secure boot. The PS is the master of the boot and configuration process. Upon reset, the device PS MODE pins are read to determine the primary boot device to be used. The UltraZed-EG SOM allows several of those boot devices: QSPI, SD Card, eMMC, and JTAG boot are easily accessible by changing the Boot Mode Switch, SW2, settings.

NOTE: The JTAG interface is to be implemented on the end-user carrier card.

The boot mode pins on Zynq UltraScale+ MPSoC are dedicated pins unlike the Zynq SoC which shared the mode pins with PS MIO pins. All PS MODE pins are pulled either high or low through the Boot Mode Switch. The table below shows the available boot mode configuration settings using the Boot Mode Switch, SW2.

Boot Mode	Mode Pin [3:0]	SW2 [1:4]
JTAG *	0x0	ON-ON-ON-ON
QSPI24	0x1	OFF-ON-ON-ON
QSPI32	0x2	ON-OFF-ON-ON
SD1/MMC33 *	0x5	OFF-ON-OFF-ON
EMMC18	0x6	ON-OFF-OFF-ON
SD1/MMC33 *	0xE	ON-OFF-OFF-OFF

Table 29 – UltraZed-EG SOM Configuration Modes

**Interfaces on the End User Carrier Card*

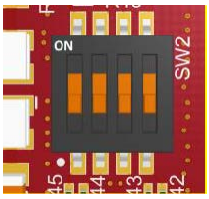


Figure 12 – UltraZed-EG SOM Boot Mode Switch

The boot time to application start may be affected by a number of circumstances such as the hardware definition, the peripherals in use and their driver load times, the Ethernet interface not being connected and active, as well as pre-installed applications load time. Avnet's PetaLinux 2016.2 Out-of-Box design contains items that load at boot time that may not exist in end-user applications. It is expected that the load times for Avnet's Out-of-Box design can be decreased depending on the end-user optimizing their Linux environment.

The Zynq UltraScale+ MPSoC has many configuration options; The UltraZed-EG SOM uses this configuration:

- VCCO_0 does not require a rail as it has an internal 1.8V.
- PUDC_B can be pulled high or low on the UltraZed-EG SOM. This active-low input enables internal pull-ups during configuration on all SelectIO pins. By default, the resistor jumper is populated with a 1K resistor in the 1-2 position, which pulls up PUDC_B and disables the pull-ups during configuration.
- PS_INIT_B is pulled high via a 4.7KΩ resistor.
- PS_PROG_B is pulled high via a 4.7KΩ resistor with activation control through a push button.

The PS is responsible for configuring the PL. The Zynq UltraScale+ MPSoC will not automatically reconfigure the PL as in standard FPGAs by toggling PROG. Likewise, it is not possible to hold off Zynq boot up with INIT_B as this is done with PS_POR_B. If the application needs to reconfigure the PL, the software design must do this, or you can toggle the PS_POR_B to restart everything. When PL configuration is complete a blue DONE LED will illuminate.

2.14.1 JTAG Connections

The UltraZed-EG SOM requires an external JTAG cable connector populated on the carrier card for JTAG operations. JTAG signals are routed from Bank 503 of the Zynq UltraScale+ MPSoC to the Micro Header JX1. The following table shows the JTAG signal connections between the Zynq and the Micro Header.

The Zynq UltraScale+ MPSoC Bank 503 reference voltage, +VCCO_PSIO, is connected to 1.8V. The JTAG VREF on the end-user carrier card should be connected to 1.8V to ensure compatibility between the interfaces. For reference, see the UltraZed-EG IOCC carrier card schematics.

MPSoC Pin #	UltraZed-EG SOM Net Name	JX1 Pin #
K16	JTAG_TCK	1
L18	JTAG_TMS	2
L17	JTAG_TDO	3
L15	JTAG_TDI	4

Table 30 – UltraZed-EG SOM JTAG Connections

NOTE: JTAG 4.7-kΩ Pull-ups will exist on the end-user carrier card. Also, JTAG series termination resistors will exist on the end-user carrier card if required

NOTE: Further documentation on the pull-ups and series terminations will exist in the UltraZed Carrier Card Design Guide

2.15 Power Supplies

2.15.1 Voltage Rails and Sources

The UltraZed-EG SOM is powered through the Micro Header connection between itself and the end-user carrier card.

There are five regulators that reside on the UltraZed-EG SOM that provide 0.85V, 1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V and 0.6V power rails. These voltages are used to power the peripheral devices as well as the UltraZed-EG SOM. Most of these regulators are powered from the end-user carrier card via the **+VIN** pins on the Micro Headers and are expected to carry +5V or +12V to the UltraZed-EG SOM regulator inputs.

There are also four bank voltages that are supplied from the end-user carrier card to the UltraZed-EG SOM. Bank 26 (**+VCCO_HD_26**), Bank 64 (**+VCCO_HP_64**), Bank 65 (**+VCCO_HP_65**), and Bank 66 (**+VCCO_HP_66**) voltages are generated on the end-user carrier card and connected to the UltraZed-EG SOM via the Micro Headers. The voltage at which these banks operate is up to the end-user carrier card design as all I/O that connect to these banks is exclusive to the Micro Headers (no on-board device is connected to these banks).

The diagram below shows a high level depiction of the power provided by the end-user carrier card through the Micro Headers as well as the regulators that exist on the UltraZed-EG SOM.

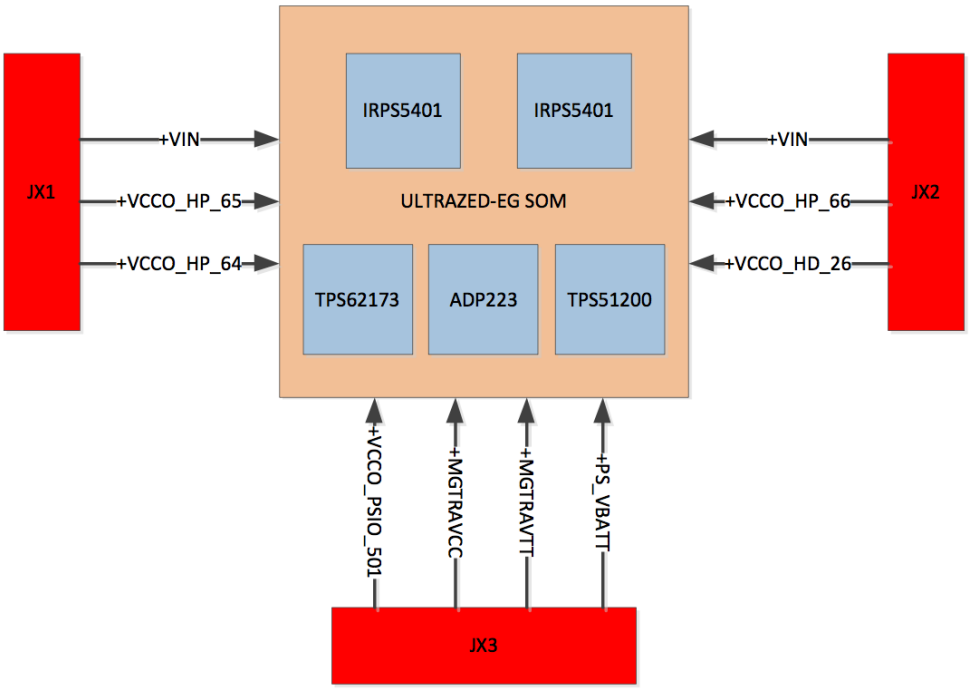


Figure 13 – UltraZed-EG SOM Power Solution

The table below shows the various voltage rails names on the schematic, the associated voltage for each rail, where they are connected on the Zynq UltraScale+ MPSoC, and where the voltage originates from.

Schematic Voltage Name	Voltage Level	Zynq Connection	Voltage Origination
+5VREG	5.0V	N/A	UltraZed-EG SOM
+2.5V	2.5V		
+DDR4_VREF	1.2V		
+1.0V	1.0V		
+DDR4_VTT	0.6V		
+VCCO_PSIO	1.8V	VCCO_PSIO0_500	
		VCCO_PSIO2_502	
		VCCO_PSIO3_503	
		VCC_PSADC	
		VCC_PSAUX	
+VCCAUX	1.8V	VCCAUX	
		VCCAUX_IO	
		VCCADC	
+VCC_PSINTLP	0.85V	VCC_PSINTLP	
+VCC_PSINTFP	0.85V	VCC_PSINTFP	
		VCC_PSINTFP_DDR	
+VCC_PSPLL	1.2V	VCC_PSPLL	
+VCCO_PSDDR_504	1.2V	VCCO_PSDDR_504	
+VCCINT_IO	0.85V	VCCBRAM	
		VCCINT_IO	
+3.3V	3.3V	N/A	
+VCCINT	0.85V	VCCINT	
+VCC_PSDDR_PLL	1.8V	VCC_PSDDR_PLL	
+VIN	5V or 12V	N/A	JX1 / JX2
+VCCO_HP_64	1.0V to 1.8V	VCCO_64 (Bank 64)	JX1
+VCCO_HP_65	1.0V to 1.8V	VCCO_65 (Bank 65)	JX1
+VCCO_HP_66	1.0V to 1.8V	VCCO_66 (Bank 66)	JX2
+VCCO_HD_26	1.2V to 3.3V	VCCO_26 (Bank 26)	JX2
+VCCO_PSIO_501	1.8V to 3.3V	VCCO_PSIO1_501	JX3
+MGTRAVCC	0.85V	PS_MGTRAVCC	JX3
+MGTRAVTT	1.8V	PS_MGTRAVTT	JX3
+PS_VBATT	1.5V	VCC_PSBATT	JX3

Table 31 – UltraZed-EG SOM Voltage Rails

2.15.2 Voltage Regulators

The following block diagram contains the on-board power solution for the UltraZed-EG SOM.

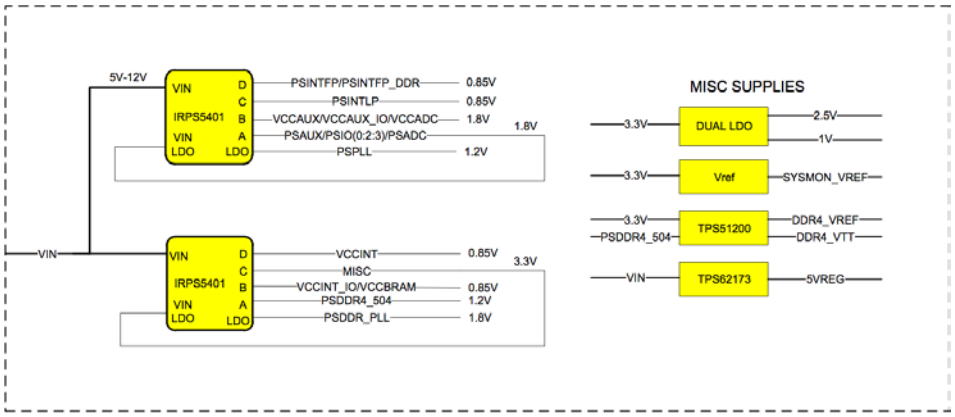


Figure 14 – On-Board Regulation Circuits

The POWER GOOD output of the +3.3V rail is used to ENABLE the DDR termination regulator and the ADP223 regulator completing the power sequence. These two supplies are the last regulators to be brought up.

The UltraZed-EG SOM provides a power good signal to the end-user carrier card to signal that the SOM power sequencing has completed and the end-fuser carrier card is free to bring up the VCCO supplies. This signal is called SOM_PG_OUT and is tied to JX2.Pin 41. SOM_PG_OUT on the Micro Headers serves to gate the power supplies for Bank 501, Bank 26, Bank 64, Bank 65, Bank 66, MGTRAVCC, and MGTRAVTT on the end-user carrier card.

NOTE: SOM_PG_OUT is provided by the power good output of the DDR termination regulator.

The table below shows the maximum output current for each regulator on the UltraZed-EG SOM. Also listed in the table below are the supported power modes and whether or not the rail is to remain active during the power mode that the UltraZed-EG SOM is being operated in.

Voltage Rail	Voltage (V)	Max Current (A)	Power Domain	Power Modes		
				Full Power	PS Only	PS Low Power
+5VREG	5.0V	0.5A	N/A	Y	Y	Y
+2.5V	2.5V	0.3A	N/A	Y	Y	Y
+DDR4_VREF	1.2V	0.04A	N/A	Y	Y	Y
+1.0V	1.0V	0.3A	N/A	Y	Y	Y
+DDR4_VTT	0.6V	5.5A	N/A	Y	Y	Y
+VCCO_PSIO	1.8V	0.5A *	PS LP	Y	Y	Y
+VCCAUX	1.8V	1.1A *	PL	Y	N	N
+VCC_PSINTLP	0.85V	0.6A *	PS LP	Y	Y	Y
+VCC_PSINTFP	0.85V	3.7A *	PS FP	Y	Y	N
+VCC_PSPLL	1.2V	0.2A *	PS LP	Y	Y	Y
+VCCO_PSDDR_504	1.2V	1.2A *	PS LP	Y	Y	N
+VCCINT_IO	0.85V	0.6A *	PL	Y	N	N
+3.3V	3.3V	1.0A *	N/A	Y	Y	Y
+VCCINT	0.85V	4.0A *	PL	Y	N	N
+VCC_PSDDR_PLL	1.8V	0.5A *	PS FP	Y	Y	N
+VIN	5V or 12V	-	N/A	Y	Y	Y
+VCCO_HP_64	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HP_65	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HP_66	1.0V to 1.8V	1.5A **	PL	Y	N	N
+VCCO_HD_26	1.2V to 3.3V	1.5A **	PL	Y	N	N
+VCCO_PSIO_501	1.8V to 3.3V	0.5A **	PS LP	Y	Y	Y
+MGTRAVCC	0.85V	1.5A **	PS FP	Y	Y	N
+MGTRAVTT	1.8V	1.0A **	PS FP	Y	Y	N
+PS_VBATT	1.5V	0.5A *	N/A	Y	Y	Y

Table 32 – Voltage Rails Max Current and Power Modes

** Max Current Derived using Preliminary Xilinx Power Estimator Tools (On-Board)*
*** Max Current Derived using Micro Header Pin Current Carrying Capacity (Carrier Card)*

2.15.3 Power Supply Sequencing and Power Modes

Sequencing for the power supplies follows the recommendations for the Zynq UltraScale+ device. The power configuration programmed into the International Rectifier IRPS5401MTRPBF devices controls the power supply sequencing. An end-user may utilized the PMBUS on the carrier-card or utilize the Zynq UltraScale+ MPSoC interface to the PMBUS to power down individual rails to implement the different power modes supported by the MPSoC.

Sequencing is needed for board power up, as well as entering and exiting different power modes. There are 3 power domains, PS LP (Processing Subsystem Low Power), PS FP (Processing Subsystem Full Power) and PL (Programmable Logic Power). The PS LP domain shall come up first followed by the PS FP and PL power domains.

PS LP Power Domain Sequence:

DS295 (V1.1) Recommended:

VCC_PSINTLP → VCC_PSAUX, VCC_PSADC, VCC_PSPLL → VCCO_PSIO

UltraZed-EG SOM Implementation:

VCC_PSINTLP → VCCO_PSIO / VCC_PSPLL → VCCO_PSIO_501

PS FP Power Domain Sequence:

DS295 (V1.1) Recommended:

VCC_PSINTFP, VCC_PSINTFP_DDR → VPS_MGTRAVCC, VCC_PSDDR_PLL → VPS_MGTRAVTT, VCCO_PSDDR

UltraZed-EG SOM Implementation:

VCC_PSINTFP → MGTRAVCC / VCC_PSDDR_PLL → MGTAVTT / VCCO_PSDDR4_504

PL Power Domain Sequence:

DS295 (V1.1) Recommended:

VCCINT → VCCINT_IO, VCCBRAM → VCCAUX, VCCAUX_IO → VCCO_HD_26 / VCCO_HP_64 / VCCO_HP_65 / VCCO_HP_66

UltraZed-EG SOM Implementation:

VCCINT → VCCINT_IO → VCCAUX → VCCO_HD_26 / VCCO_HP_64 / VCCO_HP_65 / VCCO_HP_66

Entering / Exiting Power Domains:

To enter power down modes, the reverse order of start-up should be followed (last supply to come up should be the first to be shut down, etc.). The PL and PS FP domains can be powered down independently and either can be powered down before or after the other. When shutting down power to a domain however, sequencing must be followed in relation to the specific power domain group. Upon repowering these domains, proper sequencing should again be followed.

The following diagrams are indicative of the pre-programmed power-on and power-off sequences that exist on the UltraZed-EG SOM and the UltraZed IO Carrier Card.

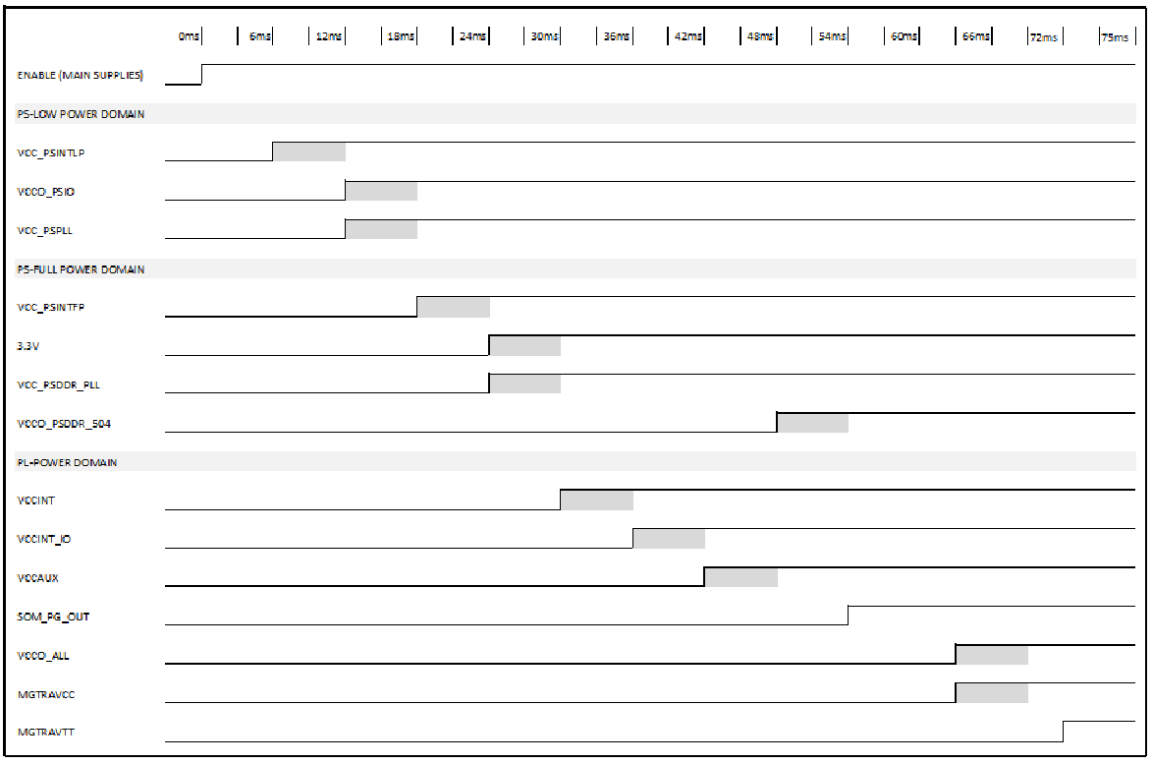


Figure 15 – UltraZed Power-On Sequence

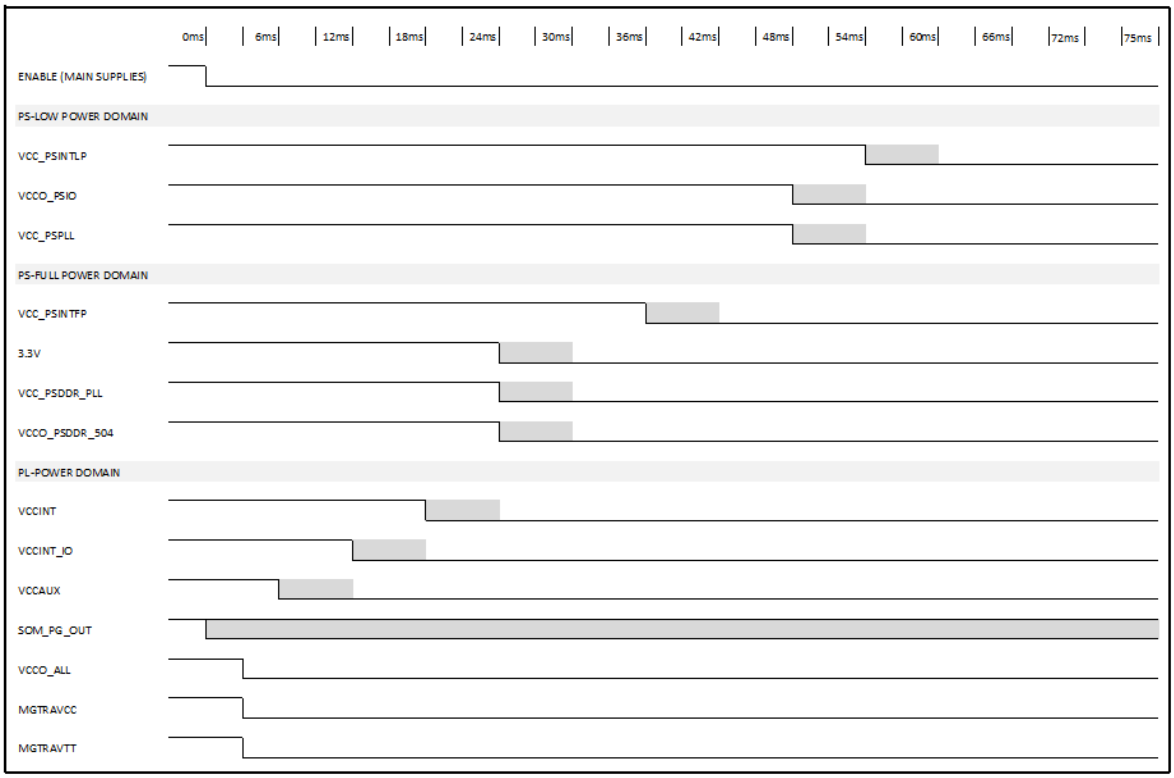


Figure 16 – UltraZed Power-Off Sequence

The following diagram illustrates the power-up flow with an end-user carrier card:

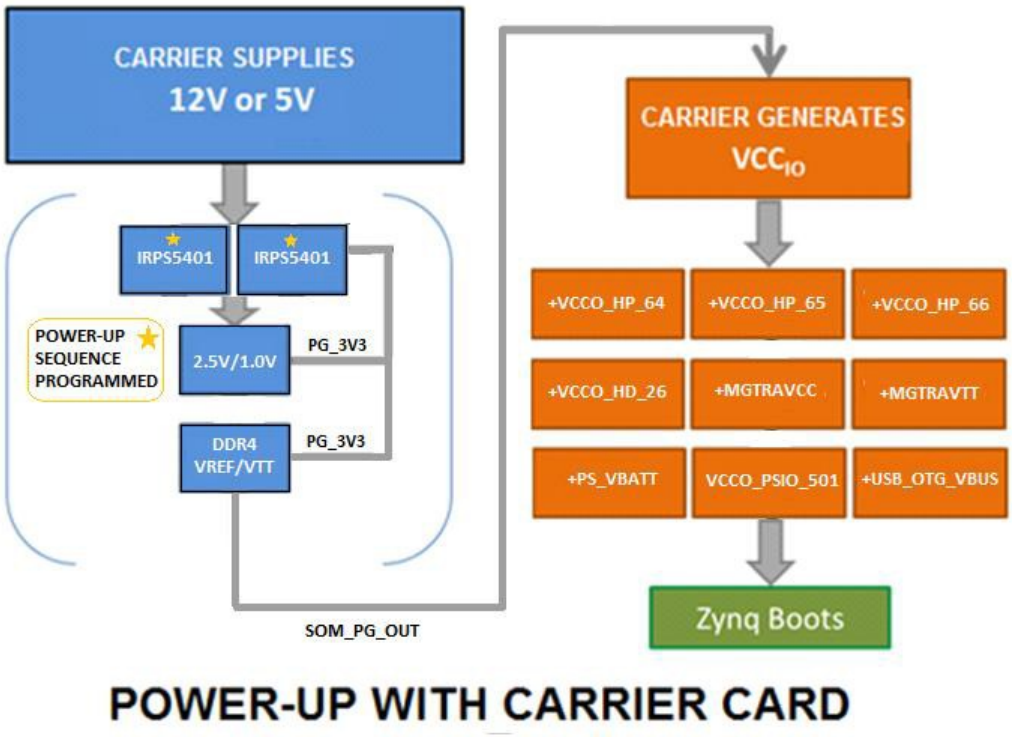


Figure 17 – Power-Up Flow with Carrier Card

2.15.4 PCB Bypass / Decoupling Strategy

The UltraZed-EG SOM design follows at a minimum the PCB decoupling strategy as outlined in UG583 for the Zynq UltraScale+ MPSoC in the SFVA625 package.

NOTE: These quantities are considered preliminary and subject to change because power and package modelling is still in progress at Xilinx. A review of these requirements is required as this design moves from engineering silicon to production silicon.

Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations

	V_{CCINT}/V_{CCINT_IO}			V_{CCBRAM}		V_{CCAUX}/V_{CCAUX_IO}		HRIO	HPIO
	680 µF	100 µF	4.7 µF	47 µF	4.7 µF	47 µF	4.7 µF	47 µF	47 µF
XCZU3EG-SBVA625	1	1	1	1	1	1	2	1	1

Zynq UltraScale+ MPSoC PS Decoupling Capacitor Recommendations

VCC_PSINTLP		VCC_PSINTFP		VCC_PSAUX		VCC_PSPLL		PS_MGTRAVCC	PS_MGTRAVTT	VCC_PSINTFP_DDR		VCCO_PSIOx (Each)		VCC_PSBATT	
100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	4.7 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 18 – PCB Decoupling Capacitor Requirements

2.15.5 Power Estimation

Since the total power consumption of the system heavily depends on many factors with regard to the configuration/utilization of the Zynq UltraScale+ MPSoC device, it is highly recommended that the end user perform some power estimation and analysis using the Xilinx Power Estimator (XPE). This tool is very useful for plugging in various parameters and getting an estimated power consumption estimate for the system.

When designing the UltraZed-EG SOM architecture, the XPE tool was used to ensure that the UltraZed-EG SOM system could supply enough power to the Zynq UltraScale+ and its on-board peripherals using worst case parameters including logic utilization, operating frequency and temperature while still supporting low power modes and various speed grade options.

Since the power supply for the VCCIO rails for banks 26, 64, 65 and 66 are supplied from the end-user carrier card, it is important to make sure that the end-user carrier card power supplies are adequate to power these rails over the desired and/or estimated operating scenario.

NOTE: When designing a custom UltraZed-EG carrier board, be sure to use XPE (Xilinx Power Estimator) to estimate the power needed by the Zynq UltraScale+ MPSoC device. The designer will need this figure in sizing the input supply to the UltraZed-EG SOM.

NOTE: In addition to the XPE results for the Zynq UltraScale+ MPSoC, the end user will need to add to their power estimate to compensate for the power that is needed for the on-board devices that exist on the UltraZed-EG SOM such as the various memory, USB and Ethernet PHY devices, and serial devices.

2.15.6 System Monitor (SYSMON)

The Zynq UltraScale+ Architecture supports an on-chip system monitor. SYSMON monitors the physical environment via on-chip temperature and supply sensors with integrated analog-to-digital converters (ADC). An overview of the System Monitor primitive, SYSMON, is provided by Xilinx User Guide **UG580 – UltraScale Architecture System Monitor**.

The UltraZed-EG SOM supports System Monitor functionality thru the JX connectors to a SYSMON header that would be implemented on the end-user carrier card. The UltraZed-EG SOM contains selectable reference voltages via a 0-ohm resistor jumper. The following figure depicts the implementation of the system monitor on the UltraZed-EG SOM.

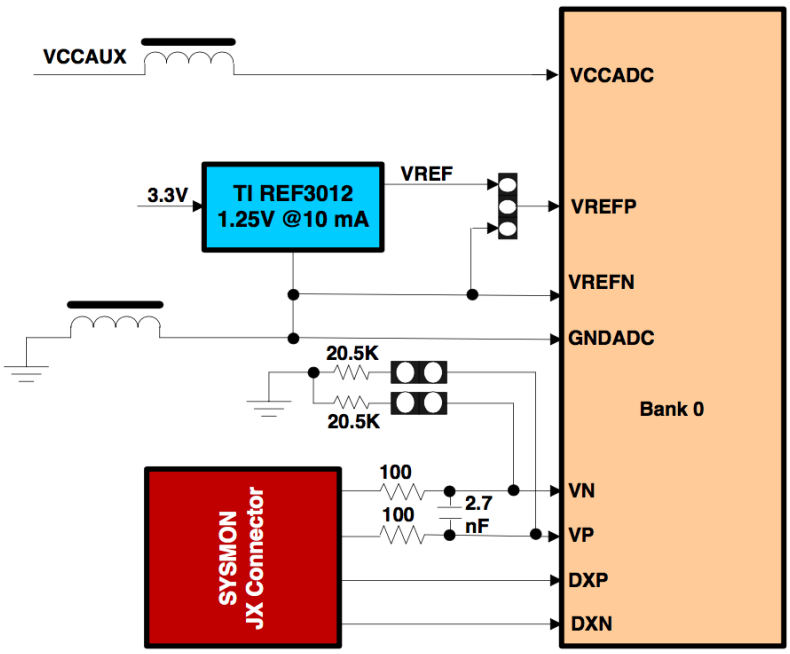


Figure 19 – UltraZed-EG SOM SYSMON Circuit

The following table shows the SYSMON interface connections to the JX2 connectors. Note: The SYSMON header is to be implemented on the end-user carrier card.

MPSoC Pin #	UltraZed-EG SOM Net Name	JX2 Pin #
P12	SYSMON_V_N	1
N13	SYSMON_V_P	2
R12	SYSMON_DX_N	3
R13	SYSMON_DX_P	4

Table 33 – UltraZed-EG SOM SYSMON Connections

2.15.7 Battery Backup – Device Secure Boot Encryption Key

The Zynq UltraScale+ MPSoC power rail +PS_VBATT is a 1.2V to 1.5V voltage typically supplied by a battery. This supply is typically used to maintain an encryption key in battery-backed RAM for device secure boot. The encryption key can alternatively be stored in eFuse which does not require a battery.

On the UltraZed-EG SOM, +PS_VBATT is interfaced to the JX3 connector relying on the end-user carrier card to properly implement the battery functionality. To apply an external battery to Zynq UltraScale+ MPSoC from the end-user carrier card the proper voltage should be applied to the +PS_VBATT pin on the JX3 connector, JX3-PIN 46.

MIO Name	Package Pin Number	Net Name	JX3 Connector
VCC_PSBATT	N19	+PS_VBATT	JX3.46

Table 34 – UltraZed-EG SOM +PS_VBATT Connection

NOTE: When the final solution does not require battery backup, the end-user carrier card should tie the +PS_VBATT pin to the appropriate voltage range from +1.2V to +1.5V.

2.15.8 Thermal Management: Heatsink and Fan Assembly

Depending on the end-user application, the performance of the UltraZed-EG SOM will require a thermal solution to help maintain performance across temperature.

The UltraZed-EG SOM comes populated with an example thermal solution of a 19.05mm Heatsink and Fan assembly (Heatsink + Fan + Hardware Height). This active arrangement is secured directly to the Zynq UltraScale+ MPSoC via 3M thermal tape. A Cool Innovations Heat Sink (PN: **3-101002UBFA**) and a Sunon 5V DC Fan (PN: **MC25100V1-000U-A99**) are assembled and shipped with the UltraZed-EG SOM.

The active heat sink is powered by connecting a three position connector to the 5V fan mating connector on an end-user carrier card. This 3-pin keyed connector is .100" pitch and has the 5V conductor as pin 2 on the connector. For reference, the fan supplied with the UltraZed-EG SOM mates with the fan header on the UltraZed IO Carrier Card.

Under most circumstances this 19.05mm Heatsink and Fan assembly should provide adequate relief across temperature, but it cannot be guaranteed to support all environmental conditions due to lack of knowledge regarding end-users thermal environment and the possible enclosure of the UltraZed-EG SOM. For aggressive applications it is recommended that an accurate worst-case power analysis be performed in order to avoid the pitfalls of over designing or under designing your product's power and thermal management system.

NOTE: End users should design a custom Heatsink and Fan assembly that is more conducive to the requirements of their system including alternative mounting techniques for the assembly which could enhance the thermal reliability of the system.

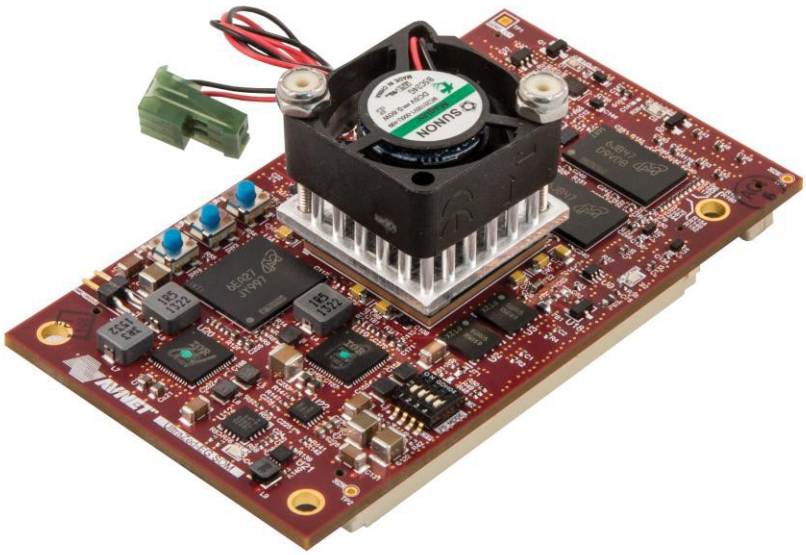


Figure 20 – UltraZed-SOM with 19.05mm 5VDC Heatsink and Fan Assembly

3 Zynq UltraScale+ MPSoC I/O Bank Allocation

3.1 PS MIO Bank Allocation

There are 78 I/O available in the PS MIO Banks. The tables below lists the number of required I/O per peripheral and the MIO locations where the interface exists.

Interface	I/O Required	MIO
QSPI FLASH	12	0-5, 7-12
USB	12	52-63
ETHERNET	14	64-77
eMMC	10	13-22
I2C	2	24-25
TOTAL	**50**	

Table 35 – PS MIO Bank Interface Requirements

The General Purpose I/O assignments aren't specifically defined interfaces such as those that are defined in Table 32. The table below provides the MIO locations of the PS MIO general purpose pins and also MIO pins that support other functions.

Interface	I/O Required	MIO
QSPI FB CLK	1	6
MIO23_INT_N	1	23
General Purpose PS MIO	26	26-77
TOTAL	**28**	

Table 36 – PS MIO Bank Interface Requirements

The end-user is encouraged to utilize the Zynq UltraScale+ MPSoC TRM in defining the MIO peripheral mappings that they would like to utilize on a custom UltraZed Carrier Card.

3.2 Zynq UltraScale+ MPSoC Bank Voltages

The I/O bank voltage assignments are shown in the table below.

Bank	Voltage (default)	Source
PS-Side		
MIO Bank 500	+VCCO_PSIO (1.8V)	SOM
MIO Bank 501	+VCCO_PSIO_501 (ADJ)	Carrier Card
MIO Bank 502	+VCCO_PSIO (1.8V)	SOM
MIO Bank 503	+VCCO_PSIO (1.8V)	SOM
MIO Bank 504	+VCCO_PSDDR4_504 (1.2V)	SOM
MIO Bank 505	+MGTRAVCC / +MGTRAVTT	Carrier Card
PL-Side		
Bank 0	1.8V (Internal)	Zynq UltraScale+
Bank 26	+VCCO_HD_26 (ADJ)	Carrier Card
Bank 64	+VCCO_HP_64 (ADJ)	Carrier Card
Bank 65	+VCCO_HP_65 (ADJ)	Carrier Card
Bank 66	+VCCO_HP_66 (ADJ)	Carrier Card

Table 37– Zynq Bank Voltage Assignments

PL I/O Banks 26, 64, 65, and 66 are powered from the end-user carrier card. These bank supplies are designed to be independent on the UltraZed-EG SOM. Maximum flexibility is allowed to the designer for these banks as the voltage level and standards are left to the end-user carrier card design. The designer of the end-user carrier card VCCO supplies is provided the choice of whether the IO banks use a shared voltage supply or independent voltage supplies.

When designing a customer end-user carrier card, please review the Zynq UltraScale+ MPSoC data sheet for the appropriate supported bank voltages and tolerances.

4 Specifications and Ratings

This section contains the absolute maximum and the recommended operating ranges for SOM temperature, supply voltages, and I/O voltages. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

4.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes	Reference Document
Storage Temperature	-40	85	°C		

Table 38 – Absolute Maximum Temperature Rating

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
VIN	-0.3	16.0	V		UltraZed-EG Designer's Guide
*Sense	-	-	V	Voltage Sense outputs- Do not drive from carrier	
Xilinx Zynq UltraScale+					
+PS_VBAT	-0.5	2.0	V	VCC_PSBATT – supply for battery backed BRAM and RTC	Xilinx Datasheet DS925
+VCCO_PSIO_501	-0.5	3.63	V	Supply voltage for PS MIO bank 501	
+VCCO_HD_26	-0.5	3.4	V	PL supply voltage for HD I/O bank 26	
+VCCO_HP_*	-0.5	2.0	V	PL supply voltages for HP I/O banks 64, 65, 66	
+MGTRAVCC	-0.5	1.0	V	PS-GTR supply voltage	
+MGTRAVTT	-0.5	2.0	V	PS-GTR termination voltage	
Peripheral Devices					
USB_VBUS_OTG	-0.5	6.0	V	Resistor required on carrier	Microchip Datasheet USB3320

Table 39 – Absolute Maximum Ratings for Supply Voltages

Parameter	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking					
SOM_RESET_IN_N	-0.5	6.5	V		UltraZed-EG Designer's Guide
CC_RESET_OUT_N	0	50	V	This is an open-drain output with no pullup on the SOM	
SOM_PG_OUT	-0.3	N/A	V	Open-drain signal. Do not drive high by the carrier	
PMBus_ALERT_N	-0.3	5.3	V	Open-drain output from SOM with 2 KΩ pull-up to 3.3V on the SOM	
PMBus_SCL	-0.3	5.3	V		
PMBus_SDA	-0.3	5.3	V		
CC_INT_N	-0.5	7.0	V		
CC_SDA	-0.5	7.0	V		
CC_SCL	-0.5	7.0	V		
Xilinx Zynq UltraScale+					
SYSMON*	-0.5	2.35	V	Bank0	Xilinx Datasheet DS925
JTAG_*	-0.5	2.35	V	Bank 503	
JX1_HP_DP_[00:23]*	-0.5	+VCCO_HP_64 + 0.55	V	Bank 64	
JX1_HP_DP_[24:41]*	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
JX1_HP_SE_[00:03]	-0.5	+VCCO_HP_64 + 0.55	V	Bank 64	
JX1_HP_SE_[04:05]	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
JX2_HP_DP_[00:23]*	-0.5	+VCCO_HP_66 + 0.55	V	Bank 66	
JX2_HP_DP_[24:29]*	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
JX2_HD_SE_[00:11]*	-0.5	+VCCO_HD_26 + 0.55	V	Bank 26	
JX2_HP_SE_[00:03]	-0.5	+VCCO_HP_66 + 0.55	V	Bank 66	
JX2_HP_SE_[04:05]	-0.5	+VCCO_HP_65 + 0.55	V	Bank 65	
MIO*	-0.5	+VCCO_PSIO_501 + 0.55	V	Bank 501	
GTR_TX*/GTR_RX*	-0.5	1.2	V	Bank 505	
GTR_REFCLK*	-	-	V	AC coupled. Bank 505	
Peripheral Devices					
ETH_MD*	-0.3	6.5	V		DP83867 Datasheet
ETH_PHY_LED*	-0.3	2.1	V		
USB_ID	-0.5	6.0	V		Microchip Datasheet USB3320
USB_OTG*	-0.5	6.0	V		
USB_OTG_CPEN	-0.5	6.0	V		

Table 40 – Absolute Maximum Ratings for I/O Voltages

4.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
C-Grade SOM	0	70	°C	Zynq UltraScale+ Tj < 100°C Micron DDR4 Tc < 95°C USB3320 Tj < 100°C	Xilinx Datasheet DS925 Micron Datasheet Microchip Datasheet USB3320
I-Grade SOM	-40	85	°C	Zynq UltraScale+ Tj < 100°C Micron DDR4 Tc < 95°C[1] USB3320 Tj < 100°C.	

Table 41 – Recommended Ambient Operating Temperature

Parameter	Min	Max	Units	Notes	Reference Document
SOM					
VIN	5.0	12.0	V		UltraZed-EG Designer's Guide
*Sense	-	-	V	Voltage Sense outputs- Do not drive from carrier	
Xilinx Zynq UltraScale+					
+PS_VBAT	1.2	1.5	V	VCC_PSBATT – supply for battery backed BRAM and RTC	Xilinx Datasheet DS925
+VCCO_PSIO_501	1.71	3.465	V	Supply voltage for PS MIO bank 501	
+VCCO_HD_26	1.14	3.4	V	PL supply voltage for HD I/O bank 26	
+VCCO_HP_*	0.95	1.9	V	PL supply voltages for HP I/O banks 64, 65, 66	
+MGTRAVCC	0.825	0.875	V	PS-GTR supply voltage	
+MGTRAVTT	1.746	1.854	V	PS-GTR termination voltage	
Peripheral Devices					
USB_VBUS_OTG	0	5.5	V	Resistor required on carrier	Microchip Datasheet USB3320

Table 42 – Recommended Supply Voltages

[1] Enable temperature-controlled refresh mode if T_c exceeds 85°C.

Parameter	Dir[2]	Min	Max	Units	Notes	Reference Document
SOM Control / Handshaking						
SOM_RESET_IN_N	I	0	+VCCO_PSIO_501	V	This signal has a 10KΩ pullup to +VCCO_PSIO on the SOM	
CC_RESET_OUT_N	Open-drain	0	3.3	V	This is an open-drain output with no pullup on the SOM	
SOM_PG_OUT	Open-drain	0	N/A	V	This is an open-drain signal with 10KΩ pull-up to 3.3V on the SOM. Do not drive high from the carrier	
PMBus_ALERT_N	O	0	4.0	V	Open-drain output from SOM with 2 KΩ pull-up to 3.3V on the SOM	UltraZed-EG Designer's Guide
PMBus_SCL	IO	0	3.3	V	2 KΩ pull-up to 3.3V on the SOM if JP3 installed	
PMBus_SDA	IO	0	3.3	V	2 KΩ pull-up to 3.3V on the SOM if JP2 installed	
CC_INT_N	I	0	3.0	V	Pull up to 1.8V, 2.5V, or 3.3V on carrier card	
CC_SDA	IO	0	5.5	V		
CC_SCL	O	0	5.5	V	Open-drain output. Pull up to 1.8V, 2.5V, or 3.3V on carrier card	
Xilinx Zynq UltraScale+						
JTAG_TCK	I	-0.2	2.0	V		
JTAG_TDI	I	-0.2	2.0	V	Bank 503 I/O voltage set to 1.8V on SOM	
JTAG_TDO	O	0	1.8	V		
JTAG_TMS	I	-0.2	2.0	V		
SYSMON*	I	See System Monitor Guide UG580			VCC_PSADC set to 1.8V on SOM	
JX1_HP_DP_[00:23]*	IO	-0.2	+VCCO_HP_64 + 0.2	V	Bank 64 I/O voltage set by carrier	
JX1_HP_DP_[24:41]*	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	Xilinx Datasheet DS925
JX1_HP_SE_[00:03]	IO	-0.2	+VCCO_HP_64 + 0.2	V	Bank 64 I/O voltage set by carrier	
JX1_HP_SE_[04:05]	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	
JX2_HP_DP_[00:23]*	IO	-0.2	+VCCO_HP_66 + 0.2	V	Bank 66 I/O voltage set by carrier	Xilinx System Monitor Guide UG580
JX2_HP_DP_[24:29]*	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	
JX2_HD_SE_[00:11]*	IO	-0.2	+VCCO_HD_26 + 0.2	V	Bank 26 I/O voltage set by carrier	
JX2_HP_SE_[00:03]	IO	-0.2	+VCCO_HP_66 + 0.2	V	Bank 66 I/O voltage set by carrier	
JX2_HP_SE_[04:05]	IO	-0.2	+VCCO_HP_65 + 0.2	V	Bank 65 I/O voltage set by carrier	
MIO*	IO	-0.2	+VCCO_PSIO_501 + 0.2	V	Bank 501 I/O voltage set by carrier	
GTR_TX*/GTR_RX*	IO	0.075	+MGTRAVCC	V	Bank 505 I/O voltage set by carrier	
GTR_REFCLK*	IO	0.25	2.0	V	AC coupled. Bank 505 I/O voltage set by carrier	
Peripheral Devices						
ETH_MD*	IO	See DP83867 Datasheet and UltraZed-EG Designer's Guide for details				DP83867 Datasheet
ETH_PHY_LED	O					
USB_ID	I	0	3.3	V		Microchip Datasheet USB3320
USB_OTG*	IO	0	3.3	V	DM/DP on USB3320	
USB_OTG_CPEN	O	0	3.3	V	External 5V supply enable	

Table 43 – Recommended I/O Voltages

[2] "Dir" is the Direction of the signal relative to the SOM. For example, SOM_RESET_IN_N is listed as "I" which is Input to the SOM; therefore, this signal is an output from the Carrier.

5 Mechanical

The UltraZed-EG SOM measures 2.00” x 3.50” (50.80 mm x 88.9 mm).

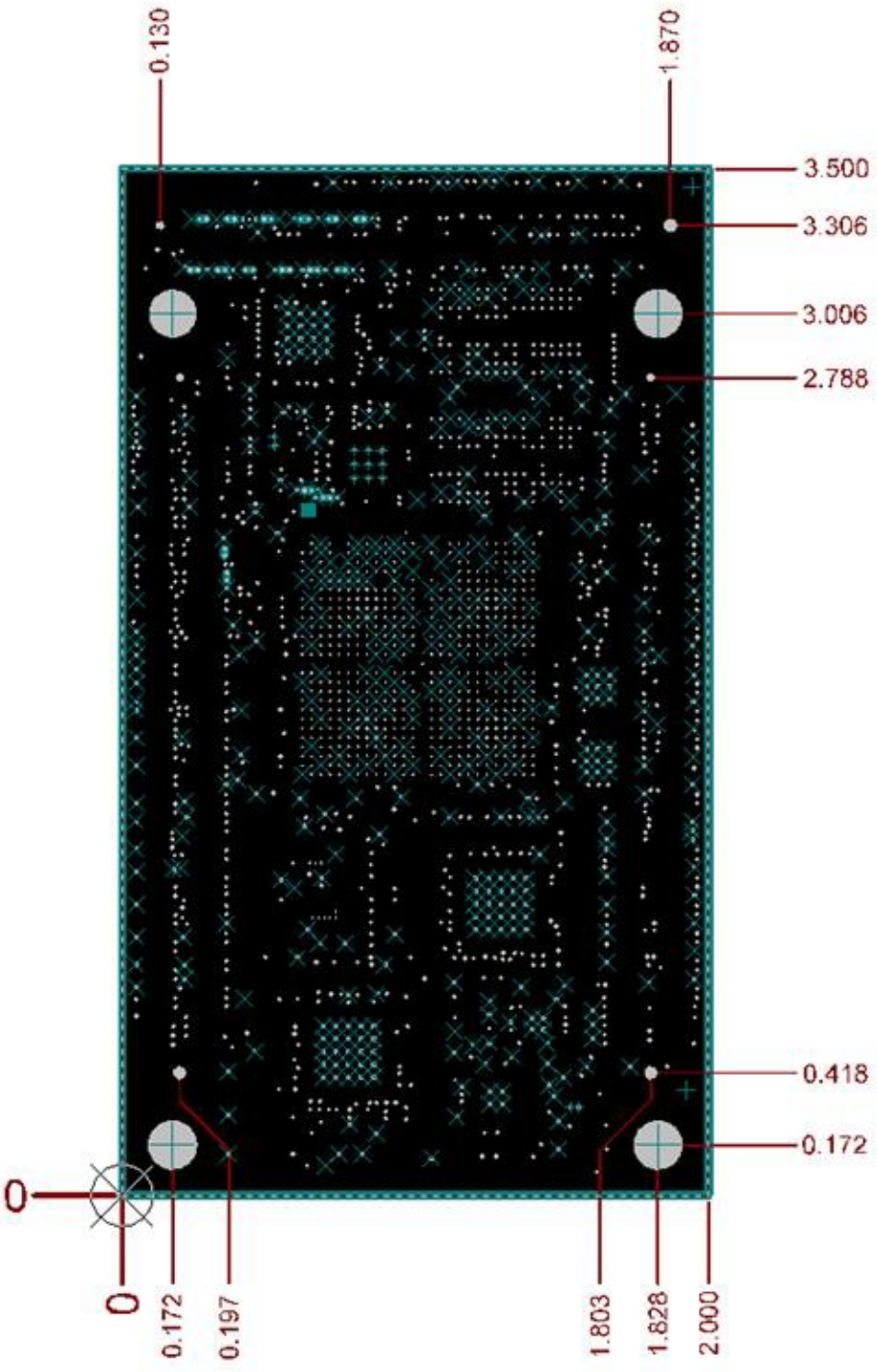


Figure 21 – UltraZed-EG SOM Top View Mechanical Dimensions

The UltraZed-EG SOM has a maximum vertical dimension of 0.487” (12.38 mm).

Figure 22 – UltraZed-EG SOM Side View Mechanical Dimensions

The UltraZed-EG SOM is populated with an active fan and heatsink combination that has a maximum vertical dimension of 1.750” (44.45 mm). The Heatsink is available in many other sizes, but the minimum vertical dimension of the fan and heatsink combination using the smallest heatsink is 0.750” (19.05 mm).

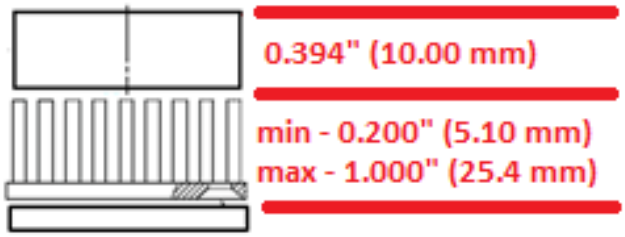


Figure 23 – UltraZed-EG SOM Fan and Heatsink Vertical Dimensions

NOTE: The above figure does not show the additional hardware required to attach the fan to the heatsink. This additional hardware coincides with approximately 0.156-inches (3.96mm) of additional height for the nut and screw.

The heatsink delivered with the UltraZed-EG SOM has a height of 0.200-inches. When combined with the fan and associated nuts and bolts, the height of the heatsink and fan assembly is approximately 19.05mm which approaches 0.750-inches in additional overall height.