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An insight into Nexperia Power GaN technology – Applications, quality, reliability and scalability

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Document information

Information	Content
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Abstract	In this paper we have concentrated on the Power GaN product and technology robustness, quality, reliability and volume manufacturability based on GaN on Si base material. We report here on the product robustness from applications and parametric point of view and qualification testing results of latest generation 650V GaN FETs qualified in accordance with AEC-Q101 standard. Devices offer rated operating temperature of -55°C to +175°C and this family comes with robust gate with high threshold voltage which provides a high safety margin against gate-source transients. Some of the tests are performed beyond AEC-Q101 requirements

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1. Introduction

Most efficient power conversion requires best semiconductor devices as the fundamental building block. Power GaN technology offers best possible efficiency. Proving performance is not in question for those closely following the Power GaN technology for its performance demonstration in different applications. Providing robustness of the products in operation, quality, reliability of the technology and the scalability uptake in manufacturing are yet to prove. Power GaN technology is full of challenges. In RF applications they are already successful but in high current high power applications in high voltage, volume manufacturers need to address these challenges to satisfaction. In this paper we'd like to share product robustness for applications, quality and reliability at high voltage and high temperatures, for the Power GaN technology.

Nexperia Power GaN technology focuses on high power applications like AC/DC, PFC, OBC, DC/DC and Traction Inverters within 650V-900V for Automotive, Telecom, Server, storage, data centres and industrial market sectors

WBG materials with higher critical electric field and higher mobility together give lowest R_{DSon} (source drain on state resistance) for higher voltages and significantly better switching FOM (Figure of Merit). WBG devices as beginning to enter the market shows significant promise and takes away many limitations naturally imposed by Si IGBT and Si SJ devices. Some of the hard switched application topologies where Si SJ FETs cannot be used due to the diode reverse recovery can easily use Power GaN FETs and take full advantage of reduced components count and higher efficiency with simpler control schemes.

GaN HEMT (High Electron Mobility Transistor) works with the formation of 2DEG (2 Dimensional Electron Gas) due to the spontaneous polarisation and piezoelectric polarisation combined at the interface of GaN and $Al_xGa_{1-x}N$. Epi is formed on Si substrate via seed layer and a graded layer of GaN and AlGaN layers before the pure GaN layer is grown and thin layer of AlGaN then forms the 2DEG. Electron mobility in this layer is very high hence the name.

Current Power GaN FETs are of two main flavour: E-mode or single die normally off device, and D-mode or two die normally off device. Stability and leakage current of the E-mode gates are of concern but two die normally off or cascode configuration currently gives peace of mind as the driving of these FETs are simple and robust. E-mode device drive is complex, especially for high voltage high power applications. For high voltage and high power applications, to avoid gate bounce and harmful shoot through situation, need to have high gate threshold voltage and stable gate drive without worrying for over drive. This is currently not achievable with existing E-mode technologies. The device in our presentation is two die normally off configuration

2. Product robustness

The product parameters shared here came from our 50 mΩ (typical at 25°C) 650 V device but all our products/technology share the same common robustness. Product robustness include parametric assurance like, high reliability gate structure (± 20 V) and high threshold voltage (V_{th} = 4 V) that provides a high safety margin against gate source transients induced due to the high drain source dv/dt, high voltage source-drain transient specification (800 V for 650 V device) capable of handling switching transients up to 800 V reliably, rated operating range of -55 °C to 175 °C with $T_{j(max)}$ of 175 °C, body diode characteristics with very low V_F (1.3V @ 12 A) enabling Si-like freewheeling current capability without complex dead time adjustments and along with other parametric performances are part of the product robustness of the GaN product family.

3. Quality / qualification of power GaN technology including failure modes

The latest generation 650 V GaN FETs are qualified in accordance with AEC-Q101 Rev D level qualification tests. Results shared here are done on 50 mΩ (typical at 25 °C) 650 V device that include 650 V, 175 °C High Temperature Reverse Bias (HTRB) tests (1000 hrs) and dynamic R_{DSon} shifts. In the following, the term *dynamic R_{DSon}* will be used to emphasize that R_{DSon} measurements are made with a dynamic, switch-mode test. Temperature cycling tests (1000 cycles) are performed over the range of -55°C to 150°C. High temperature (175 °C) Gate positive (+20 V) and negative (-20 V) bias tests were performed. Further life tests include high temperature biased and unbiased humidity tests and operating life tests. These are only some of the critical tests performed and passed to show the reliability and high quality of the technology.

3.1. HTRB

High-Temperature Reverse Bias has been performed at full rated voltage and maximum operating temperature: 650 V and 175 °C. The condition for passing is that R_{DSon} does not shift by more than 20%. For GaN FETs it is important that R_{DSon} be tested dynamically to detect any short-term change due to charge trapping. Figure 1 shows the shift in dynamic R_{DSon} for the test population. Note that the maximum shift is less than 15%. An additional HTRB test was performed and passed at 800 V for 10 hours. This voltage is well above the DC rating, but does correspond to the repetitive transient voltage rating.

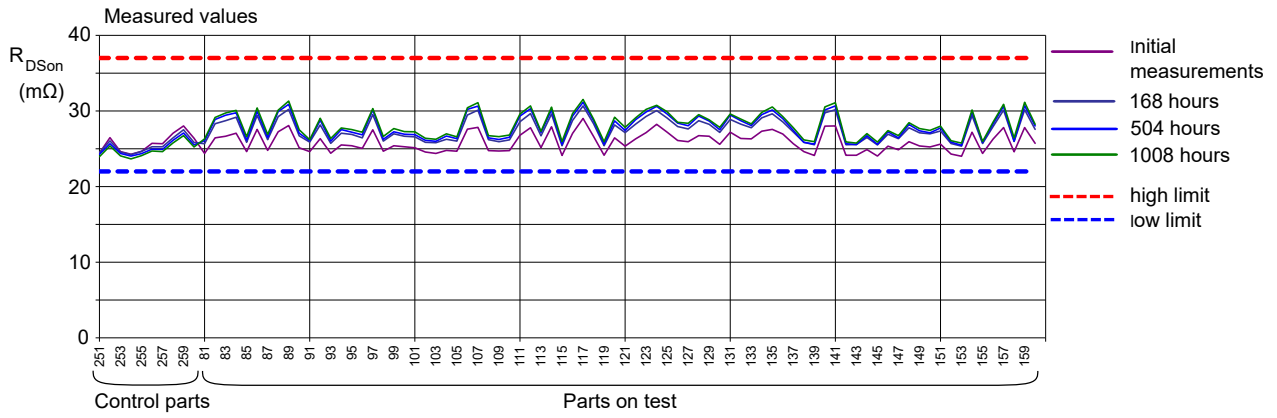


Fig. 1. Dynamic R_{DSon} measurement during HTRB

3.2. HTOL

High-Temperature Operating Life tests are not part of the AEC-Q101 standard, but are useful in validating reliability of the parts under actual operating conditions. This is particularly important for new materials, like GaN, to ensure that any new or unfamiliar failure modes are uncovered. A basic half-bridge operating in continuous conduction mode provides the most fundamental exercise of switching behaviour. For this test, a number of identical half-bridge circuits were prepared using two each of the GAN063-650WSA. These were operated continuously as synchronous-boost converters with the following conditions:

- V_{in} = 200 V
- V_{out} = 480 V
- P_{out} = 800 W
- T_j = 175 °C
- Frequency = 300 kHz

The following graph shows efficiency of all samples during the 1,000 hour test. As may be seen, there is no indication of degradation in any of the sample circuits. Following the tests, all devices were tested for shifts in dynamic R_{DSon}, leakage current, and threshold voltage. All parameters were found to be stable, with any parametric shift within allowed levels.

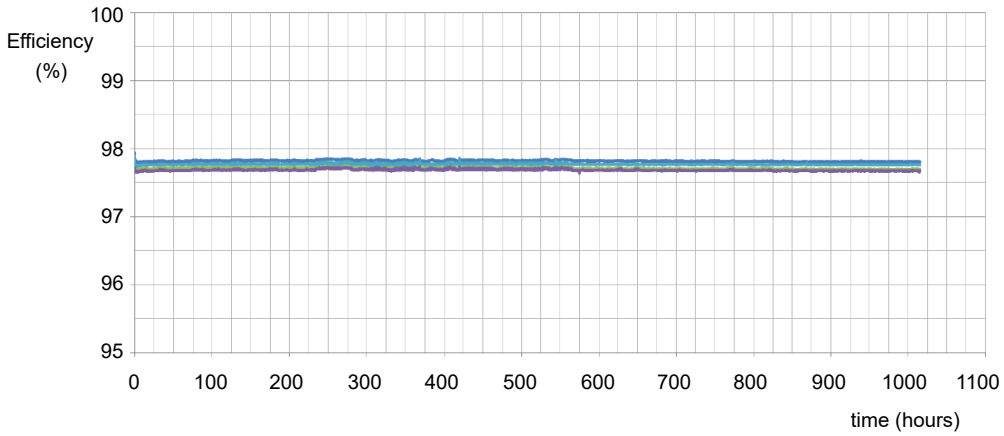
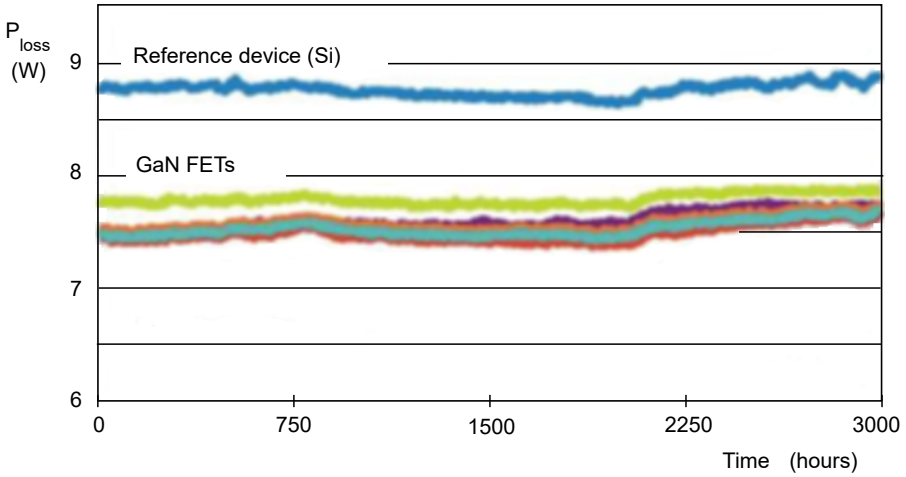


Fig. 2. Efficiency of boost converters (HTOL) over 1000 hours



Tested in hard-switched boost converter.
Operating conditions: 200 / 400 V converter operation:
175 °C; 300 kHz; 410 W

Fig. 3. Hard switched boost converter (HTOL) @ 175 °C for 3000 hours

Failure modes addressed by life testing power GaN technology failure modes can be linked back to the life testing and extra testing performed. Like power cycling relates to wire bond heel crack, temperature cycling address the solder degradation, HTGB look at the gate insulator failure, HTRB addresses the field plate insulator failure while high temperature direct current test addresses the trapped charge in gate region and consequently higher R_{DSon} (>20% assumes fail).

4. Conclusion

Power GaN technology, though at the early stage of technology maturity offers significant commercial viability with robustness and reliability. For scaling up, tremendous growth potential is better addressed with power GaN technology on Si.

5. References

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2. **650 V Highly Reliable GaN HEMTs on Si substrates over multiple generations: matching Silicon CMOS manufacturing metrics and process control** — S. Chowdhury, et al., Compound Semiconductor Integrated Circuit Symposium (CSICS), IEEE, 2016.

6. Revision history

Table 1. Revision history

Revision number	Date	Description
1.0	2020-07-21	Initial version

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