M.2 High Speed IO Module Hardware User Guide

Version 1.0

LIT# ACC-HSIO-M2-UG-V1P0

Contents

Figures

Tables

.

1 Document Control

Document Version: 1.0

Document Date: 20 September 2024

2 Version History

Version	Date	Comment
1.0	09/20/2024	Initial Release

3 Introduction

The M.2 High Speed IO (HSIO) Module is an accessory expansion card solution that is intended to be paired with Tria Technologies AMD platforms containing the mating High Speed IO connectors.

- Offering an expansion port conversion from HSIO connector to M.2 E-Key or M.2 B-Key connector. Allows AMD based expansion port for engineers to adopt in development, proof-of-concept, and production projects.
- Allows expansion to a variety of M.2 based modules such as WiFi, Bluetooth, Solid State Drives, and AI accelerators.
- Target many applications for development, including:
    - Machine Vision
    - Factory Automation
    - Industrial IoT and Smart Sensors
    - Smart Home Appliances
    - Prototyping and Experimentation

4 Architecture and Features

The M.2 High Speed IO Module provides a hardware environment for developing designs targeting the Tria Technologies portfolio of AMD offerings. The High-Speed IO (HSIO) connector exists on platforms that include the Zynq UltraScale+ such as the low cost ZUBoard and K24 Development Kit. The High-Speed IO connector also exists on a Versal AI Edge platform called the VE2302 Starter Kit.

The M.2 High Speed IO Module provides users access to an M.2 E-Key and a M.2 B-Key interface. These interfaces can accept a variety of M.2 off-the-shelf modules. The M.2 E-Key connector can support modules designed for the E-Key or the A+E Key combo. The M.2 B-Key connector can support modules that are designed for the B-Key or the B+M Key combo.

The details for the M.2 High Speed IO Module features are described in Functional Description sections that follow.

4.1 List of Features

The M.2 High Speed IO Modules supports the following features:

- High-Speed IO Board-to-Board Connector
  - Samtec Q-Strip High Performance 40-Pin 0.5mm Differential Pair Array
    - Part Number: **QTH-020-01-F-D-DP-A-K-TR**
- Programmable MCU for information sharing between M.2 HSIO Module and the host platform
  - Microchip AVR ATTiny Microcontroller 8-Bit
    - Part Number: **ATTINY44A-MMH**
- M.2 E-Key Connector (Supports E modules A+E modules)
  - Amphenol ICC (FCI) Female M.2 (NGFF) PCIe M.2 Gen 3 Card Edge Connector
    - Part Number: **MDT275E01001**
- M.2 B-Key Connector (Supports B modules and B+M modules)
  - Amphenol ICC (FCI) Female M.2 (NGFF) PCIe M.2 Gen 3 Card Edge Connector
    - Part Number: **10128796-004RLF**
- PCIe Clock Generator
  - Microchip Crystal-less Four Output PCIe Clock Generator
    - Part Number: **DSC557-054444KI1**
- PCIe 4-Channel Switch
  - Diodes Incorporated 3.3V 20-Gbps 2:1 Mux/De-Mux Switch
    - Part Number: **PI3DBS16412**

4.2 Block Diagram

The following figure is a high-level block diagram of the M.2 HSIO Module:

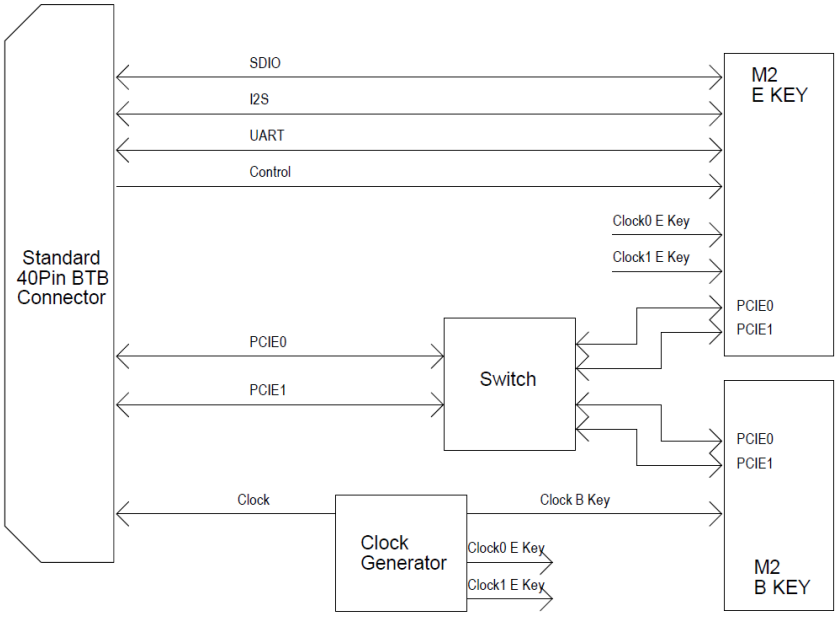

Figure 1 – M.2 HSIO Block Diagram

4.3 What's In The Box

The M.2 HSIO Module box includes only the M.2 HSIO Module and a Quick Start Card. This accessory kit is meant for HSIO expansion connector evaluation on Tria Technologies AMD platforms allowing for the integration of many of-the-shelf interfaces and peripherals. The K24 Development Kit includes the following in the box:

- M.2 HSIO Module
- Quick Start Card

Customers need to acquire an appropriate Tria Technologies platform that includes the mating HSIO connector.

- Tria Technologies ZUBoard-1CG: **http://avnet.me/zuboard-1cg**
- Tria Technologies K24 Development Kit: **http://avnet.me/k24-dk**
- Tria Technologies VE2302 Starter Kit: **http://avnet.me/ve2302-dk**

5 Functional Description

The following sections provide brief descriptions of each feature provided on the M.2 HSIO Module.

5.1 Interfaces and Connectors

The following figure provides an overview of the physical connections, their designators, and relative position on the M.2 HSIO Module.

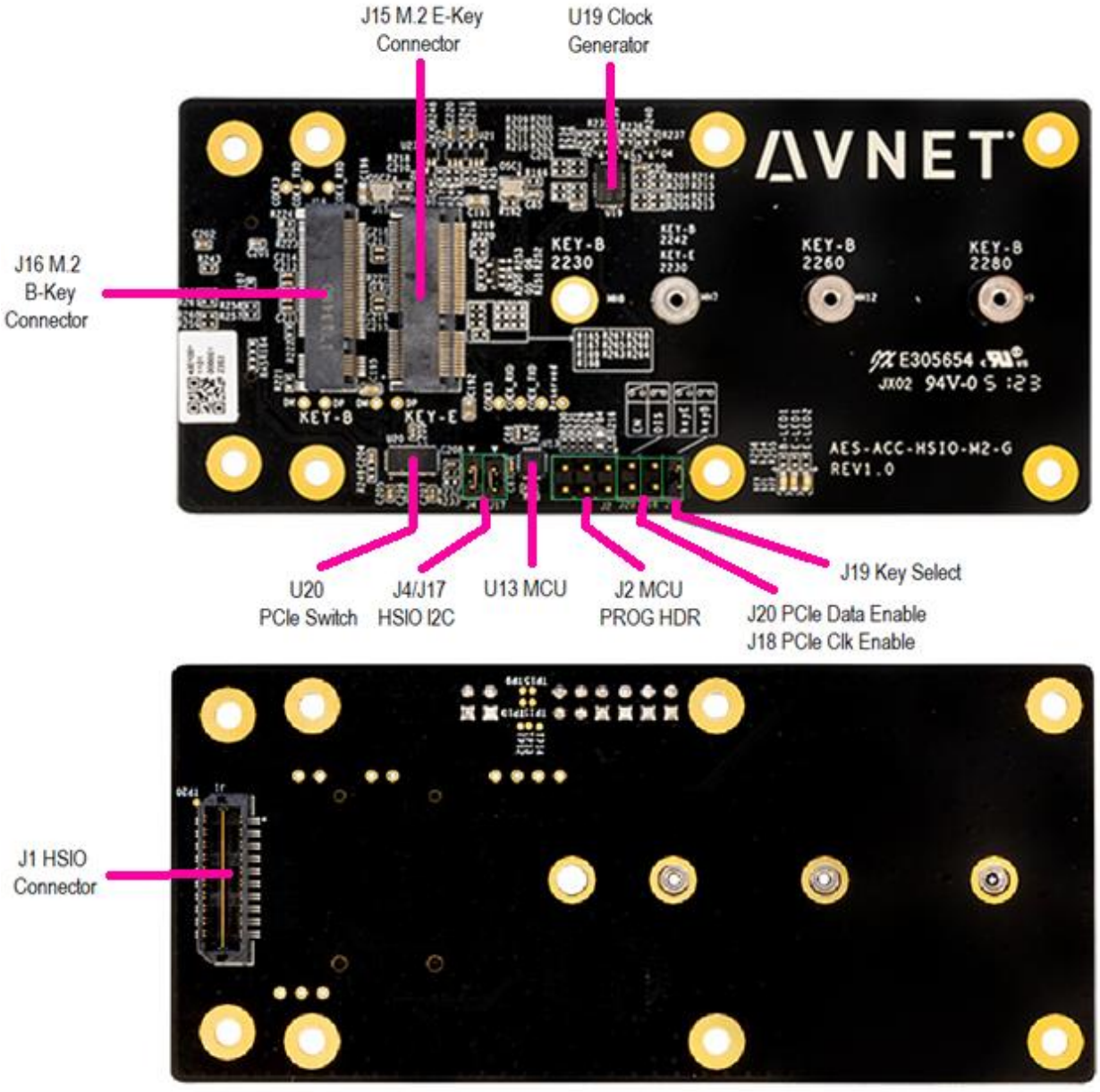

Figure 2 – Interfaces and Connectors

5.2 Setting up the M.2 HSIO Module

The M.2 HSIO Module requires has several headers on-board that allows the user to setup the board depending on what type of interface they would like to operate. What follows are descriptions of the various headers that exist on the board and the functionality they represent.

The first headers we will review are the **J4** / **J17** HSIO expansion interface I2C headers and the **J2** MCU Programming Header. The **J4** / **J17** headers allow a user to open circuit the I2C pins on the HSIO expansion interface when a user desires to utilize the **J2** MCU Programming Header to program the on-board MCU. The headers are used to prevent contention between the MCU and the interface pins on the Carrier Card processor. By open circuiting header **J4** / **J17** a user can prevent damage to the Carrier Card processor and the on-board MCU.

- When **J4 / J17** are shunted, the Carrier Card processor can access to the MCU and the programming header, **J2,** should not be utilized.

- When **J4** / **J17** are not shunted, the Carrier Card processor is isolated from the MCU and the programming header, **J2**, can be utilized to program the MCU.

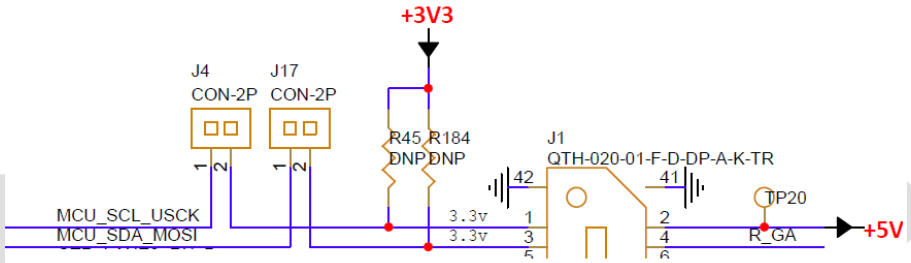

Figure 3 – HSIO I2C Headers J4 / 17

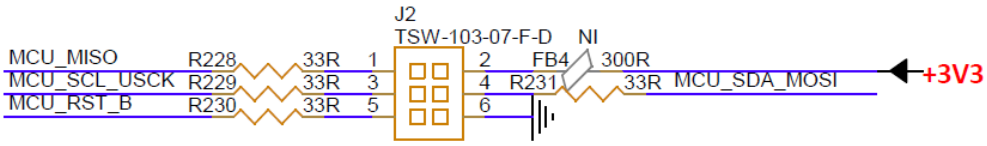

Figure 4 – MCU Programming Header J2

The three remaining headers on the board are utilized to enable PCIe data, clocks, and select which M.2 connector receives the high-speed data lanes.

- The header **J18** is used to enable the PCIe clock generation. **J18** open enables the PCIe clock generation. **J18** shunted disables the PCIe clock generation. A user can use this disable feature if they are not utilizing the high-speed data lanes.

- The header **J20** is used to enable the PCIe switch. **J20** open enables the PCIe switch. J20 shunted disables the PCIe switch. A user can use this disable feature if they are not utilizing the high-speed data lanes.

- The header **J19** is used to select whether the high-speed data lanes are routed to the M.2 E-Key connector or are routed to the M.2 B-Key connector. **J19** open selects the M.2 E-Key connector to utilize the high-speed data lanes. **J19** shunted selects the M.2 B-Key connector to utilize the high-speed data lanes.

5.3 HSIO Expansion Interface

The M.2 HSIO Module offers a Samtec connectors for HSIO (high-speed I/O) expansion interfaces as the main board-to-board connector, **J1**. This board-to-board interface contains a mix of high-speed data lanes known as GTs (multi-gigabit transceivers) and general purpose I/Os. How these pins are interfaced to will depend on the Carrier Board that is utilized with the M.2 HSIO Module.

It is important that you review the mating board connections to the HSIO expansion connector interface to ensure proper operation. Please check that the voltage provided by the HSIO expansion connectors, and that the available IO are mapped to appropriate signals. The HSIO expansion connectors can include transceivers (GTs) from the programmable logic (GTH, GTY, etc) or the processor (PS-GTR) as well as providing GPIO from the programmable logic (HPIO, HRIO, etc) or the processor (MIO). Each design can present challenges with the chosen Carrier Card depending on the mix presented on the HSIO expansion connector and available IP in the device targeted.

When designing with the M.2 HSIO Module the user will be expected to map appropriate interfaces and voltage standards to the M.2 HSIO module. To do this, the user should review the schematics of the mating Carrier Boards HSIO expansion connector and map that through the **J1** HSIO connector on the M.2 HSIO Module to the respective M.2 Key target. The M.2 Key connector sections will define the expected voltages on the interfaces.

A Samtec **QTH-020-01-F-D-DP-A-K-TR** connector is used to provide the HSIO expansion interface which is also known as a TXR2 PLIO expansion interface. Figure 5 and Table 1 shows the pinout of the HSIO expansion interface and interfaces that are mapped to the connector.

- Manufacturer: Samtec
- Part Number: **QTH-020-01-F-D-DP-A-K-TR**
- 0.50mm / 40-position differential array connector

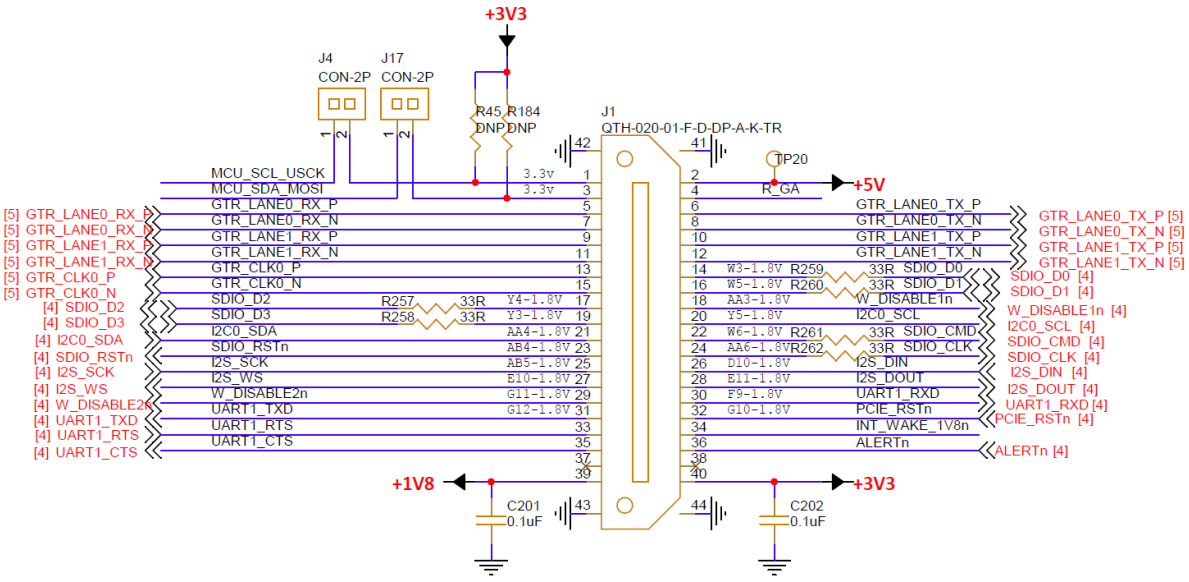

Figure 5 – HSIO Expansion Interface

HSIO Interface (J1) Pin Numbers	Schematic Net Name	Connection on M.2 Module
1	MCU_SCL_USCK	MCU I2C Clock Pin
3	MCU_SDA_MOSI	MCU I2C Data Pin
5 / 7	GTR_LANE0_RX_P/N	Shared GT RX Lane 0 Diff Pair
6 / 8	GTR_LANE0_TX_P/N	Shared GT TX Lane 0 Diff Pair
9 / 11	GTR_LANE1_RX_P/N	Shared GT RX Lane 1 Diff Pair
10 / 12	GTR_LANE1_TX_P/N	Shared GT TX Lane 1 Diff Pair
13 / 15	GTR_CLK0_P/N	Shared GT Reference Clock Diff Pair
14	SDIO_D0	E-Key SD Interface Data 0
16	SDIO_D1	E-Key SD Interface Data 1
17	SDIO_D2	E-Key SD Interface Data 2
18	W_DISABLE1n	B-Key W_DISABLE#
19	SDIO_D3	E-Key SD Interface Data 3
20	I2C0_SCL	E-Key I2C Clock
21	I2C0_SDA	E-Key I2C Data
22	SDIO_CMD	E-Key SD Interface Command
23	SDIO_RSTn	E-Key SD Interface Reset#
24	SDIO_CLK	E-Key SD Interface Clock
25	I2S_SCK	E-Key I2S Clock
26	I2S_DIN	E-Key I2S SD In
27	I2S_WS	E-Key I2S WS
28	I2S_DOUT	E-Key I2S SD Out
29	W_DISABLE2n	B-Key POWER_OFF#
30	UART1_RXD	E-Key UART_RXD
31	UART1_TXD	E-Key UART_TXD
32	PCIE_RSTn	Shared PERST#
33	UART1_RTS	E-Key UART_RTS
34	INT_WAKE_1V8n	Shared Interrupt / Wake Signal
35	UART1_CTS	E-Key UART_CTS
36	ALERTn	Shared ALERT#

Table 1 – HSIO Expansion Interface Connections

5.4 M.2 E-Key Interface

The M.2 HSIO Module offers an Amphenol connector for the M.2 E-Key Interface, **J15**. This connector interface makes connections to the HSIO expansion connector, **J1**. M.2 modules such as Wifi and Bluetooth will be able to utilize the M.2 E-Key interface. The M.2 E-Key connector on the M.2 HSIO Module accepts boards designed to E-Key or A+E Key M.2 pinouts.

When using the M.2 E-Key interface the user will be expected to map appropriate interfaces and voltage standards from the M.2 E-Key interface to the HSIO expansion connector, **J1**, and then map that through to the processor interfaces on the mating Carrier Board. The M.2 E-Key connections will define the expected voltages on the interfaces and connections to the **J1** connector.

An Amphenol **MDT275E01001** connector is used to provide the M.2 E-Key interface. Figure 6 and Table 2 shows the pinout of the M.2 E-Key interface and how the interface is mapped to the HSIO expansion connector, **J1**.

- Manufacturer: Amphenol ICC (FCI)
- Part Number: **MDT275E01001**
- Female M.2 (NGFF) PCIe M.2 Gen 3 Connector E-Key

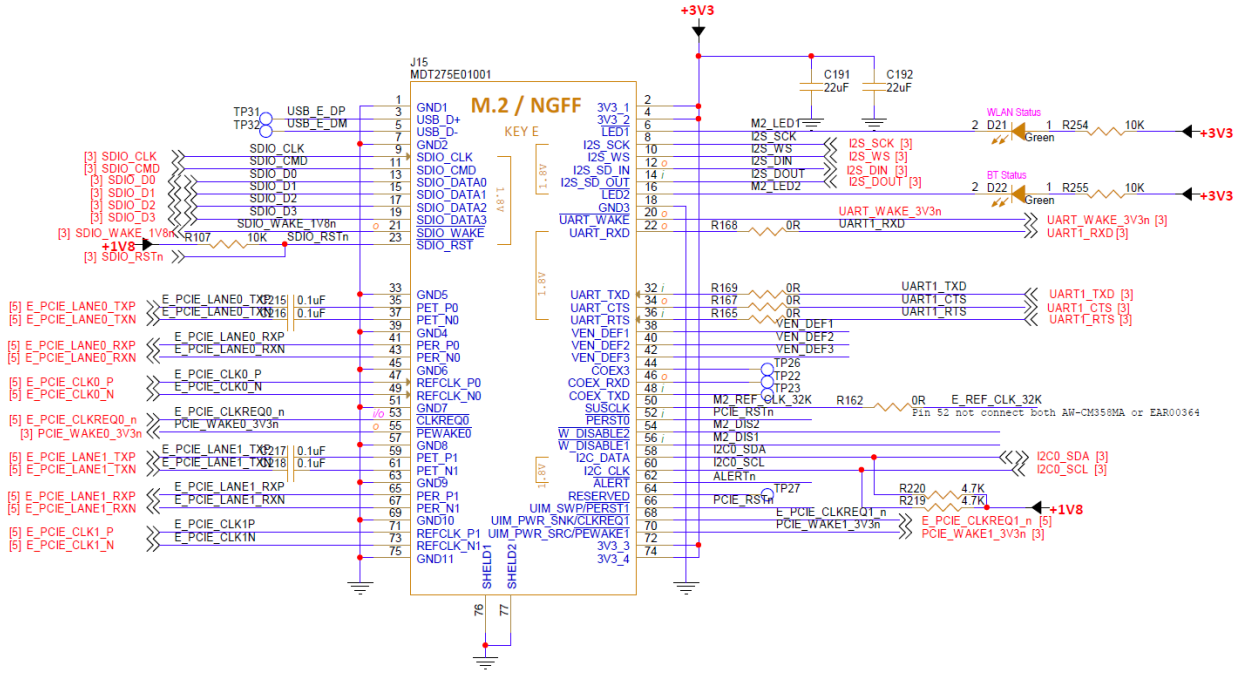

Figure 6 – M.2 E-Key Interface

M.2 E-Key (J15) Name and Number	Schematic Net Name	HSIO Interface (J1)
USB_D+ (1)	USB_E_DP	TP31
USB_D- (3)	USB_E_DM	TP32
SDIO_CLK (9)	SDIO_CLK	24
SDIO_CMD (11)	SDIO_CMD	22
SDIO_DATA0 (13)	SDIO_D0	14
SDIO_DATA1 (15)	SDIO_D1	16
SDIO_DATA2 (17)	SDIO_D2	17
SDIO_DATA3 (19)	SDIO_D3	19
SDIO_WAKE# (21)	SDIO_WAKE_1V8n	SHARED - 34
SDIO_RST# (23)	SDIO_RSTn	23

E_PCIE_LANE0_TXP (35)	PET_P0	MUXED - 6
E_PCIE_LANE0_TXN (37)	PET_N0	MUXED - 8
E_PCIE_LANE0_RXP (41)	PER_P0	MUXED - 5
E_PCIE_LANE0_RXN (43)	PER_N0	MUXED - 7
E_PCIE_CLK0_P (47)	REFCLK_P0	U19 - 8
E_PCIE_CLK0_N (49)	REFCLK_N0	U19 - 7
E_PCIE_CLKREQ0_n (53)	CLKREQ0#	U19 - 1 / 11
PCIE_WAKE0_3V3n (55)	PEWAKE0#	SHARED - 34
E_PCIE_LANE1_TXP (59)	PET_P1	MUXED - 10
E_PCIE_LANE1_TXN (61)	PET_N1	MUXED - 12
E_PCIE_LANE1_RXP (65)	PER_P1	MUXED - 9
E_PCIE_LANE1_RXN (67)	PER_N1	MUXED - 11
E_PCIE_CLK1P (71)	REFCLK_P1	U19 - 16
E_PCIE_CLK1N (73)	REFCLK_N1	U19 - 15
I2S_SCK (8)	I2S_SCK	25
I2S_WS (10)	I2S_WS	27
I2S_SD_IN (12)	I2S_DIN	26
I2S_SD_OUT (14)	I2S_DOUT	28
UART_WAKE# (20)	UART_WAKE_3V3n	SHARED - 34
UART_RXD (22)	UART1_RXD	30
UART_TXD (32)	UART1_TXD	31
UART_CTS (34)	UART1_CTS	35
UART_RTS (36)	UART1_RTS	33
PERST0# (52)	PCIE_RSTn	32
W_DISABLE2# (54)	W_DISABLE1n	SHARED - 18
W_DISABLE1# (56)	W_DISABLE2n	SHARED - 29
I2C_DATA (58)	I2C0_SDA	21
I2C_CLK (60)	I2C0_SCL	20
ALERT# (62)	ALERTn	SHARED - 36
PERST1# (66)	PCIE_RSTn	SHARED - 32
CLKREQ1# (68)	E_PCIE_CLKREQ1_n	U19 - 1 / 11
PEWAKE1# (70)	PCIE_WAKE1_3V3n	SHARED - 34

Table 2 – M.2 E-Key Interface Connections

5.5 M.2 B-Key Interface

The M.2 HSIO Module offers an Amphenol connector for the M.2 B-Key Interface, **J16**. This connector interface makes connections to the HSIO expansion connector, **J1**. M.2 modules such as SSDs will be able to utilize the M.2 B-Key interface. The M.2 B-Key connector on the M.2 HSIO Module accepts boards designed to B-Key or B+M Key M.2 pinouts.

When using the M.2 B-Key interface the user will be expected to map appropriate interfaces and voltage standards from the M.2 B-Key interface to the HSIO expansion connector, **J1**, and then map that through to the processor interfaces on the mating Carrier Board. The M.2 B-Key connections will define the expected voltages on the interfaces and connections to the **J1** connector.

An Amphenol **10128796-004RLF** connector is used to provide the M.2 B-Key interface. Figure 7 and Table 3 shows the pinout of the M.2 B-Key interface and how the interface is mapped to the HSIO expansion connector, **J1**.

- Manufacturer: Amphenol ICC (FCI)
- Part Number: **10128796-004RLF**
- Female M.2 (NGFF) PCIe M.2 Gen 3 1Connector B-Key

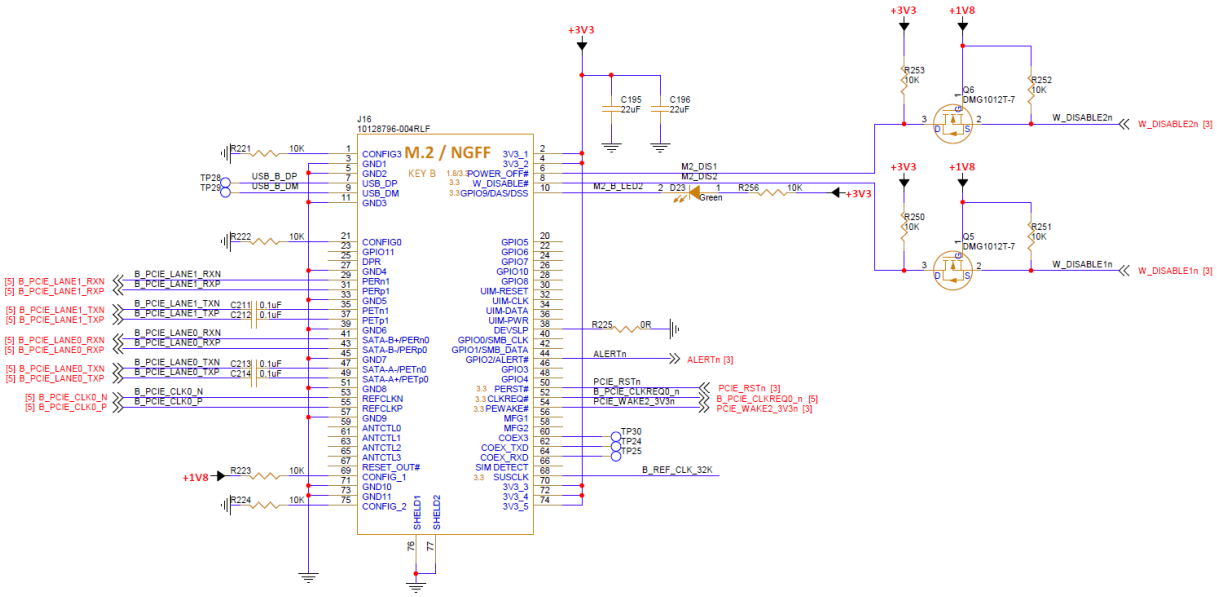

Figure 7 – M.2 B-Key Interface

M.2 B-Key (J16) Name and Number	Schematic Net Name	HSIO Interface (J1)
USB_DP (1)	USB_B_DP	TP28
USB_DM(3)	USB_B_DM	TP29
PERn1 (29)	B_PCIE_LANE1_RXN	MUXED - 11
PERp1 (31)	B_PCIE_LANE1_RXP	MUXED - 9
PETn1 (35)	B_PCIE_LANE1_TXN	MUXED - 12
PETp1 (37)	B_PCIE_LANE1_TXP	MUXED - 10
PERn0 (41)	B_PCIE_LANE0_RXN	MUXED - 7
PERp0 (43)	B_PCIE_LANE0_RXP	MUXED - 5
PETn0 (47)	B_PCIE_LANE0_TXN	MUXED - 8
PETp0 (49)	B_PCIE_LANE0_TXP	MUXED - 6
REFCLKN (53)	B_PCIE_CLK0_N	U19 – 5
REFCLKP (55)	B_PCIE_CLK0_P	U19 - 6

POWER_OFF#	W_DISABLE2n	SHARED - 29
W_DISABLE#	W_DISABLE1n	SHARED - 18
ALERT#	ALERTn	SHARED - 36
PERST#	PCIE_RSTn	SHARED - 32
CLKREQ#	B_PCIE_CLKREQ0_n	U19 - 1 / 11

Table 3 – M.2 B-Key Interface Connections

5.6 Clock Generator

The M.2 HSIO Module implements a Microchip PCIe Clock Generator IC, **U19**, to handle the creation of the clocks for the M.2 E-Key, M.2 B-Key, and the HSIO connector. The Microchip **DSC557-054444KI1** is a crystal-less four output PCIe Clock Generator that generates the 100MHz clocks required on the various interfaces.

- Manufacturer: Microchip
- Part Number: **DSC557-054444KI1**
- Crystal-Less 4-Output PCIe Clock Generator

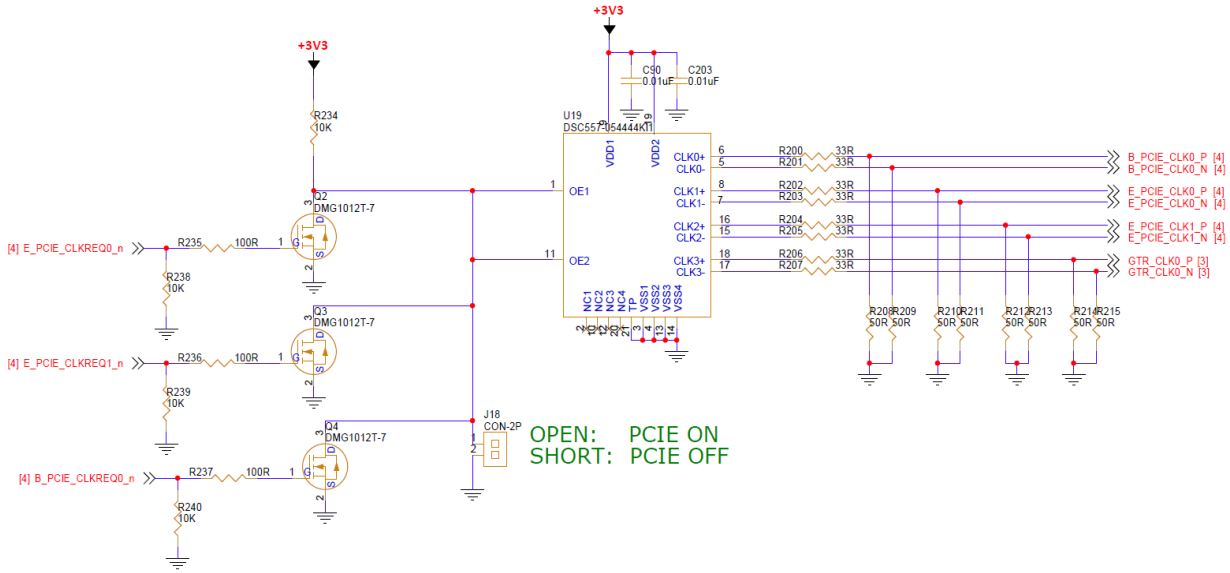

Figure 8 – Clock Generator Implementation

5.7 PCIe 4-Ch Switch

The M.2 HSIO Module implements a Diodes, Inc. PCIe 4-Channel Switch IC, **U20**, to handle selection of the GT data lanes presented from the M.2 HSIO expansion connector to the M.2 E-Key or M.2 B-Key. **U20** selects the M.2 E-Key or M.2 B-Key by setting the header **J19** appropriately. The user can disable device **U20** by appropriately setting the header **J20**. The PCIe 4-Channel Switch, **PI3DBS16412ZLCEX** is a 3.3V, up to 20Gbps, 2-Lane, 2:1 Mux/De-Mux switch with bi-directional operation.

- Manufacturer: Diodes, Inc.
- Part Number: **PI3DBS16412ZLCEX**
- 3.3V 20-Gbps 2:1 Mux/De-Mux Switch

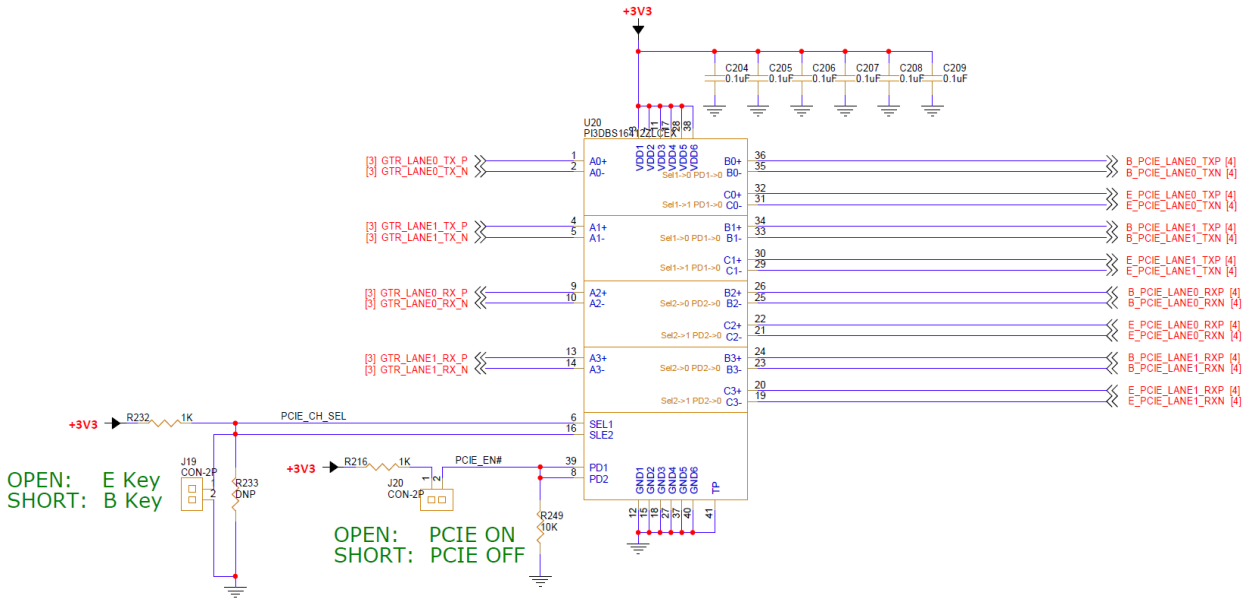

Figure 9 – PCIe 4-Ch Switch Implementation

5.8 Recommended Operating Conditions

This section contains the recommended operating conditions when using the M.2 HSIO Module. Values listed are those available at the time of publication. Users may want to consult the latest device manufacturer's specifications if their application approaches any of the limits.

It is important that you review the mating board connections to the HSIO expansion connector interface to ensure proper operation. Please check that the voltage provided by the HSIO expansion connectors agree with the table for recommended input voltages.

Parameter	Min	Max	Units	Notes
Operating Temperature	-40	80	C	M.2 Connectors Range

Table 4 – Recommended Temperature Range

Parameter	Min	Max	Units	Notes
5V Input Voltage	4.85	5.15	V	HSIO Connector 5V +/- 3%
3.3V Input Voltage	3.20	3.40	V	HSIO Connector 3.3V +/- 3%
1.8V Input Voltage	1.746	1.854	V	HSIO Connector 1.8V +/- 3%

Table 5 – Recommended Input Voltages

5.9 Mechanical

The M.2 HSIO Module is designed with a form factor intended to mate to Carrier Boards HSIO expansion sites. The M.2 HSIO Modules length was set to accommodate various size M.2 boards such as 2230, 2242, 2260, and 2280 size modules. The length used will depend on which M.2 connector is in use. The board measures 110mm x 50mm (approximately 4.33" x 1.97").

Several factors can affect the maximum vertical dimension of the board including the height of modules incorporated on the M.2 HSIO Module, custom heatsinks attached to the board perhaps in the case of an M.2 AI accelerator being used. A STEP model / DXF file of the PCB and its components can be made available to end users that may require it.

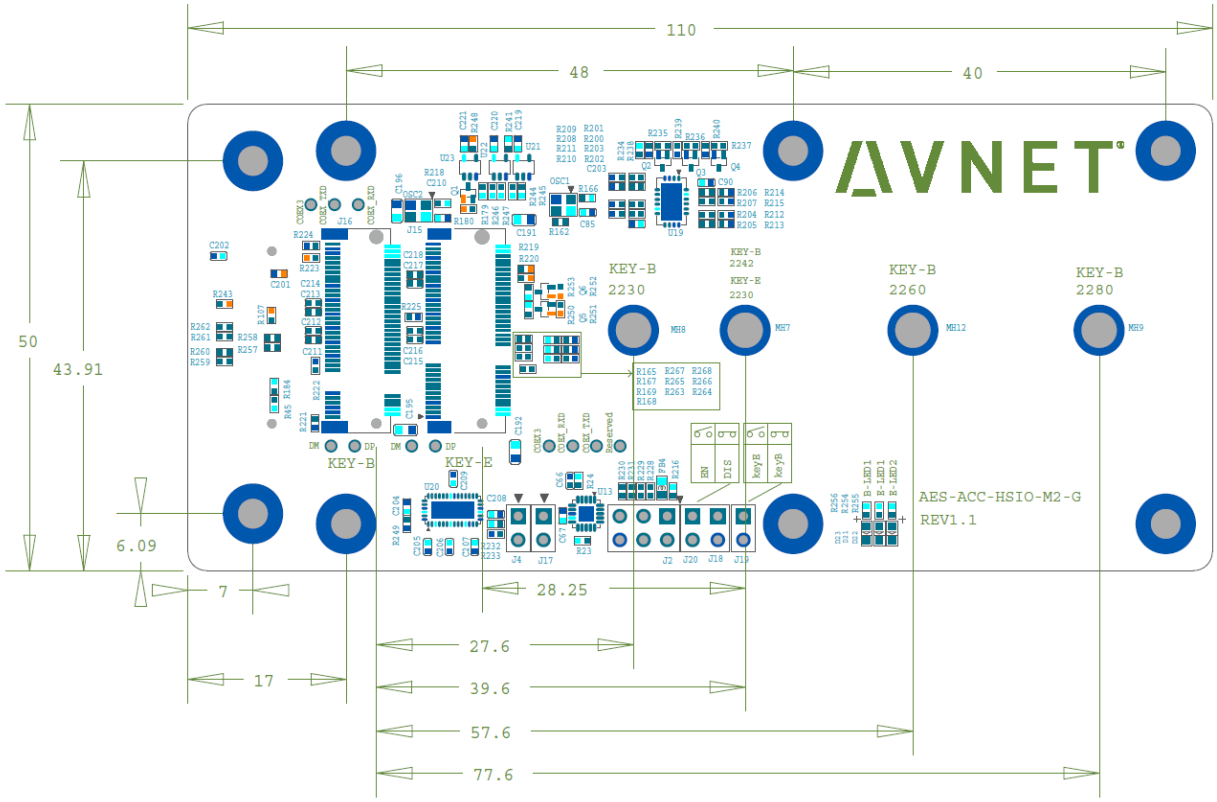

Figure 10 – Mechanical Dimensions

6 Getting Help and Support

If additional support is required, TRIA Technologies has many avenues to search depending on your needs.

For general question regarding M.2 HSIO, please visit our website at **http://avnet.me/m2-hsio-module**. Here you can find any available documentation, technical specifications, videos and tutorials, reference designs and other support.

Here are some interesting links on some posted references:

ZUBoard – Add WiFi, Bluetooth, and NVMe SSD
Hackster.IO Project: **http://avnet.me/m2-hsio-hackster**

ZUBoard - Petalinux Archive 2022.2 Tools
Avnet Sharepoint: **http://avnet.me/m2-hsio-linux-test**

ZUBoard – HSIO Hat-Trick (Using M.2 HSIO, DP-eMMC HSIO, and DualCam HSIO)
https://www.hackster.io/AlbertaBeef/supercharge-your-zuboard-with-the-hailo-8-ai-accelerator-79dd76

Detailed questions regarding M.2 HSIO Module hardware design, software application development, using AMD tools, training and other topics can be posted on the Avnet Boards Community pages at the Element14 Support Forums. Avnet's technical support team monitors the forum during normal business hours in North America.

Those interested in customer-specific options on K24 Development Kit can send inquiries to **customize@avnet.com**.

7 Certification Disclaimer

CE certification is necessary for system level products in those countries governed by this regulatory bodies.

Because Avnet boards are intended for evaluation kits only and destined for professionals (you) to be used solely at research and development facilities for such purposes, they are considered exempt from the EU product directives and normally are not tested for CE or FCC compliance.

If you choose to use your board to transmit using an antenna, it is your responsibility to make sure that you are in compliance with all laws for the country, frequency, and power levels in which the device is used. Additionally, some countries regulate reception in certain frequency bands. Again, it is the responsibility of the user to maintain compliance with all local laws and regulations.

8 Regulatory Compliance

WEEE Statement: Correct Disposal of this product.

This marking indicates that this product should not be disposed with other household wastes throughout the EU. To prevent possible harm to the environment or human health from uncontrolled waste disposal, recycle it responsibly to promote the sustainable reuse of material resources. To return your used device, please use the return and collection systems or contact the retailer where the product was purchased. They can take this product for environmentally safe recycling.

9 Safety Warnings

This product shall only be connected to a Carrier Card that provides the required current need to operate the HSIO expansion connector. Any external power supply used with the mating Carrier Card shall comply with relevant regulations and standards applicable in the country of intended use.

The connection of incompatible devices may affect compliance or result in damage to the unit and void the warranty.

This product shall be operated in a well-ventilated environment. If an enclosure is used, it shall have adequate ventilation. Use caution when handling the board when powered.