AN90003

LFPAK MOSFET thermal design guide

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Document information

Information	Content
Keywords	Thermal design, LFPAK56D, LFPAK33, LFPAK56, LFPAK88
Abstract	Thermal design guide: estimate of MOSFET power dissipation capability depending on PCB design.

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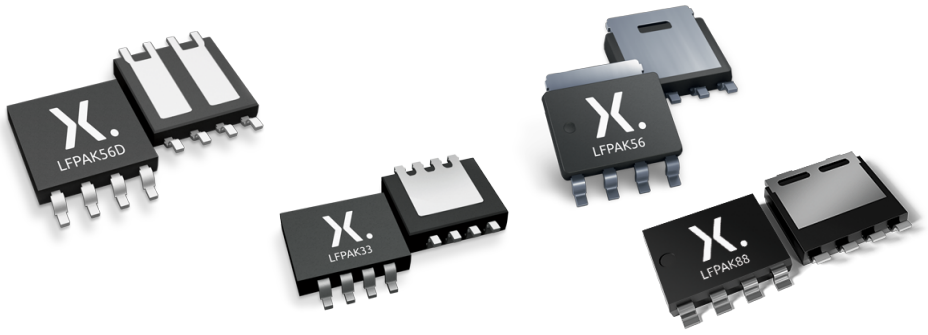
1. Introduction

This application note is a guide to assist design engineers in understanding the power dissipation limits of the LFPAK family of packages. The maximum power that a MOSFET can dissipate is considered as a function of the Printed Circuit Board (PCB) design, using some common configurations. The application notes is split into two sections addressing separately the low power LFPAKs (LFPAK56D and LFPAK33) and the high power LFPAKs (LFPAK56 and LFPAK88).



2. LFPAK56D and LFPAK33

2.1. Simple configuration with a single layer

In this section, we will present the maximum power dissipation results for a simple PCB configuration using a single layer with varying copper area.

Results for the LFPAK56D and LFPAK33 packages are given, for the LFPAK56D with only one or with both MOSFETs conducting.

2.1.1. LFPAK56D

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Fig. 1.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area.

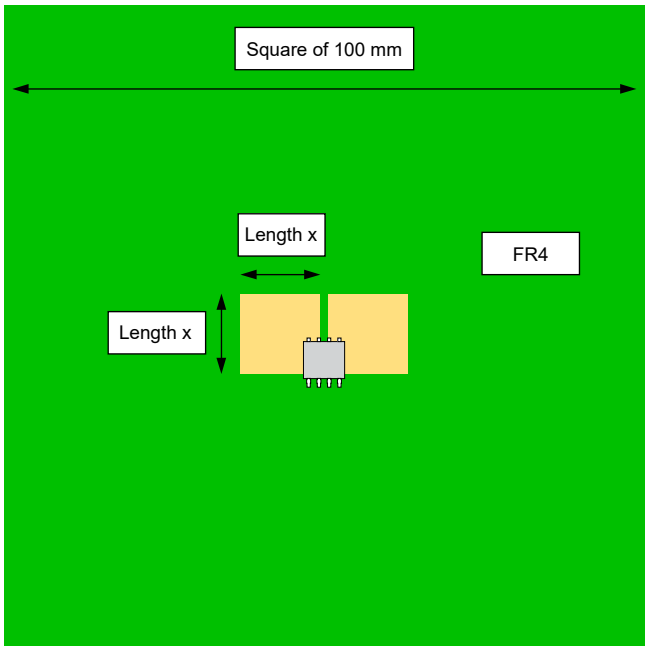


Fig. 1. Copper area configuration: LFPAK56D, single top copper layer

The graph in Fig. 2 captures two important factors:

- T_j depends greatly on length “x” and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”. In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j. As can be seen from Fig. 2 below, T_j will plateau at around 50 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j.

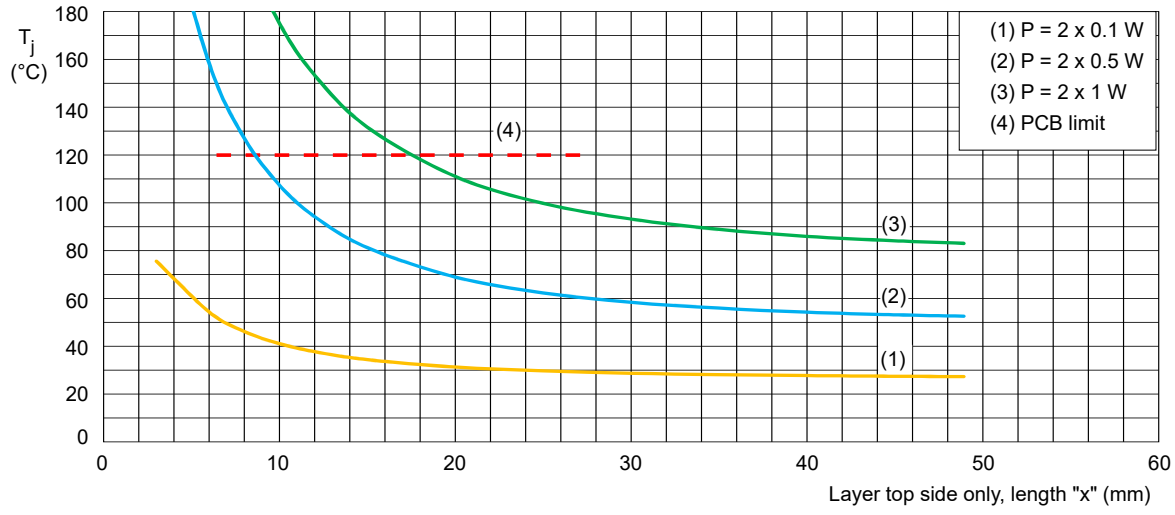


Fig. 2. Junction temperature as a function of copper side length x for LFPAK56D

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In Fig. 3 the maximum power for the conditions given is as follows:

T_{amb} = 20 °C: Max power is 2.6 W per MOSFET (2 × 2.6 W permissible in this package)
T_{amb} = 80 °C: Max power is 1.65 W per MOSFET (2 × 1.65 W permissible in this package)

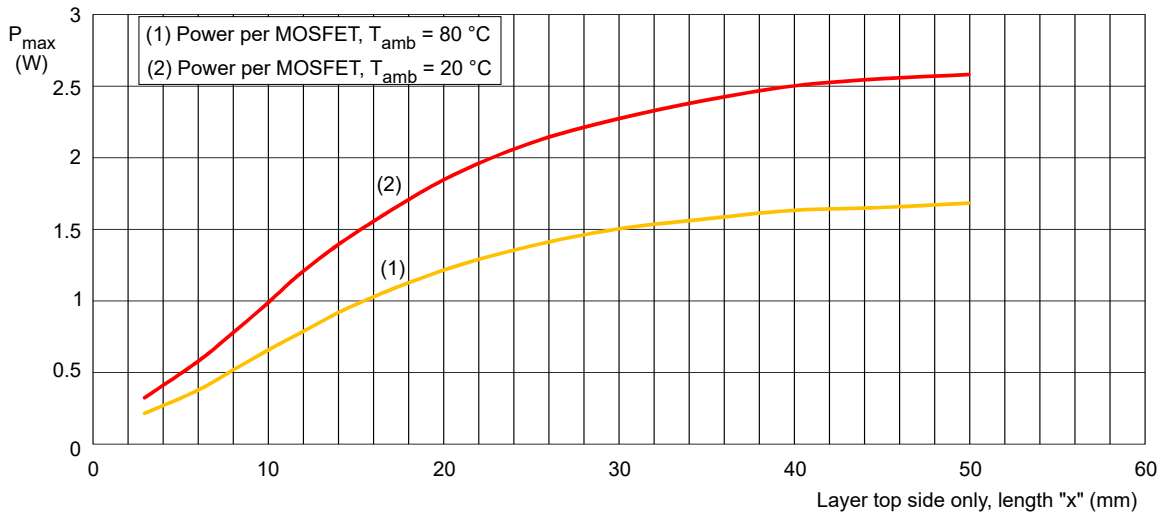


Fig. 3. Maximum permissible power dissipation as a function of copper side length x for LFPAK56D

2.1.2. LFPAK56D only one MOSFET active at a time

In a typical half bridge application only one MOSFET conducts at a time. In the graph below, Fig. 4, 1 W is dissipated in the left MOSFET (blue curve). We can see that 1 W dissipation in one MOSFET is not equivalent to 0.5 W dissipation in each of the two MOSFETs (yellow curve).

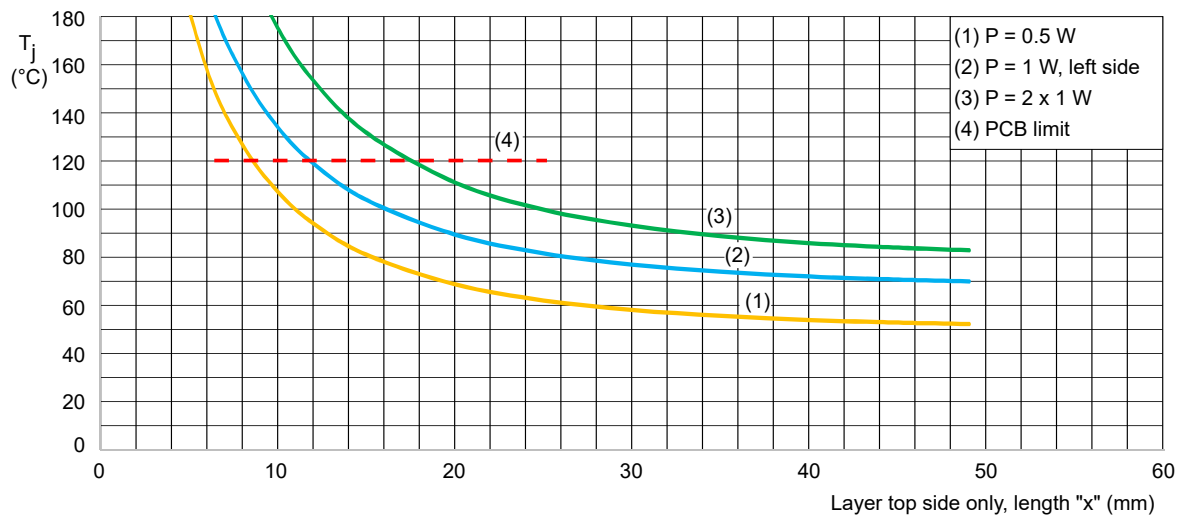


Fig. 4. Junction temperature as a function of copper side length x for LFPAK56D; one MOSFET conducting

As can be seen temperature is higher in the case of one MOSFET dissipating 1 W than it is with two MOSFETs each dissipating 0.5 W. When only one MOSFET is active the second MOSFET does not make a significant contribution to the total dissipation capability - meaning that if one MOSFET is off the heating is not shared equally between the two. This is further explained by the thermal network shown in Fig. 6.

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB. In Fig. 5 the maximum power for the conditions given is as follows:

- T_{amb} = 20 °C: Max power is 3.35 W with only left MOSFET
- T_{amb} = 80 °C: Max power is 2.1 W with only left MOSFET

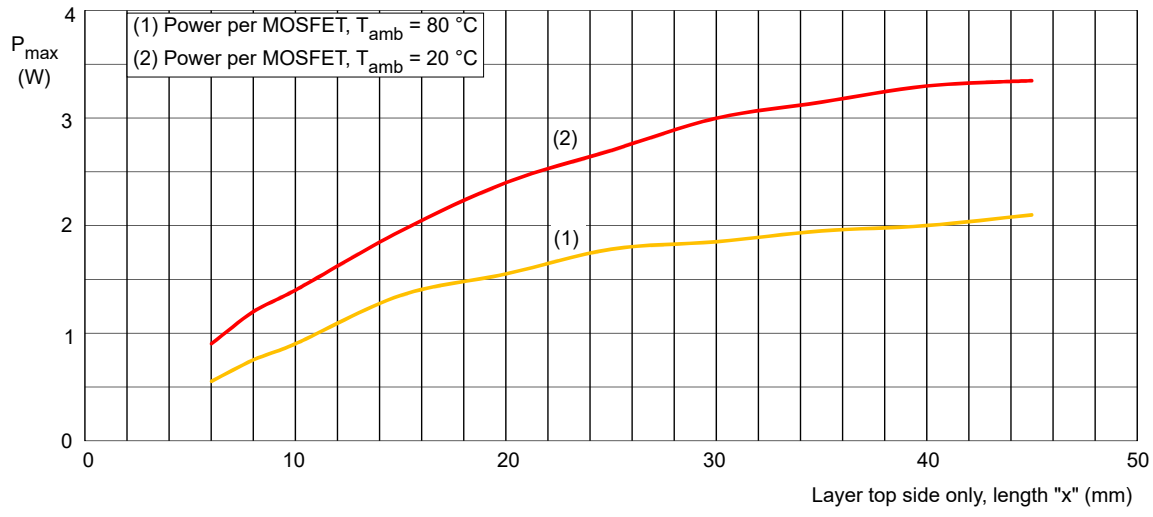


Fig. 5. Maximum power as a function of side length x for LFPAK56D; one MOSFET conducting

The concept of the second MOSFET half-sharing the thermal dissipation when turned off is not true – see Fig. 6

Dual MOSFET thermal resistance configuration:

We can see that the thermal path between both MOSFETs inside the package is highly resistive (100 K/W).

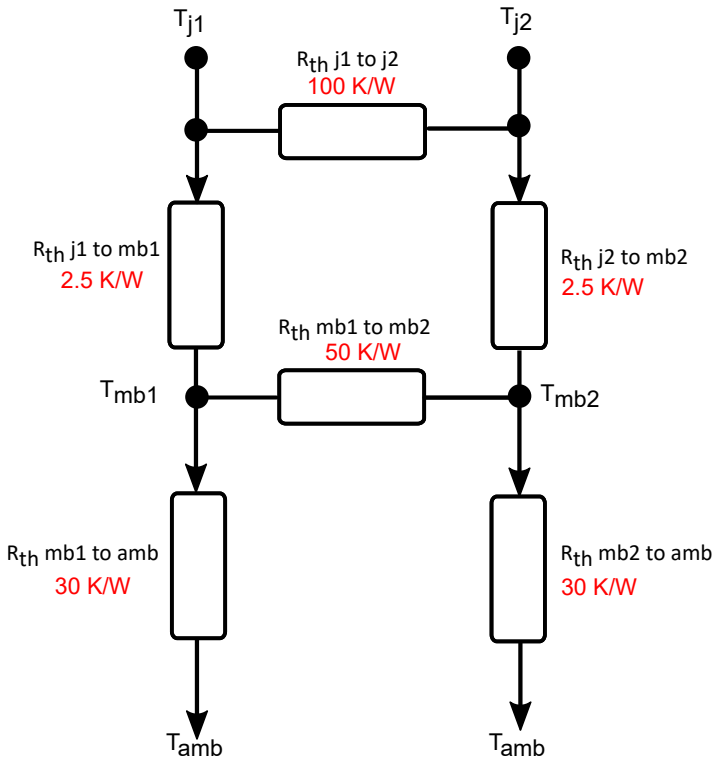


Fig. 6. Thermal resistance configuration

2.1.3. LFPAK33

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

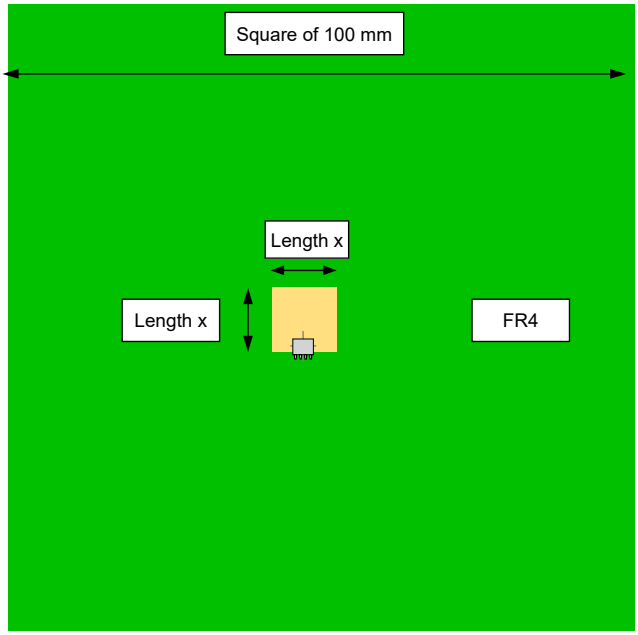


Fig. 7. Copper area configuration: LFPAK33, single top copper layer

The graph in Fig. 8 captures two important factors:

- T_j depends greatly on length “x” and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”. In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j. As can be seen from Fig. 8 below, T_j will plateau at around 40 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j.

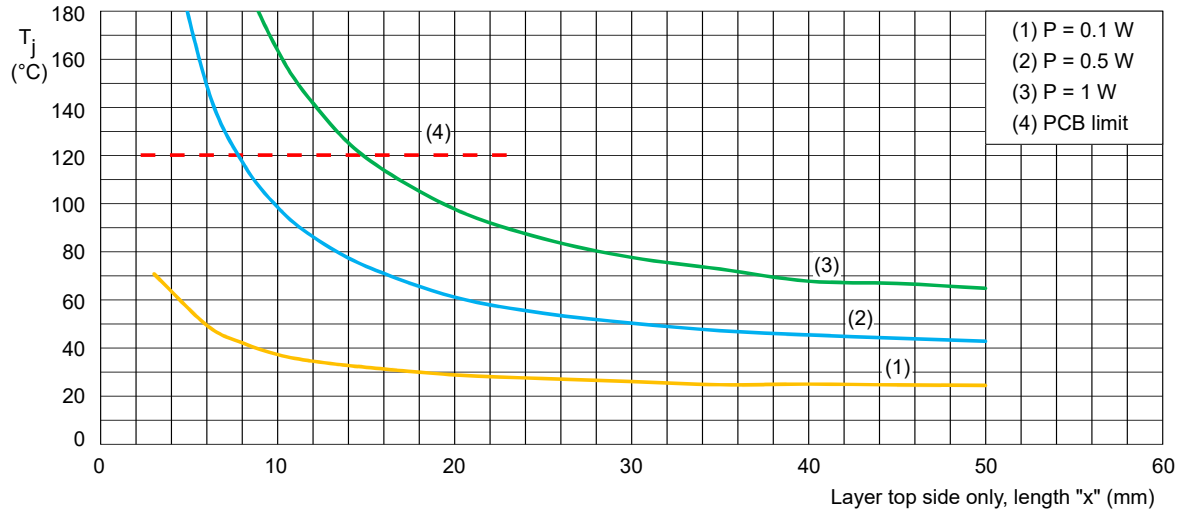


Fig. 8. Junction temperature as a function of copper side length x for LFPAK33

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below, Fig. 9, the maximum power for the conditions given is as follows:

T_{amb} = 20 °C: Max power is 3.7 W in the MOSFET
T_{amb} = 80 °C: Max power is 2.4 W in the MOSFET

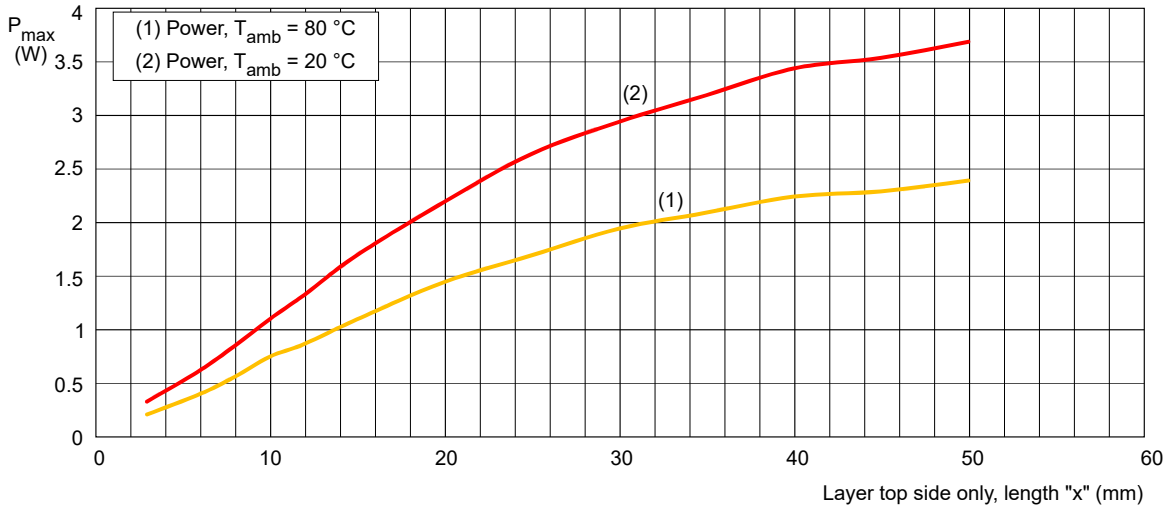


Fig. 9. Maximum permissible power dissipation as a function of copper side length x for LFPAK33

2.2. Usual configuration: 4 layers + vias

In this section, we will present the maximum power dissipation results for a PCB configuration using 4 layers + vias for dissipation on the bottom layer, with varying copper area.

Results for the LFPAK56D and LFPAK33 packages are given, for the LFPAK56D with only one or with both MOSFETs conducting.

2.2.1. LFPAK56D

Set-up:

- 4 layers + vias (vias number increases with the copper area with a maximum of 25 vias for each side)
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under MOSFETs to create a dissipation path to the heatsink.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area. In Fig. 10 below, we can see the vias configuration:

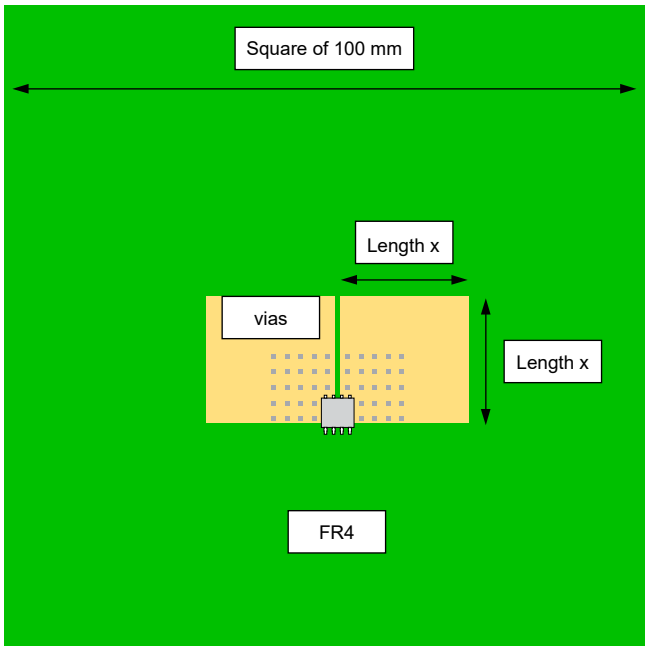
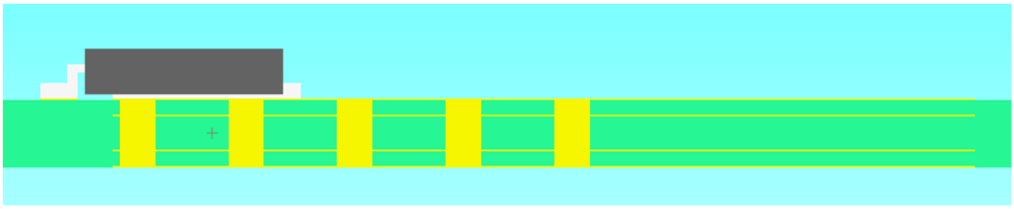


Fig. 10. Copper area configuration: LFPAK56D, 4 layers with vias



Vias configuration: square vias used for ease of simulation.

Fig. 11. Sectional view: LFPAK56D

Table 1. Limitation of number of vias

X (mm)	vias configuration		
minimal footprint	2+2 vias	Maximum number of vias able to be inserted in the copper surface	Vias pitch 2.5 mm Vias side length 0.7 mm Copper thickness 70 µm No solder fill
6	9+9 vias		
8	12+12 vias		
10	20+20 vias		
15	25+25 vias	25 vias maximum	
20	25+25 vias		
25	25+25 vias		
30	25+25 vias		
35	25+25 vias		
40	25+25 vias		
50	25+25 vias		

The graph in Fig. 12 captures two important factors:

- T_j depends greatly on length “x” and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”. In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j. As can be seen from the graph in Fig. 12, T_j will plateau at around 36 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as the PCB temperature directly under the transistor would be close to the MOSFET T_j.

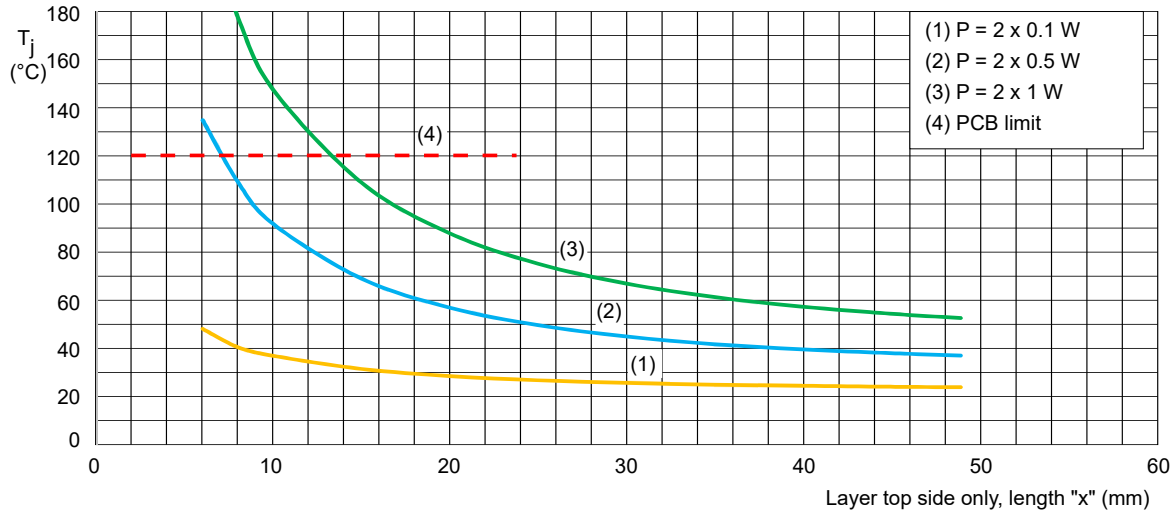


Fig. 12. Junction temperature as a function of copper side length x for LFPAK56D

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below, Fig. 13 the maximum power for the conditions given is as follows:

T_{amb} = 20 °C: Max power is 5.3 W per MOSFET (2 × 5.3 W permissible in this package)
T_{amb} = 80 °C: Max power is 3.55 W per MOSFET (2 × 3.55 W permissible in this package)

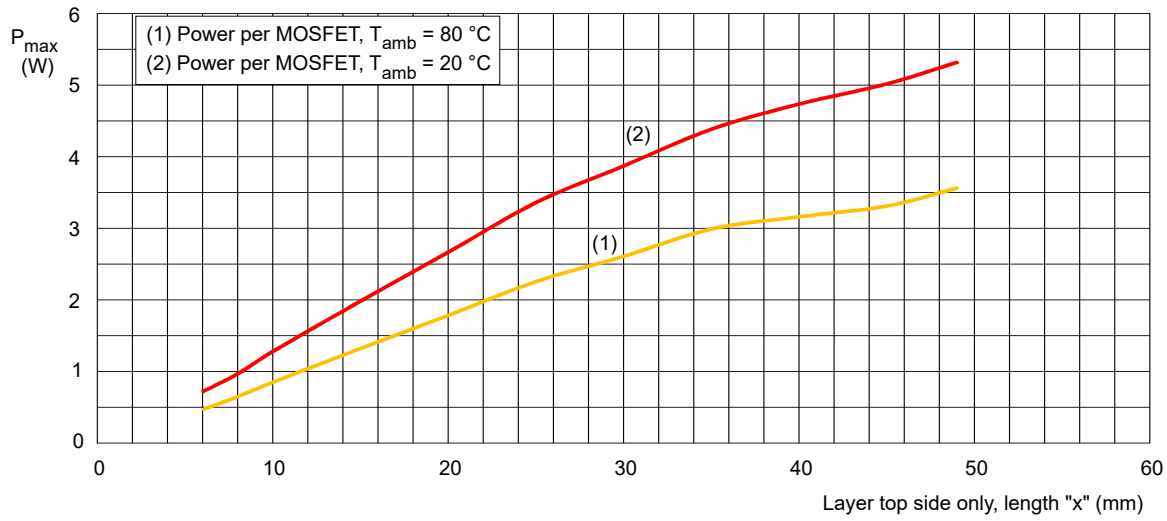


Fig. 13. Maximum permissible power dissipation as a function of copper side length x for LFPAK56D

2.2.2. LFPAK56D only one MOSFET active at a time

In a typical half bridge application only one MOSFET conducts at a time. Fig. 14 below shows the results for 1 W applied to the left MOSFET (blue curve). We can see that 1 W dissipated in one MOSFET is not equivalent to 0.5 W dissipation in each of the two MOSFETs (yellow curve).

As can be seen temperature is higher in the case of one MOSFET conducting with 1 W than it is with two MOSFETs each dissipating 0.5 W.

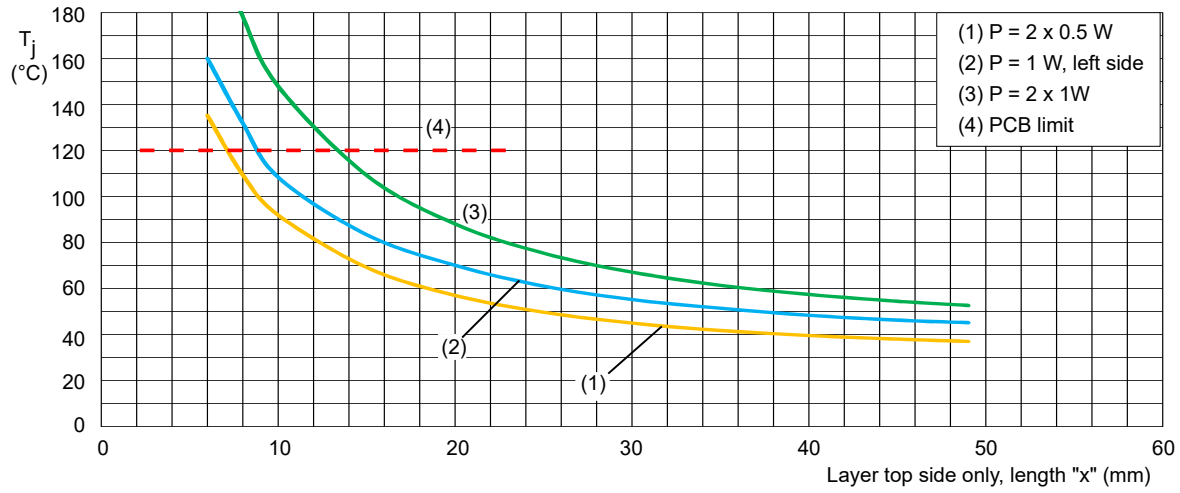


Fig. 14. Junction temperature as a function of copper side length x for LFPAK56D; one MOSFET

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In Fig. 15 the maximum power for the conditions given is as follows:

- T_{amb} = 20 °C: Max power is 6 W with only left MOSFET
- T_{amb} = 80 °C: Max power is 4 W with only left MOSFET

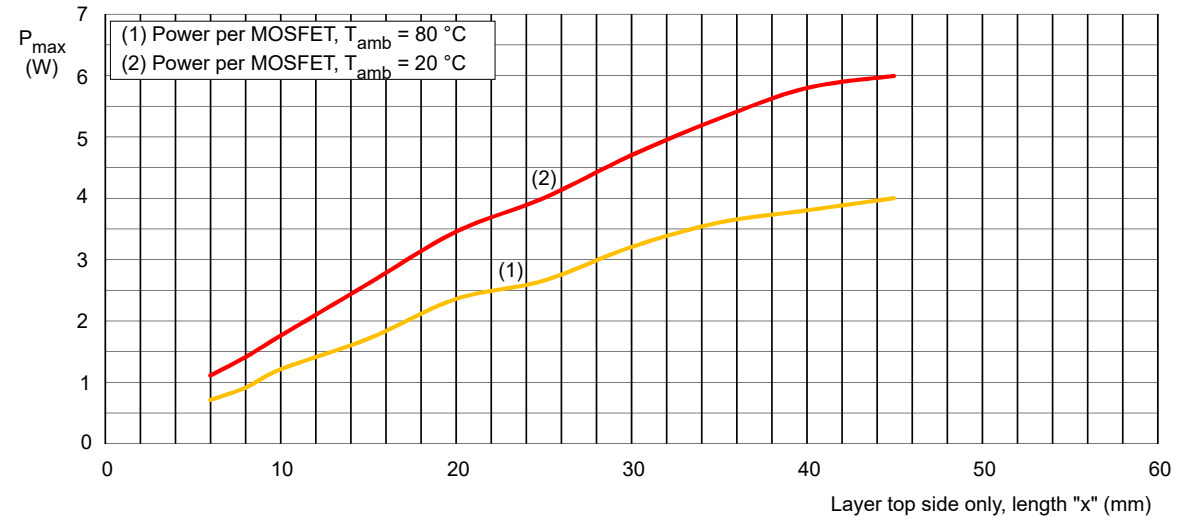


Fig. 15. Power dissipation as a function of copper side length x for LFPAK56D; one MOSFET

As previously mentioned, when only one MOSFET is active the second MOSFET does not make a significant contributution to the total dissipation capabilty – see Fig. 6.

2.2.3. LFPAK33

Set-up:

- 4 layers + vias (vias number increases with the copper area with a maximum of 25 vias for each side)
- MOSFET power dissipation is 0.1 W, 0.5 W and 1 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under the MOSFETs to create a dissipation path to the heatsink.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

In Fig. 16 below, we can see the vias configuration:

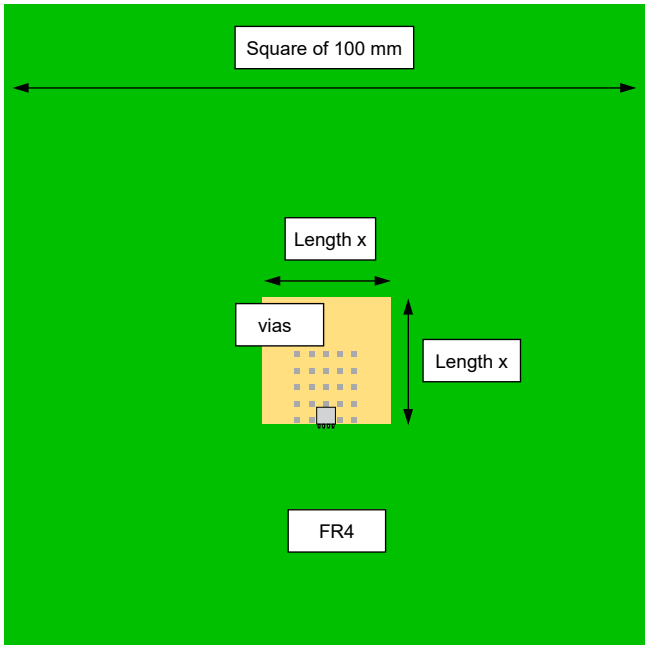
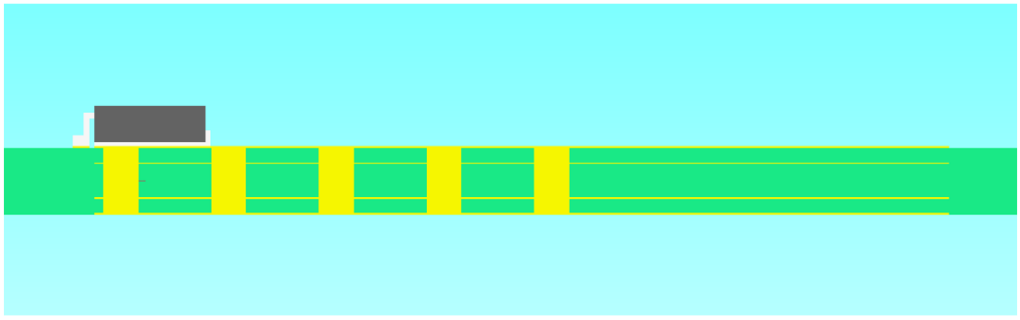


Fig. 16. copper area configuration: LFPAK33, 4 layers with vias



Vias configuration: square vias used for ease of simulation.

Fig. 17. Sectional view: LFPAK33

Table 2. Vias configuration

X (mm)	vias configuration		
minimal footprint	1 via	Maximum number of vias able to be inserted in the copper surface	Vias pitch 2.5 mm Vias side length 0.7 mm Copper thickness 70 µm No solder fill
6	6 vias		
8	9 vias		
10	20 vias		
15	25 vias	25 vias maximum	
20	25 vias		
25	25 vias		
30	25 vias		
35	25 vias		
40	25 vias		
50	25 vias		

The graph Fig. 18 captures two important factors:

- T_j depends greatly on length “x” and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”. In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j. As can be seen from Fig. 18 below T_j will plateau at around 33 °C (for 0.5 W per MOSFET) no matter how much copper area we provide.

Care must be taken for T_j above 120 °C as PCB temperature directly under the transistor would be close to the MOSFET T_j.

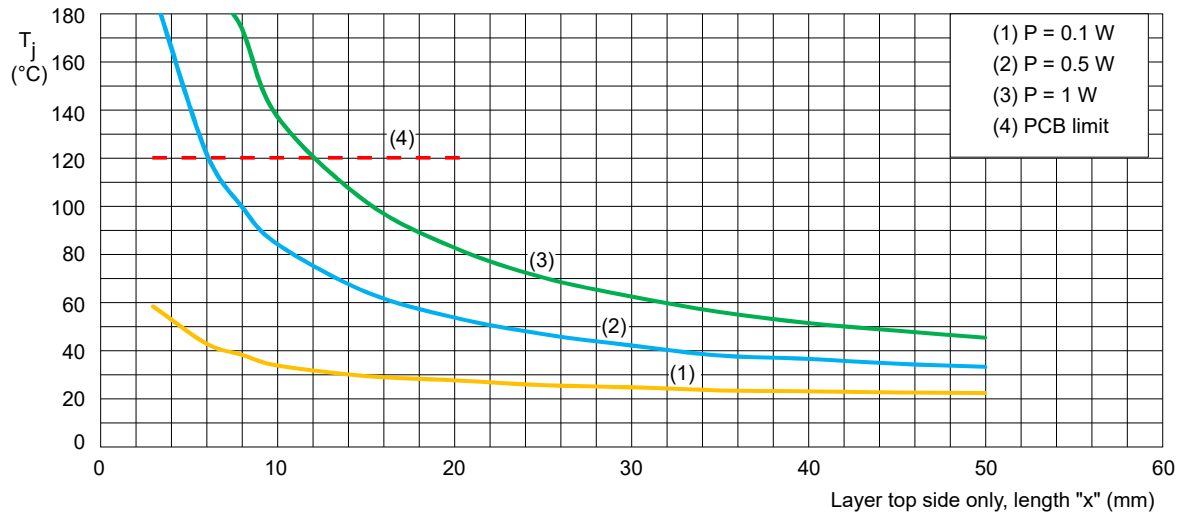


Fig. 18. Junction temperature as a function of copper side length x for LFPAK33

An alternative to the previous approach is to look at the maximum power allowed before reaching $T_{j(max)}$ = 175 °C (MOSFET absolute max). Maximum power allowed is shown for different ambient temperature and copper length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

In the graph below the maximum power for the conditions given is as follows:

T_{amb} = 20 °C: Max power is 6.5 W in the MOSFET
T_{amb} = 80 °C: Max power is 4.3 W in the MOSFET

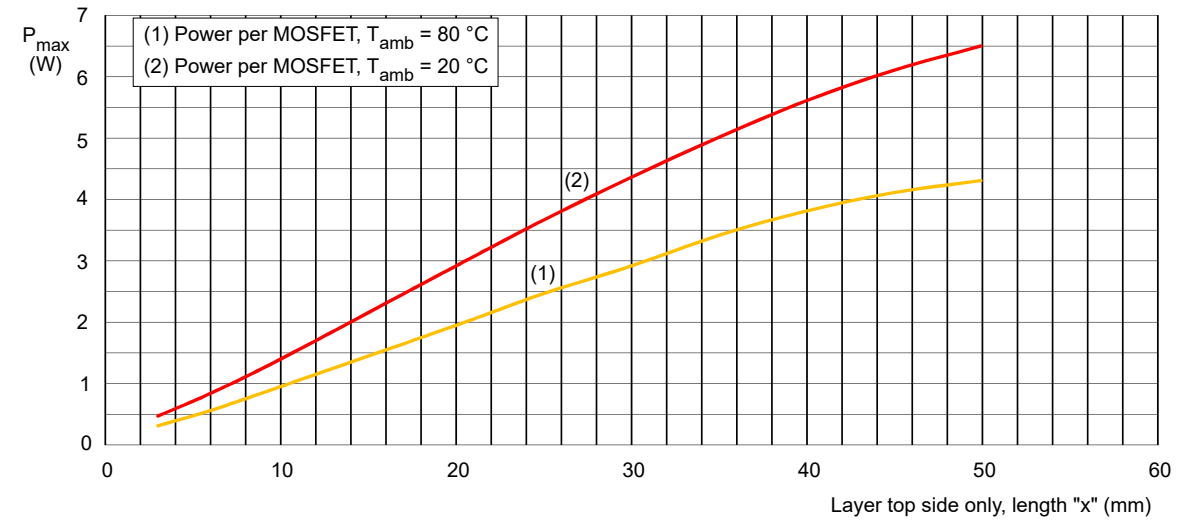


Fig. 19. Maximum permissible power dissipation as a function of copper side length x for LFPAK33

2.3. Placement advice for improved dissipation

In this section, we will present some results for two MOSFETs placed close to each other on a single layer PCB with varying copper area.

2.3.1. LFPAK56D

Simulation of two MOSFETs placed next to each other is carried out and checked against results seen in section 2.1. The aim is to understand the dissipation effect that the two LFPAK56D have on one another.

Set-up

- 1 layer on the top side
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 200 x 150 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness on all layers (external and internal) is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- 2 mm gap between right and left copper layers
- Simulation carried out for different length “x”
- 0.5 W applied on each internal MOSFET

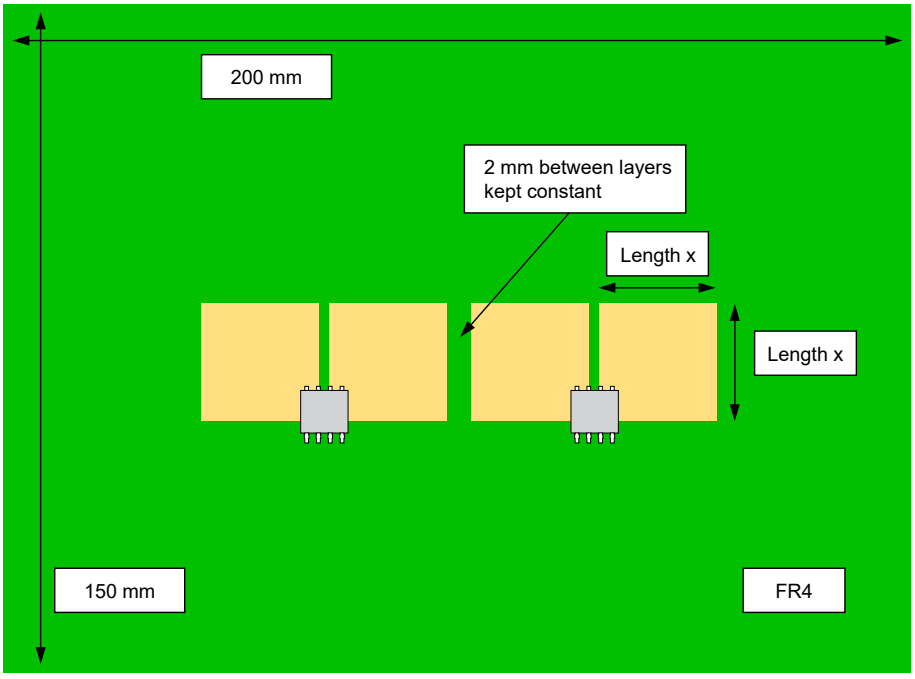


Fig. 20. Copper area configuration: LFPAK56D, single top copper layer

The graph in Fig. 21 shows:

- The results (in green) are similar to the ones observed in section 2.1 (slightly higher +3 °C)
- This is due to the low conductivity of FR4, despite only 2 mm gap it showed no heat transfer from one copper area to the other

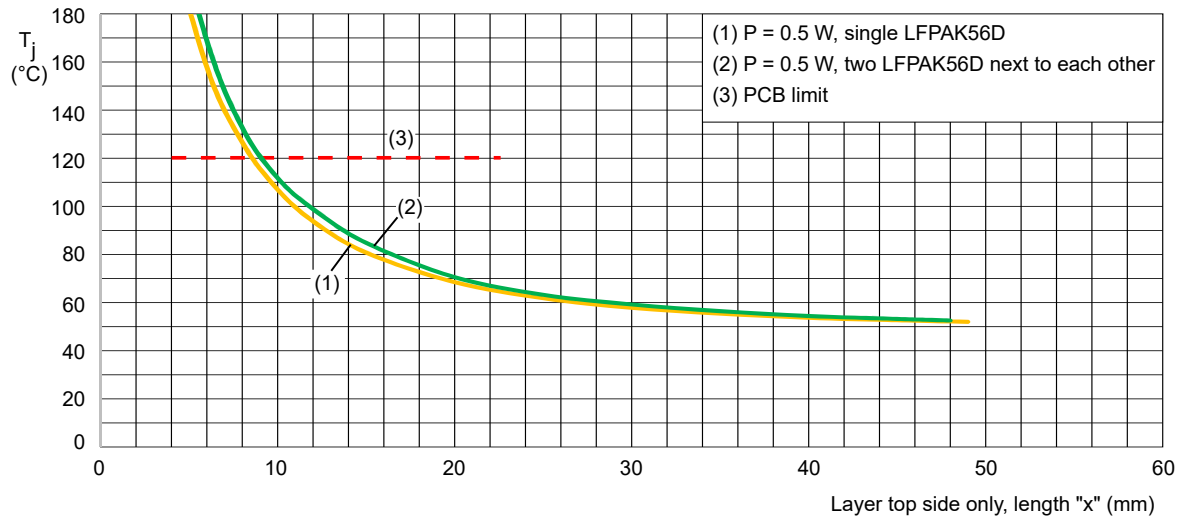


Fig. 21. Junction temperature as a function of copper side length x for 2 LFPAK56D

2.3.2. LFPAK33

Simulation of two MOSFETs placed next to each other is carried out and checked against results seen in section 2.3. The aim is to understand the dissipation effect that the two MOSFETs have on one another.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied in the MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 200 x 150 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- 2 mm gap between right and left copper layers
- Simulation carried out for different length “x”
- 0.5 W applied on each MOSFET

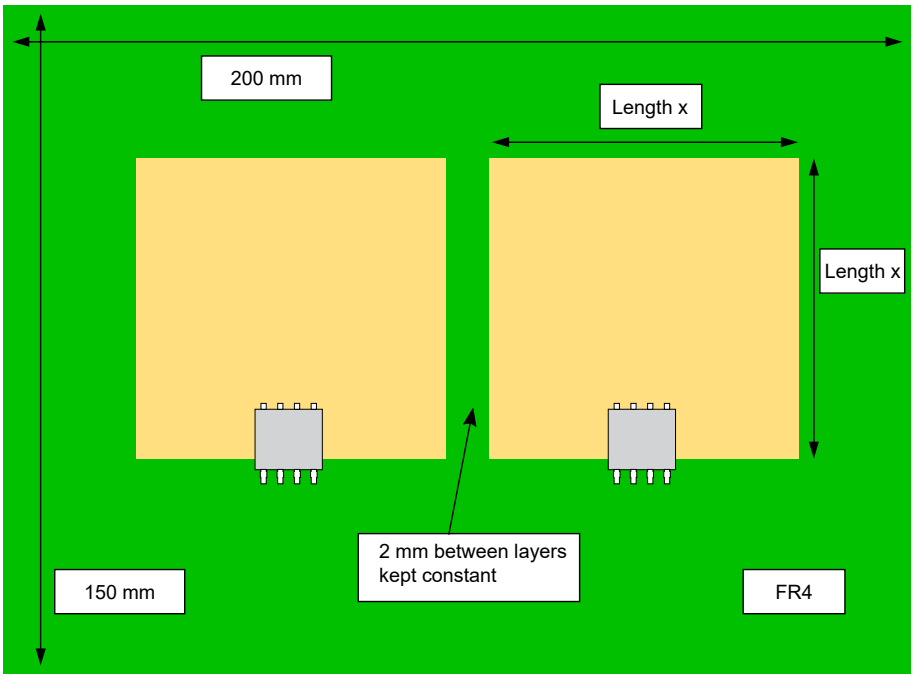


Fig. 22. Copper area configuration: LFPAK33, single top copper layer

The graph in Fig. 24 shows:

- The results for x > 20 mm are similar to the ones observed in section 2.3 (slightly higher +3 °C)
- This is due to the low conductivity of FR4, despite only 2 mm gap it showed no heat transfer from one copper area to the other
- For x < 20 mm results show up to 20 °C higher compared to the results from section 2.3.
- This is due to the MOSFETs being brought closer to each other as a result of reduced copper area – note that in this case the space between MOSFETs is half the space between MOSFETs in the case of LFPAK56D

In Fig. 23 you can see that for x = 10 mm, the distance between the LFPAK33 MOSFETs is approximatively 10 mm. Less than 20 mm apart, the MOSFETs are close enough to heat each other, hence we start to see a temperature difference.

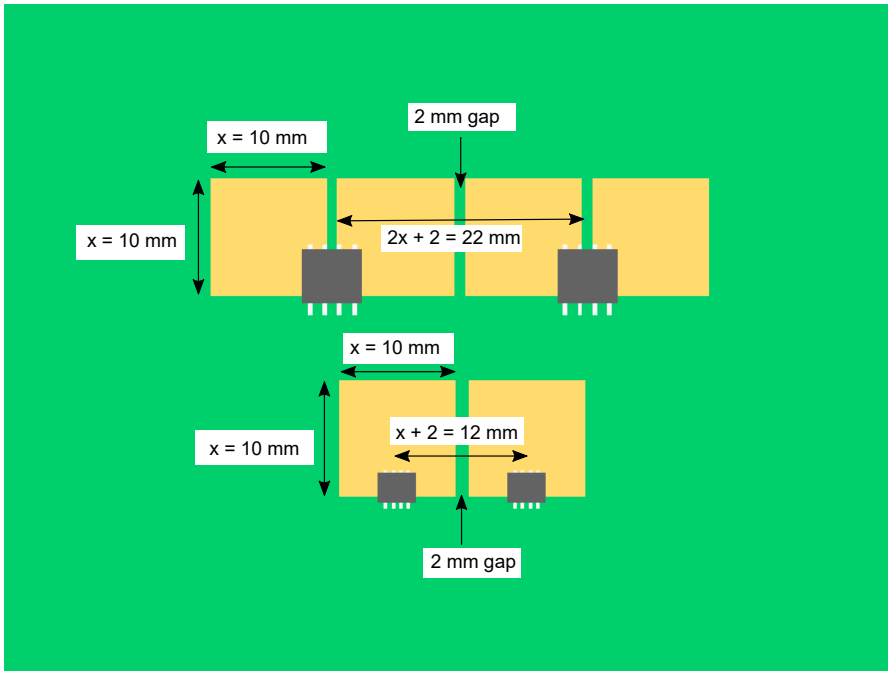


Fig. 23. Copper area configuration: 2 x LFPAK33, 2 x LFPAK56D; separation between MOSFETs

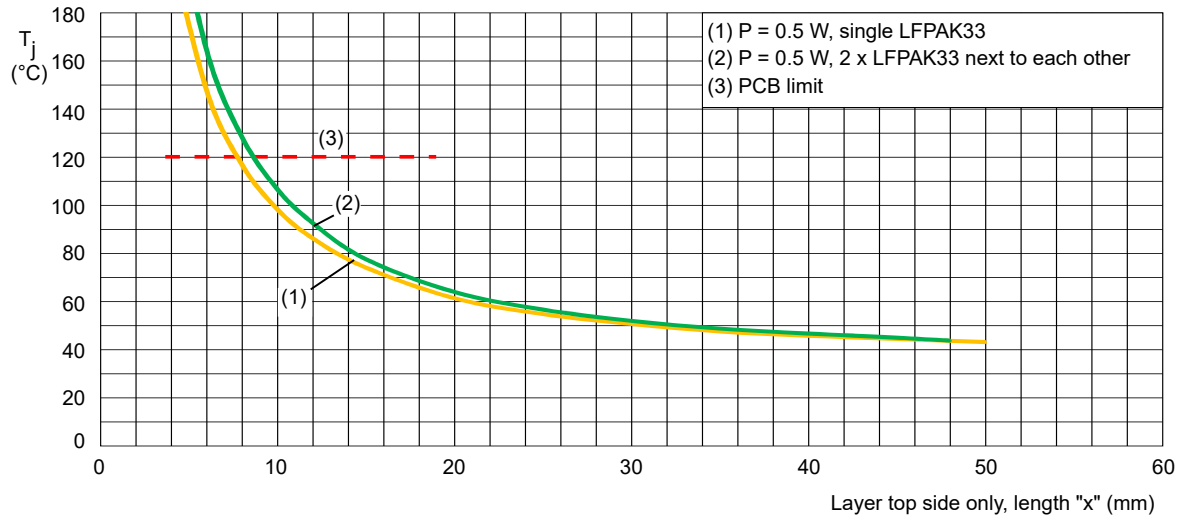


Fig. 24. Junction temperature as a function of copper side length x for 2 LFPAK33

2.4. Comparison between two LFPAK56 and one LFPAK56D, then one LFPAK56D and two LFPAK33

In this section we will present some comparative results for different package devices on a single layer board with varying copper area.

2.4.1. Two LFPAK56 to LFPAK56D

In this section the results of two single LFPAK56 MOSFETs are compared to the results of one dual LFPAK56D MOSFET (see Section 2.1.1)

The aim is to highlight the benefit of using one LFPAK56D dual MOSFET instead of two single LFPAK56 MOSFETs.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- Same gap between copper layer was used for both single LFPAK56 and dual LFPAK56D
- Simulation carried out for different length “x”.
- 0.5 W applied on each MOSFET

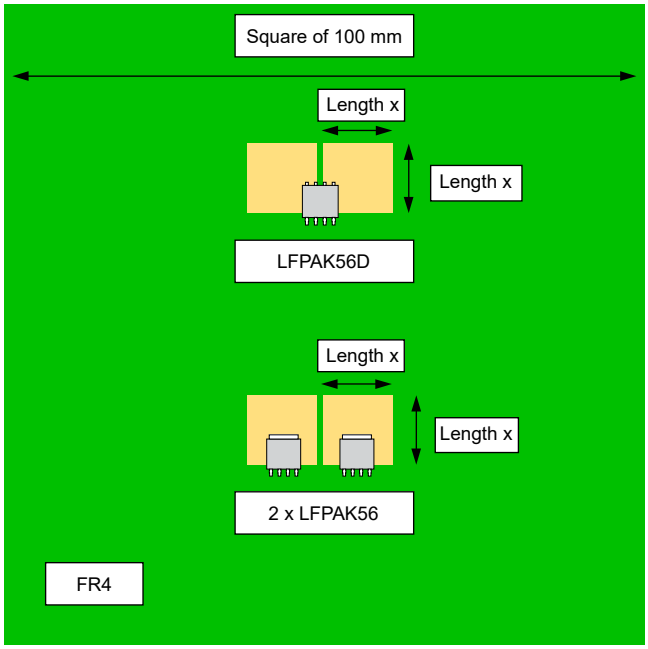


Fig. 25. Copper area configuration: 1 x LFPAK56D, 2 x LFPAK56, single top copper layer

The graph in Fig. 26 shows:

- Overall two single LFPAK56 show better heat dissipation than one dual LFPAK56D by up to approximately 10 °C. This is due to the larger surface area of the LFPAK56 drain tab giving improved heat spreading and thermal dissipation.

- Note that the 10 °C is the relative figure between the two packages, the most important factor is the operating junction temperature
- If there is enough margin before reaching 175 °C at the junction, then LFPAK56D offers an attractive option due to its space saving

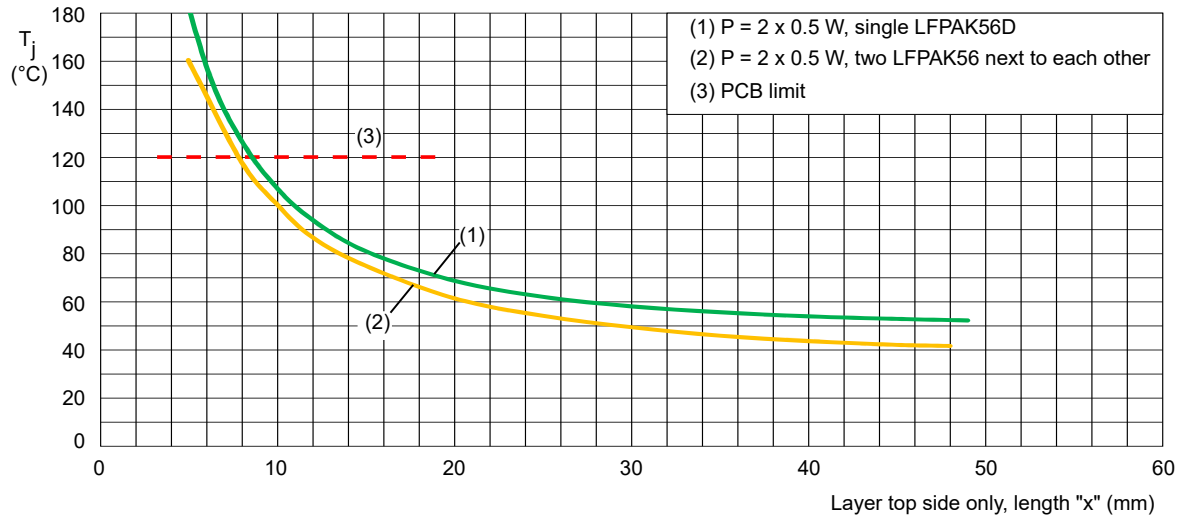


Fig. 26. Junction temperature as a function of copper side length x for 2 LFPAK56 and 1 LFPAK56D

2.4.2. LFPAK56D to two LFPAK33

In this section the results of one dual LFPAK56D MOSFET are compared to the results of two single LFPAK33 MOSFETs (see section 4.2)

Aim is to highlight the benefit of using one LFPAK56D dual instead of two single LFPAK33.

Set-up:

- 1 layer on the top
- MOSFET power dissipation is 0.5 W applied to each MOSFET
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- Maximum PCB operating temperature of 120 °C
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer. In this analysis, we will examine the variation in device junction temperature (T_j) as a function of top copper area.

- Same gap between copper layer was used for both single LFPAK33 and dual LFPAK56D
- Simulation carried out for different length “x”
- 0.5 W applied on each MOSFET

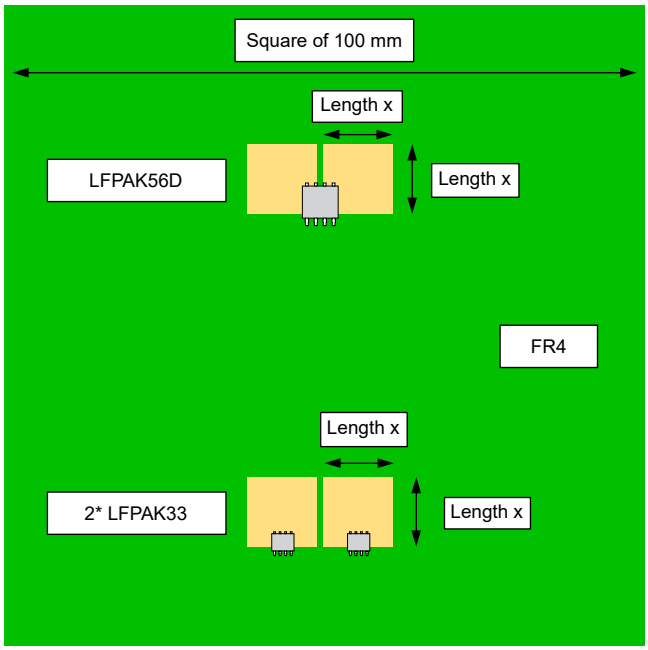


Fig. 27. Copper area configuration: 1 x LFPAK56D, 2 x LFPAK33, single top copper layer

The graph in Fig. 28 shows:

- Overall two single LFPAK33 show better heat dissipation than a dual LFPAK56D by up to approximately 5 °C. This is due to the larger drain surface area of the LFPAK33 offering better thermal dissipation, (less improvement than with LFPAK56 as LFPAK33 is a smaller package).
- Note that the 5 °C is the relative figure between the two packages, the most important factor is the operating junction temperature.
- If there is enough margin before reaching 175 °C at the junction, then LFPAK56D offers an attractive option due to all the advantages that one component offers versus two in terms of PCB layout, placement, cost effectiveness, etc.

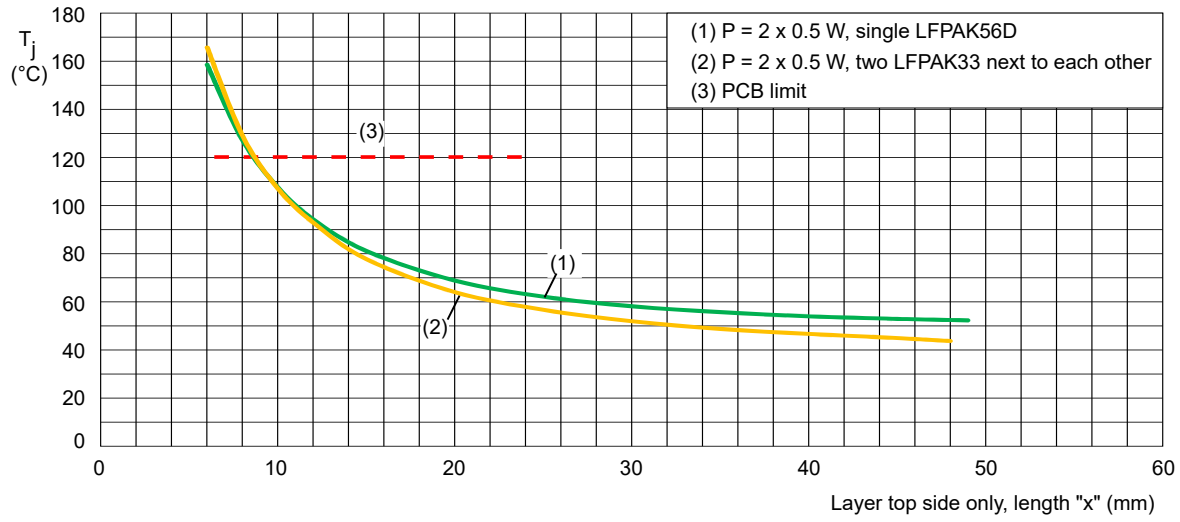


Fig. 28. Junction temperature as a function of copper side length x for 1 LFPAK56D and 2 LFPAK33

2.5. Impact of $R_{th(j-mb)}$ compared to $R_{th(mb-a)}$

Dissipation losses from the MOSFET junction are not mainly limited by the thermal resistance $R_{th(j-mb)}$ as this is very low. The high thermal path for heat dissipation is presented by the thermal resistance $R_{th(mb-amb)}$ (mounting base to PCB to ambient).

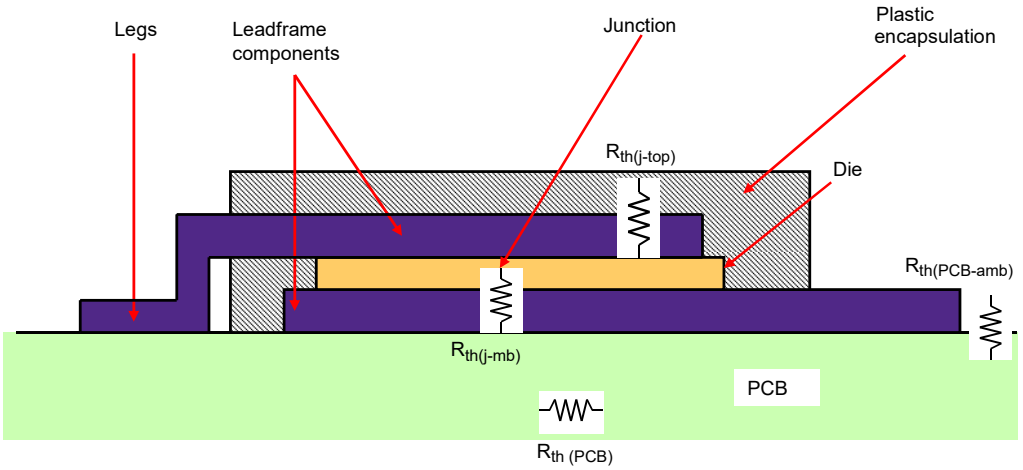


Fig. 29. View of thermal resistances in and outside the MOSFET

Example: for the part number BUK7M15-60E (LFPAK33, 15 mΩ, 60 V) the maximum thermal resistance junction to mounting base is 2.43 K/W:

Table 3. Thermal resistance BUK7M15-60E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.01	2.43	K/W

Using thermal simulation (Flotherm) with the following conditions:

0.5 W of losses in the MOSFET, air ambient is 20 °C, 35 µm copper, we can calculate some thermal resistance.

- $R_{th(j-mb)}$ is 0.8 K/W
  - This is a lower value than given in the data sheet due to the simulation using ideal conditions
- As can be seen in Table 4 below, thermal resistance for other items have high value compared Rth j-mb
- The total thermal resistance, junction to ambient, is 59.4 K/W when using 65.4 °C as (ambient) reference point.

Table 4 lists temperatures for different points captured in the simulation and shown in Fig. 30.

Table 4. Breakdown of thermal resistance for a simple case

Thermal resistance part	Temperature (°C)	R_{th} (K/W)
Junction	95.1	-
Mounting base	94.7	0.8
PCB under MOSFET	88.6	12.2
PCB to the right of the MOSFET	86.6	4
Ambient air 0.5 mm over the top of the PCB	79.1	15

Thermal resistance part	Temperature (°C)	R_{th} (K/W)
Ambient air 1 mm over the top of the PCB	65.4	27.4

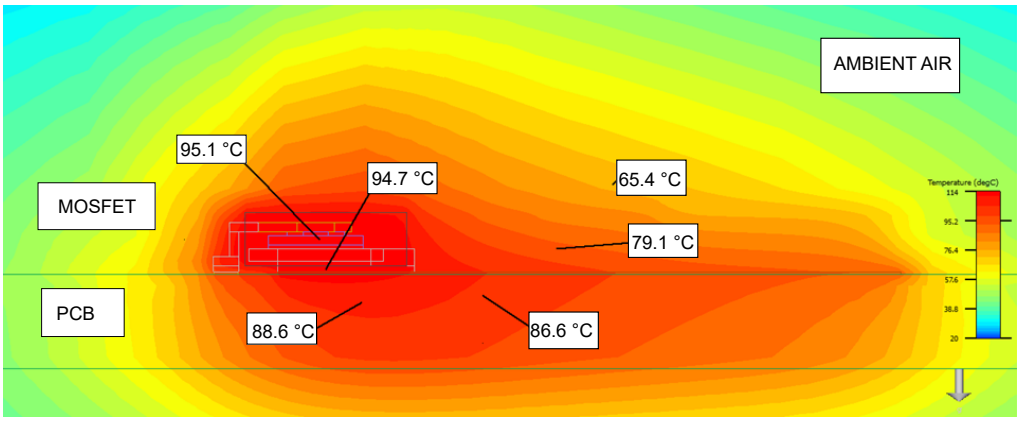


Fig. 30. Thermal result, LFPAK33, 0.5 W, 20 °C ambient

Due to the very low thermal resistance between junction and mounting base it is very important to take care of design surrounding the MOSFET, (i.e. thermal vias, copper area, heat sink, water cooling, air cooling), in order to reduce the total thermal resistance.

3. LFPAK56 and LFPAK88

3.1. Simple configuration with a single layer

In this section, we will present the maximum power dissipation results for a simple PCB configuration using a single layer with varying copper area.

Results are given for the LFPAK56 and LFPAK88 packages. Models used are based on 1 mΩ LFPAK56E and LFPAK88.

3.1.1. Set-up:

- 1 copper layer on the top
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Fig. 31.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area and calculate the maximum power that can be safely dissipated in the MOSFET to reach a T_j of 175 °C.

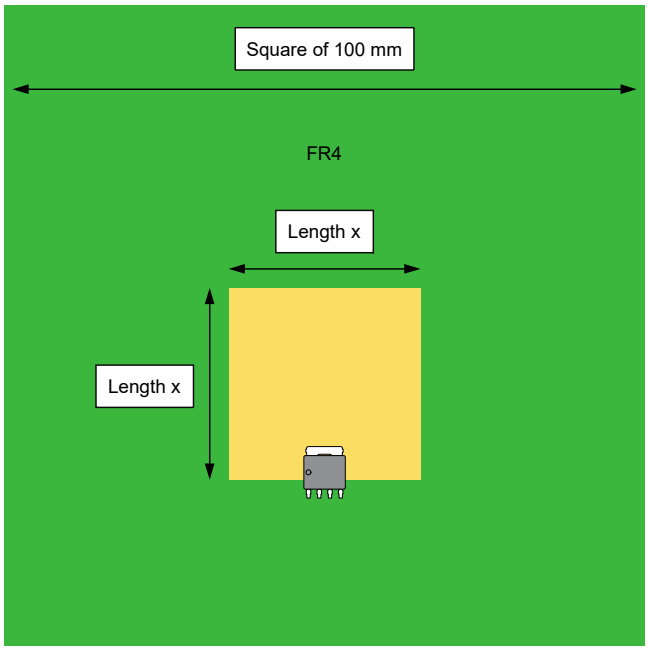


Fig. 31. Copper area configuration: LFPAK56, single top copper layer, the configuration is the same for LFPAK88

3.1.2. Junction temperature as a function of copper area

The graphs in Fig. 32 and Fig. 33 capture two important factors:

- T_j depends greatly on length “x” and thus copper area, the bigger the area the better the thermal performance
- However, the ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”. In other words, we cannot keep on adding more copper area in the hope of continuing to reduce T_j. As can be seen from Fig. 32 below, for LFPAK56, 1 W profile, T_j will plateau at around 55 °C.

Note: Standard FR4 PCBs operate at a maximum temperature of 120 °C, care must be taken for T_j > 120 °C as the PCB area directly under the transistor will be close to the MOSFET junction temperature, (due to low $R_{th(j\text{-}mb)}$).

The graphs below also shows the absolute minimum copper area needed for $T_j \leq 175$ °C.

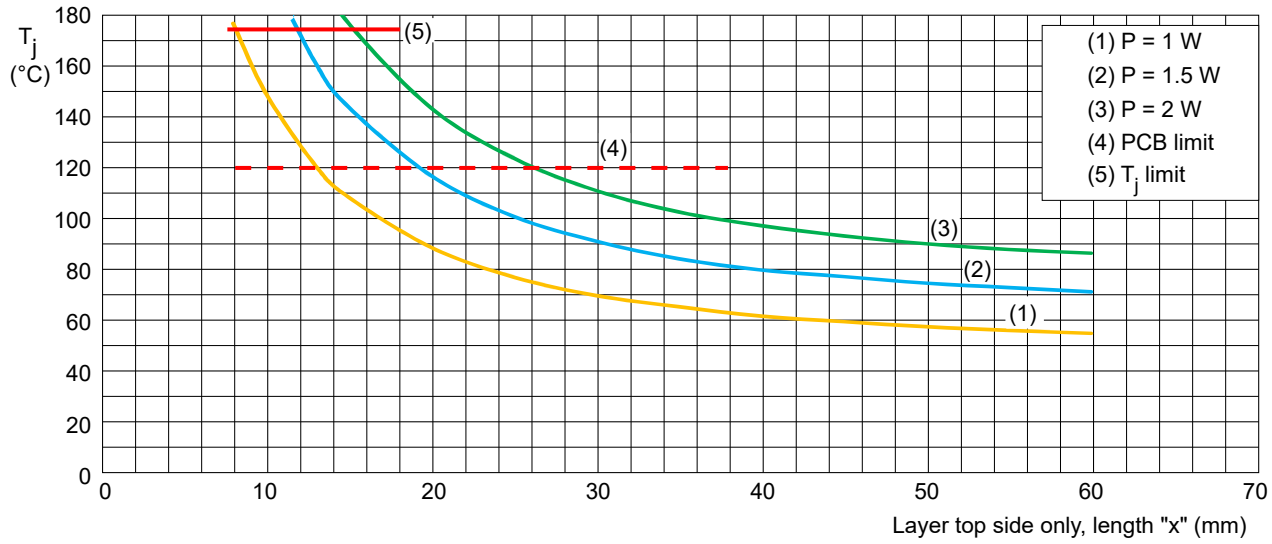


Fig. 32. Junction temperature as a function of copper side length x for LFPAK56

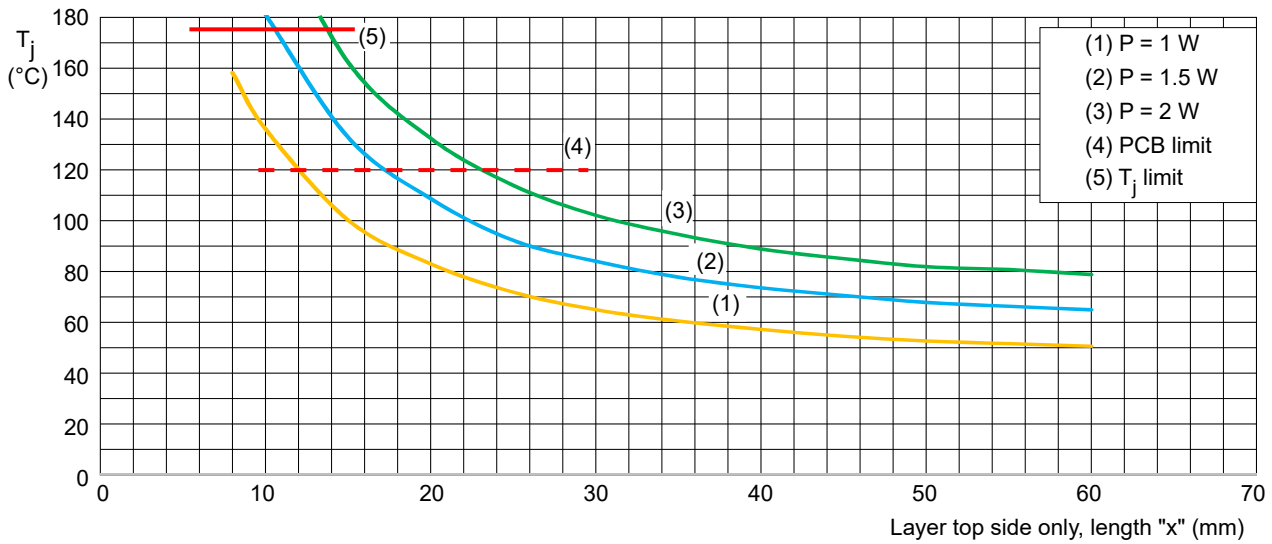


Fig. 33. Junction temperature as a function of copper side length x for LFPAK88

3.1.3. Maximum allowed power dissipation as a function of copper area

The maximum allowed power dissipation is shown in Fig. 34 and Fig. 35 below, for different ambient temperature and copper side length. In this example the PCB temperature was not considered so care must be taken for the resulting heat on the PCB.

From graphs in Fig. 34 and Fig. 35 the maximum permissible power, (T_{amb} = 20 °C), is 5.05 W and 5.9 W for the LFPAK56 and LFPAK88 packages respectively:

Table 5. Maximum power dissipation

Device	T_{amb} = 20 °C	T_{amb} = 80 °C
LFPAK56	5.05 W	3.2 W
LFPAK88	5.9 W	3.8 W

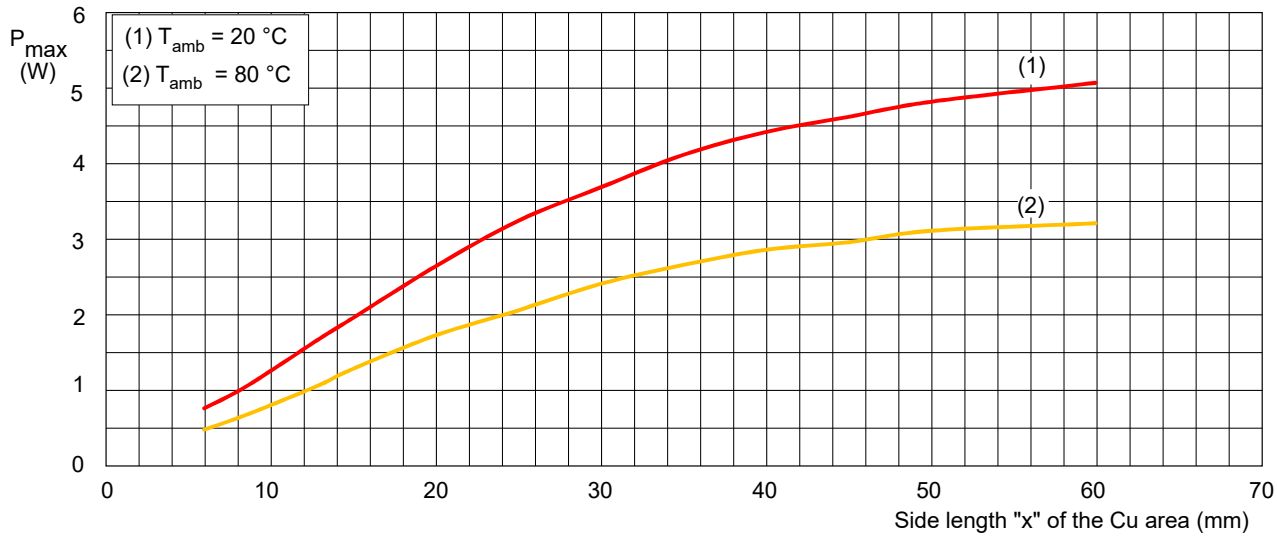


Fig. 34. Maximum permissible power dissipation as a function of copper side length “x” for LFPAK56

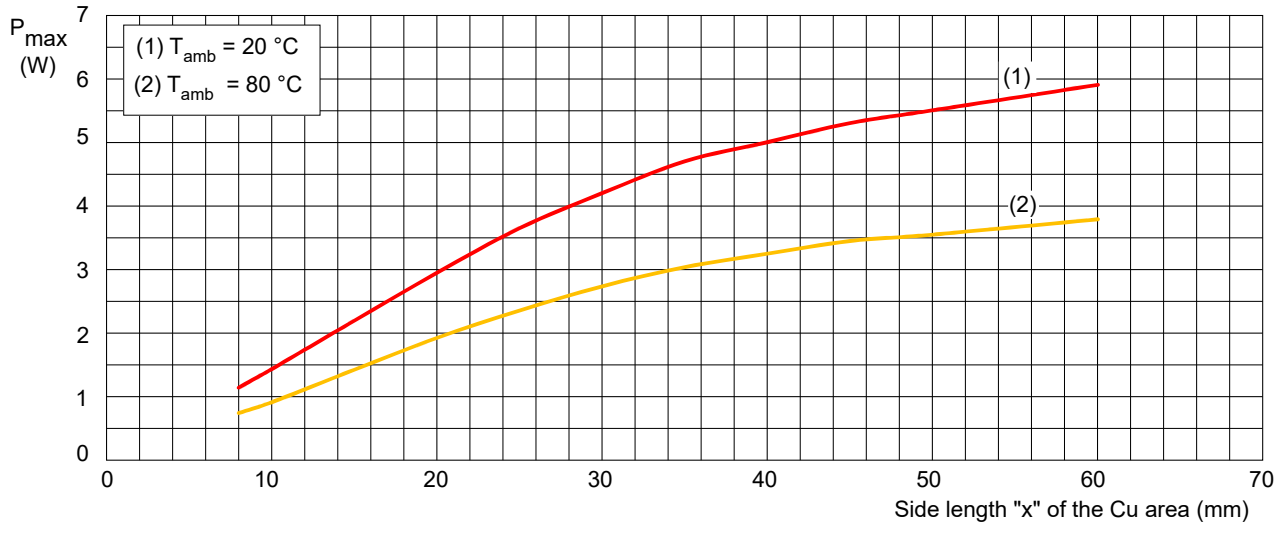


Fig. 35. Maximum permissible power dissipation as a function of copper side length “x” for LFPAK88

3.2. Usual configuration: 4 layers + vias

In this section, we will present the maximum power dissipation results for a PCB configuration using 4 layers + vias for dissipation on the bottom layer, with varying copper area.

Results are given for the LFPAK56 and LFPAK88 packages.

3.2.1. Set-up:

- Four layers with vias (max number of vias is 25 and for small copper areas this number will decrease accordingly, see Table 6)
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness of all layers is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The common PCB stack-up is 4 layers with vias under the MOSFET to create a dissipation path to heatsink (no heat sink was used in simulation).

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of copper area (same area size applied to all layers).

The configuration of the vias is shown below in Fig. 36 and Fig. 37:

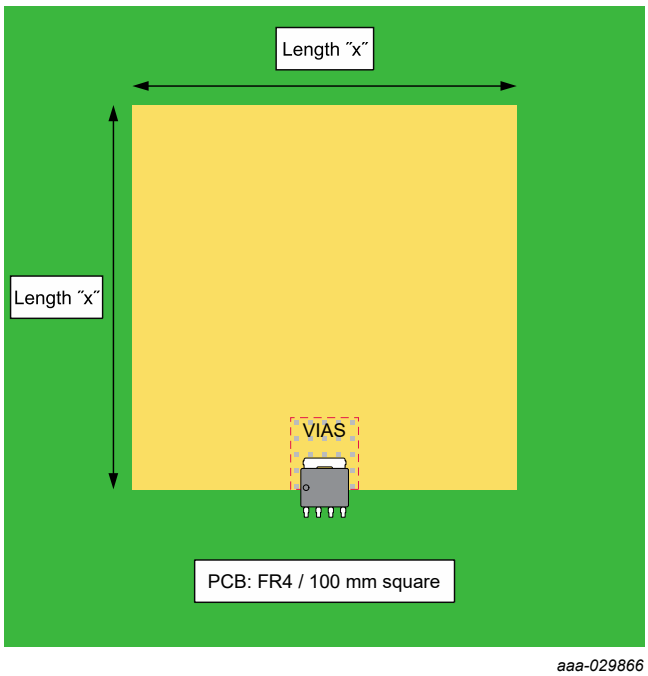
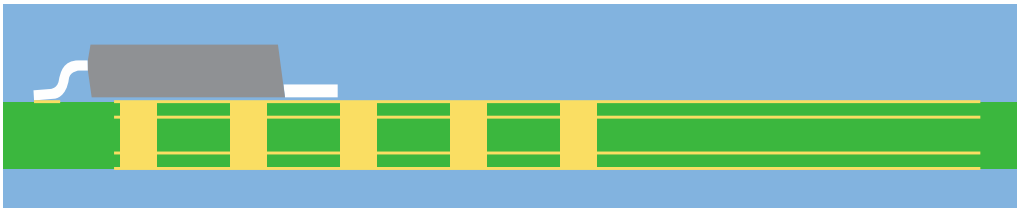


Fig. 36. Copper area configuration: LFPAK56, 4 layers with vias, the configuration is similar for LFPAK88



aaa-029867

Vias configuration: square vias used for ease of simulation.

Fig. 37. Sectional view: LFPAK56

Table 6. Limitation of number of vias

X (mm)	Vias configuration	Comments	Vias information
6	9 vias	Maximum number of vias able to be inserted in the copper area	Square vias: length 0.7 mm Vias pitch: 2.5 mm (between vias in columns) 2.0 mm (between vias in rows) Copper thickness 70 µm No solder fill
8			
10	20 vias		
15	25 vias	25 vias maximum	
20	25 vias		
25	25 vias		
30	25 vias		
35	25 vias		
40	25 vias		
45	25 vias		
50	25 vias		
60	25 vias		

3.2.2. Junction temperature as a function of copper area (4 layers and vias)

The graphs in Fig. 38 and Fig. 39 below show the junction temperature as a function of drain copper area following the same trend as the single layer PCB configuration in that:

- T_j depends greatly on copper area
- The ability of the top copper to provide heatsinking for the MOSFET shows a “law of diminishing returns”.

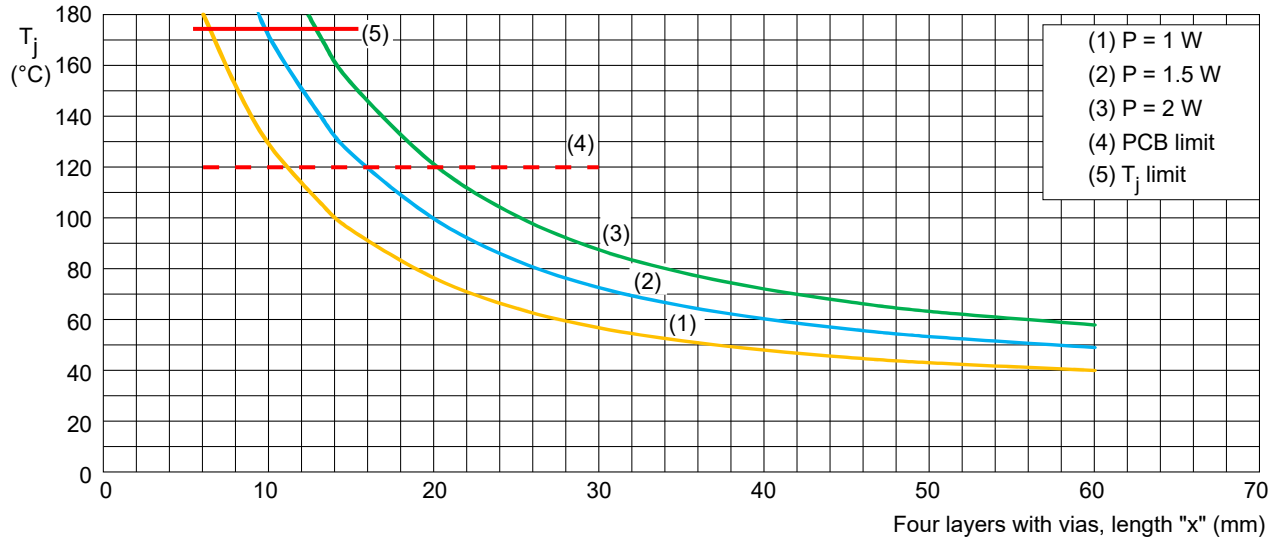


Fig. 38. Junction temperature as a function of copper side length x for LFPAK56

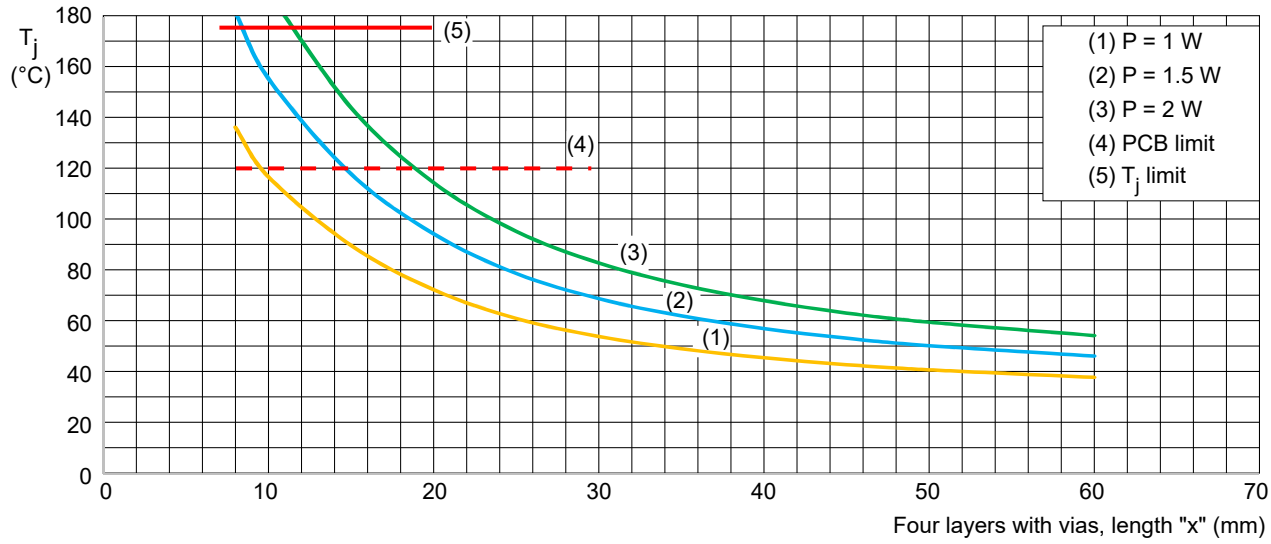


Fig. 39. Junction temperature as a function of copper side length x for LFPAK88

3.2.3. Maximum allowed power dissipation as a function of copper area (4 layers and vias)

From graphs in Fig. 40 and Fig. 41 the maximum power for a given package and conditions are as follows:

Table 7. Maximum power dissipation

Device	T_{amb} = 20 °C	T_{amb} = 80 °C
LFPAK56	9.6 W	6.3 W
LFPAK88	10.65 W	6.9 W

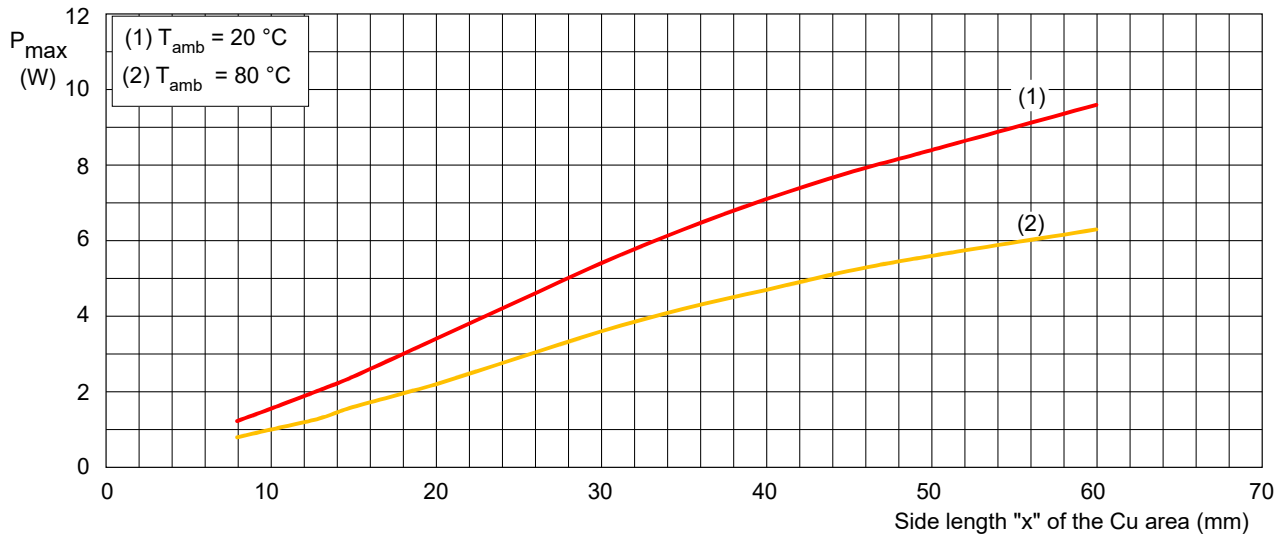


Fig. 40. Maximum permissible power dissipation as a function of copper side length “x” for LFPAK56

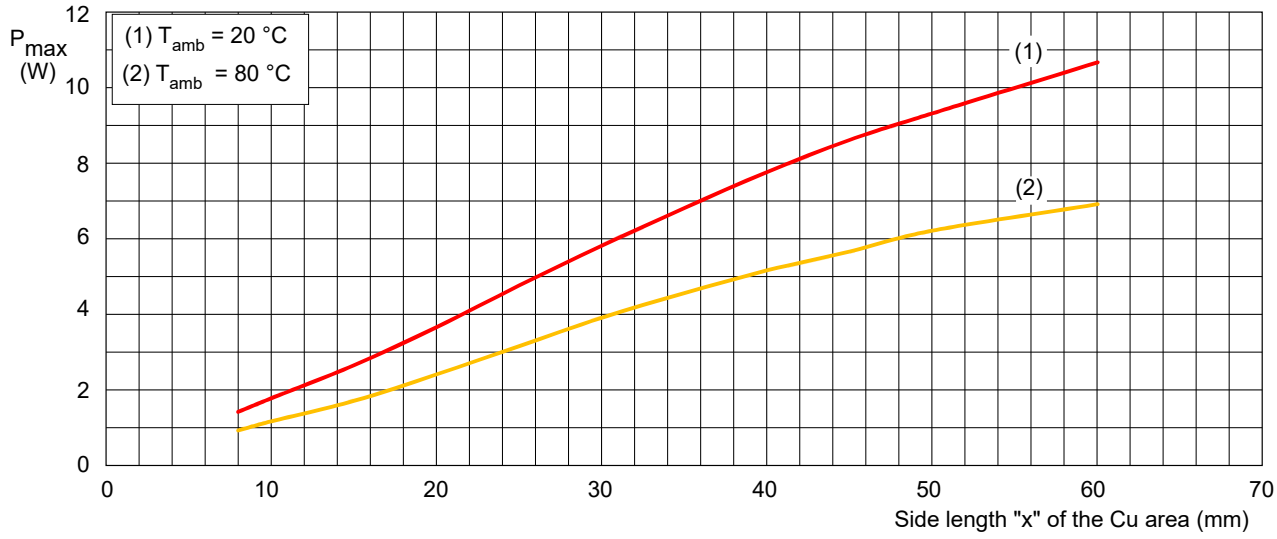


Fig. 41. Maximum permissible power dissipation as a function of copper side length “x” for LFPAK88

3.3. Simple configuration with a single split layer of copper

In this section, we will present the maximum power dissipation results as per the previous section for a simple PCB configuration using a single layer and varying copper area, but with copper layer split in two part (one part placed under the drain tab of the MOSFET and the other under the source pins).

Results are given for the LFPAK88 package only.

3.3.1. Set-up:

- 1 copper layer on the top - split into two areas:
  - 3/5 of area under drain tab
  - 2/5 of area under source pins
- MOSFET power dissipation is 1 W, 1.5 W and 2 W
- Maximum junction temperature of 175 °C
- PCB material is standard FR4, 1.6 mm thickness, dimension 100 x 100 mm
- PCB operating temperature of 120 °C and T_j of 175 °C are highlighted in graphs
- Copper thickness is 2 oz./ft^2 (70 µm)
- The PCB is suspended in free air at ambient temperature of 20 °C
- The simulation is carried out for conduction, convection and radiation heat transfer
- There is no forced air cooling applied, i.e. only natural convection is modeled

The simplest possible PCB stack-up is that of a single top copper layer, see Fig. 42.

In this analysis, we will examine the variation in device junction temperature (T_j) as a function of the top copper area.

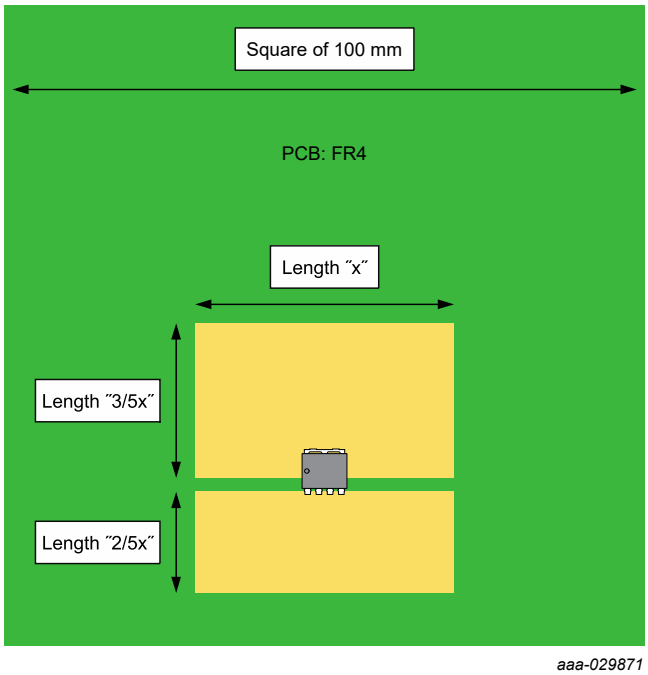


Fig. 42. Split copper area configuration: LFPAK88, single top layer with copper

The graph in Fig. 43 captures what has been previously mentioned in terms of copper area and heat dissipation i.e. the bigger the area the better the thermal performance. More importantly in this configuration, it shows the importance in considering the source pins of an LFPAK MOSFET as a thermal path for efficiently dissipating heat.

The graph in Fig. 43 also shows that coper area of length “x” = 40 mm in split copper configuration provides a performance equivalent of that provided in the solid (non-split) copper area of length “x” = 60 mm.

Split copper configuration for length “x” = 40 mm is as follows:

- 24 mm x 40 mm copper area placed under the drain tab of the LFPAK MOSFET
- 16 mm x 40 mm copper area placed under the source pins of the LFPAK MOSFET

Note: Standard FR4 PCBs operate at maximum temperature of 120 °C, care must be taken for T_j > 120 °C as PCB area directly under the transistor would be close to the MOSFET junction temperature (due to low $R_{th(j\text{-}mb)}$).

Results are for LFPAK88, but the principle applies to all Nexperia clip bond LFPAK devices. T_{amb} = 20 °C: Max power of ~6 W is achieved with an area of 40 mm x 40 mm single copper layer in split configuration, whist previously shown to require an area of 60 mm x 60 mm for single solid copper layer.

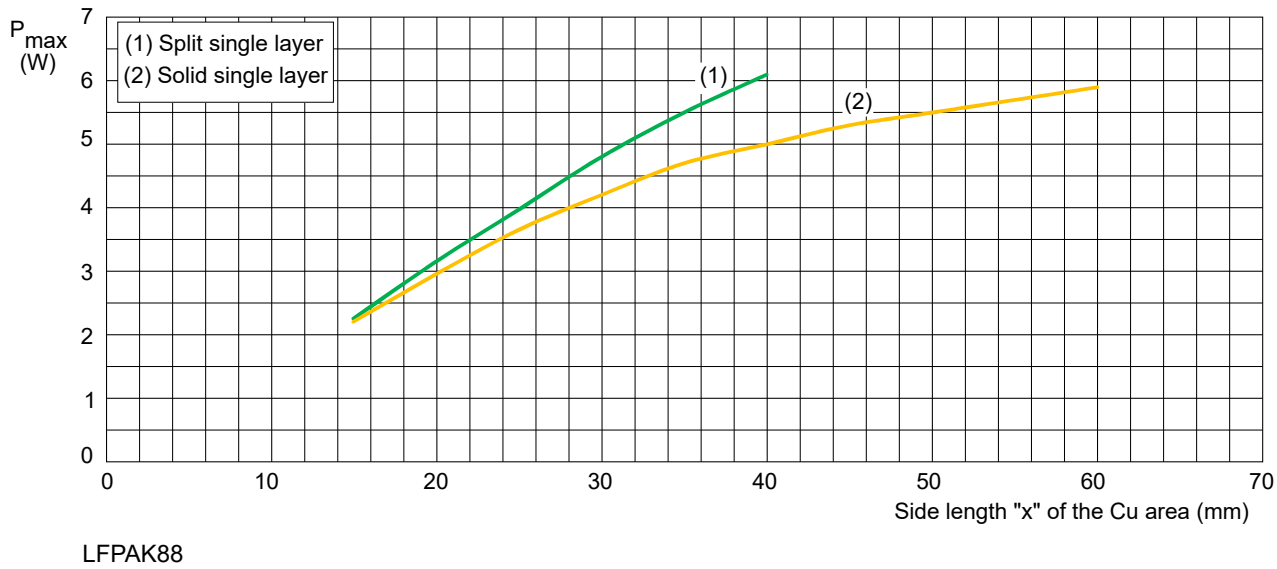


Fig. 43. Maximum permissible power dissipation as a function of copper side length “x” for LFPAK88

3.4. Impact of $R_{th(j-mb)}$ compared to $R_{th(mb-amb)}$

The thermal resistance $R_{th(j-mb)}$ of the MOSFET is very low and therefore dissipation losses are mainly limited by the high thermal resistive path presented by $R_{th(mb-amb)}$ (mounting base to ambient).

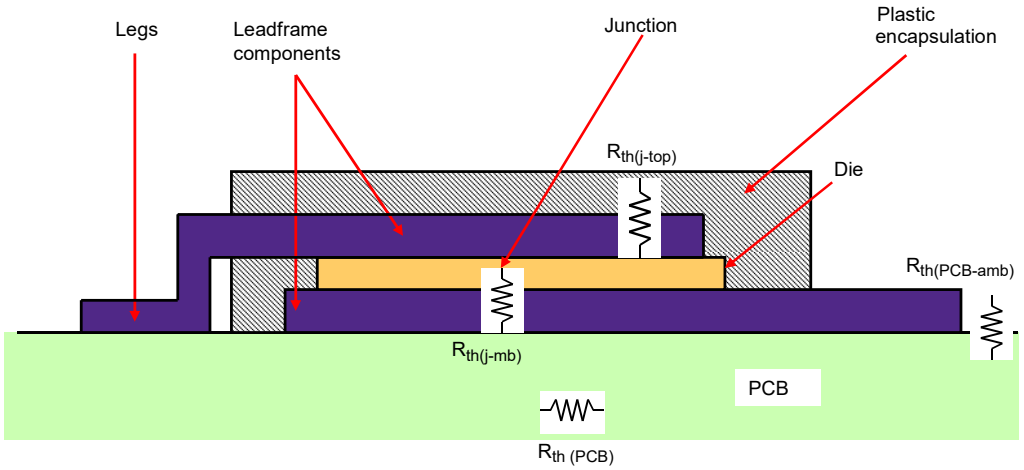


Fig. 44. View of thermal resistances in and outside the MOSFET

Example: for the part number BUK7S1R0-40H (LFPAK88, 1 mΩ, 40 V) the maximum thermal resistance junction to mounting base is 0.4 K/W, see Table 8:

Table 8. Thermal resistance BUK7S1R0-40H

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.35	0.4	K/W

Using thermal simulation (Flotherm) with the following conditions:

- 1 W of losses in the MOSFET
- Ambient air temperature of 20 °C
- 70 µm copper

we can calculate the thermal resistance for different paths, example:

- 1 W of losses in the MOSFET
- Junction temperature = 52.2 °C
- Mounting base temperature = 52.0 °C
- $R_\Theta = \Delta T / P \Rightarrow R_{th(j-mb)} = 0.2$ K/W.

This is lower than the measured value given in the data sheet due to simulation using ideal conditions.

As can be seen in Fig. 45 below, the thermal resistance between mounting base and ambient is of much higher value (~30 K/W) than $R_{th(j-mb)}$.

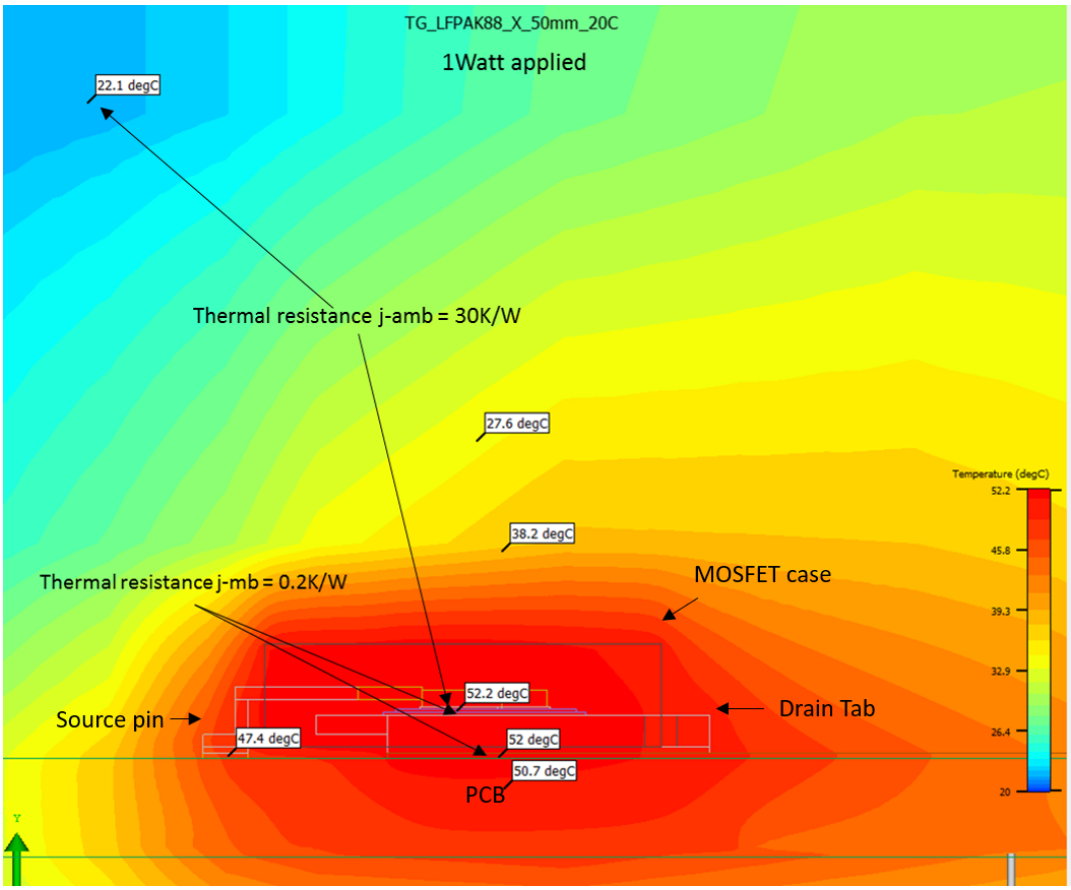


Fig. 45. Thermal resistance LFPAK88: single layer copper profile (50 x 50 mm)

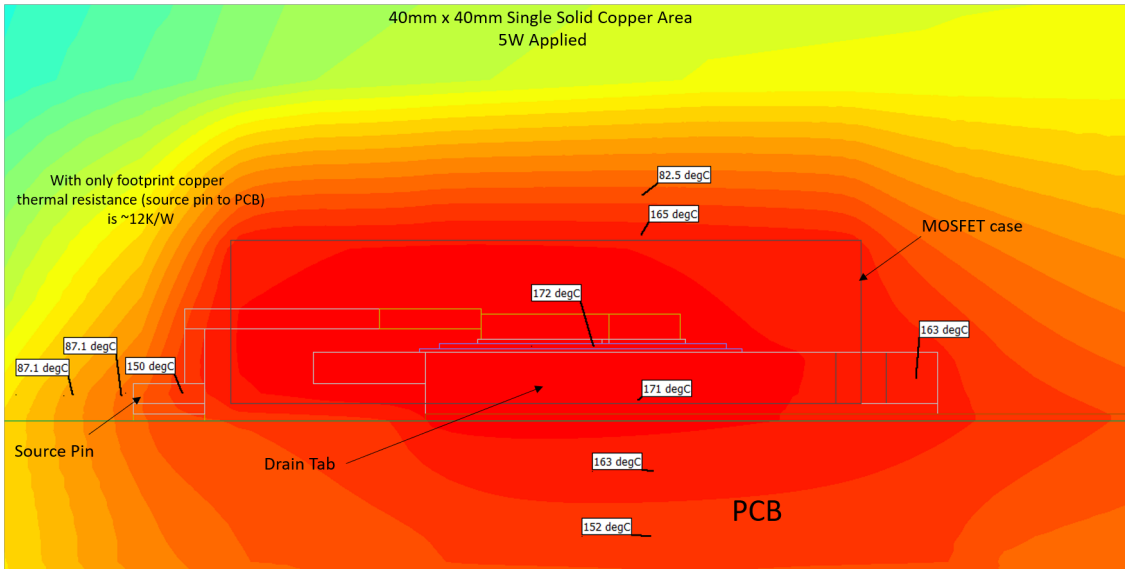


Fig. 46. Thermal resistance LFPAK88: single layer copper profile (40 x 40 mm)

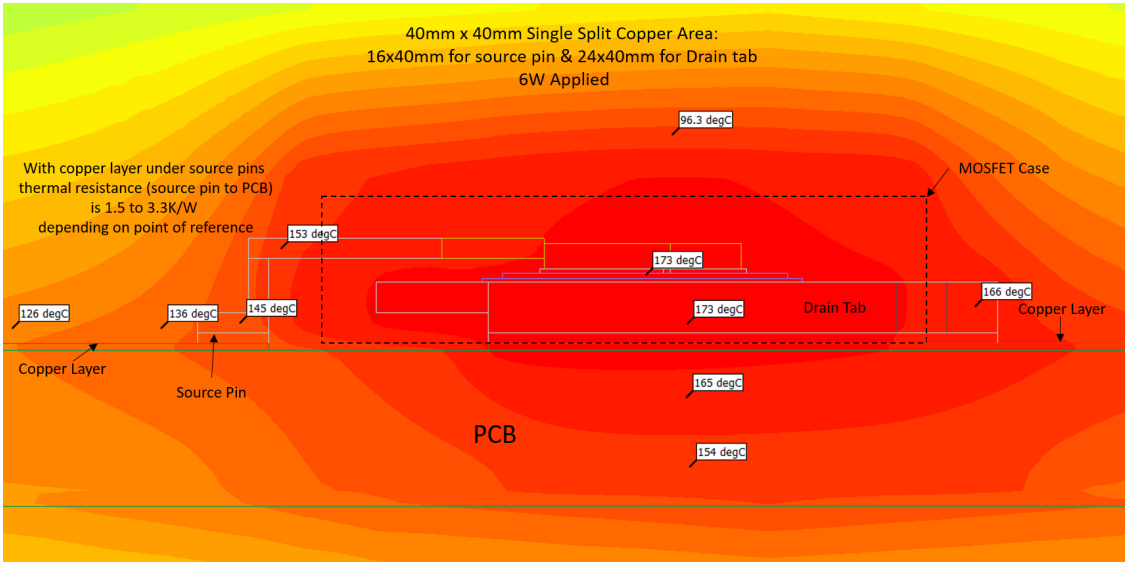


Fig. 47. Thermal resistance LFPAK88: single split layer copper profile (40 x 40 mm: split into 24 x 40 mm and 16 x 40 mm)

4. Conclusion

All the LFPAK packages offer a very good junction to mounting base thermal performance, meaning that the mounting base can be near to the junction temperature, but this is often limited by the PCB high temperature capability.

It is very important for designs to reduce the thermal resistance between mounting base and the ambient environment as this will present the bottleneck in heat dissipation. All of Nexperia LFPAK packages use clip bond technology making their source pins a good thermal path in addition to the thermal path provided by the drain tab. To take full advantage of this feature, it is important for PCB layout designs to consider placing a good amount of copper under the source pins. The drain tab still presents the main thermal path for heat dissipation and should be the focus for any thermal design layout.

In all cases a configuration with 4 layers with vias substantially improves the heat dissipation.

This thermal guide establishes the necessary principles in thermal design approaches, combined with LFPAK packages features (i.e. low $R_{th(j\text{-}mb)}$ and source clip bond) offer the designer good options in optimizing PCB thermal design.

Good thermal design practices should be applied to take advantage of the very good thermal performance LFPAK packages and $T_{j(max)}$ must be kept < 175 °C for safe operation.

5. Revision history

Table 9. Revision history

Revision number	Date	Description
2.0	2019-05-09	Additional section added for LFPAK56 and LFPAK88. Formatting of graphs updated.
1.0	2019-02-04	Initial version of the document

6. Legal information

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List of Tables

List of Figures

Contents

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