Avnet UltraZed
Board Definition File Installation and Tutorial
(Vivado 2016.2)

Version 1.0

December 2016

1 Installing the UltraZed-EG Board Definition Files

Please unzip the **ultrazed_board_definition_files_v2016_2.zip** file to the following folder of the Vivado 2016.2 install directory.

<install_location>\Vivado\2016.2\data\boards\board_files

> **Note**: If you are using the UltraZed-EG SOM with ES1 silicon, you must follow the instructions on the Getting Started Card ship with the kit to install the ES1 license file before proceeding to the next step.

2 Creating a Hardware Platform

Once the Avnet Board Definition Files are installed, they can be used to generate a Zynq UltraScale+ MPSoC based design. Please follow the steps shown below to generate the hardware platform for this tutorial using the Avnet Board Definition Files in Vivado 2016.2 tool.
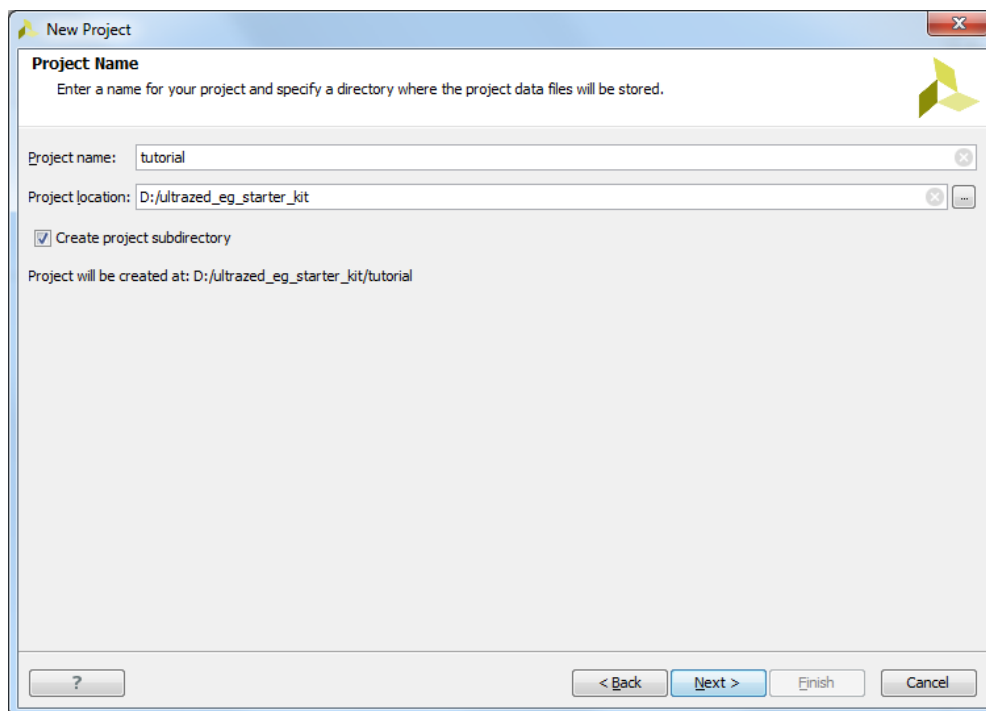
- Start the Vivado tool via **Start > All Programs > Xilinx Design Tools > Vivado 2016.2 > Vivado 2016.2**
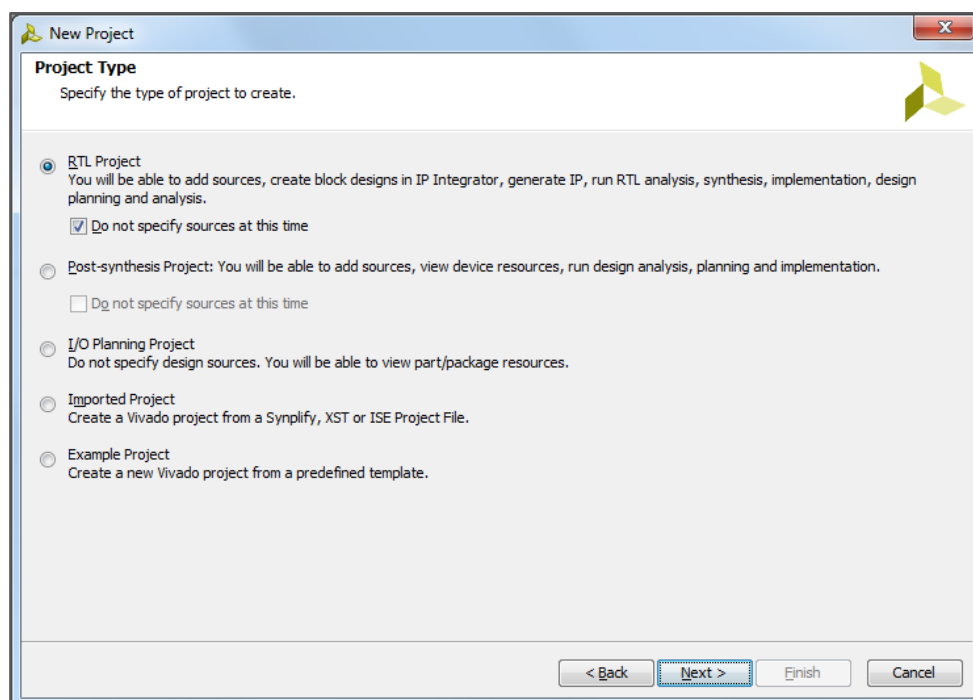
- Select **Create New Project**.
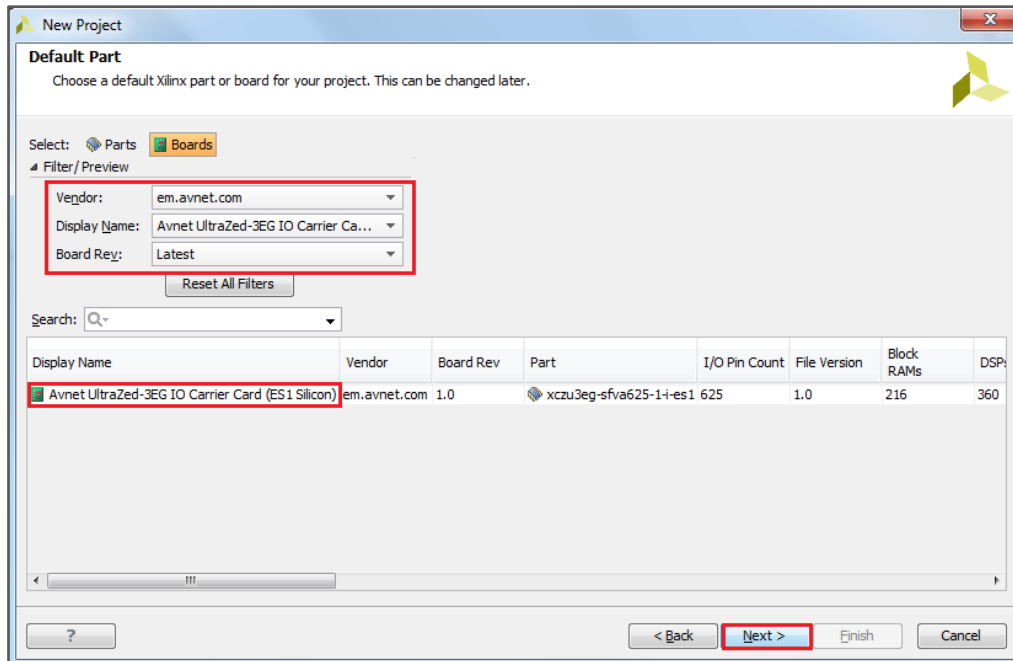

- Click **Next** to continue.

- Set the project name and location and click **Next** to continue. In this case, the project location is set to **D:/ultrazed_eg_starter_kit** and the project name is set to **tutorial**. Make sure the **Create project subdirectory** box is checked as shown in the following figure.
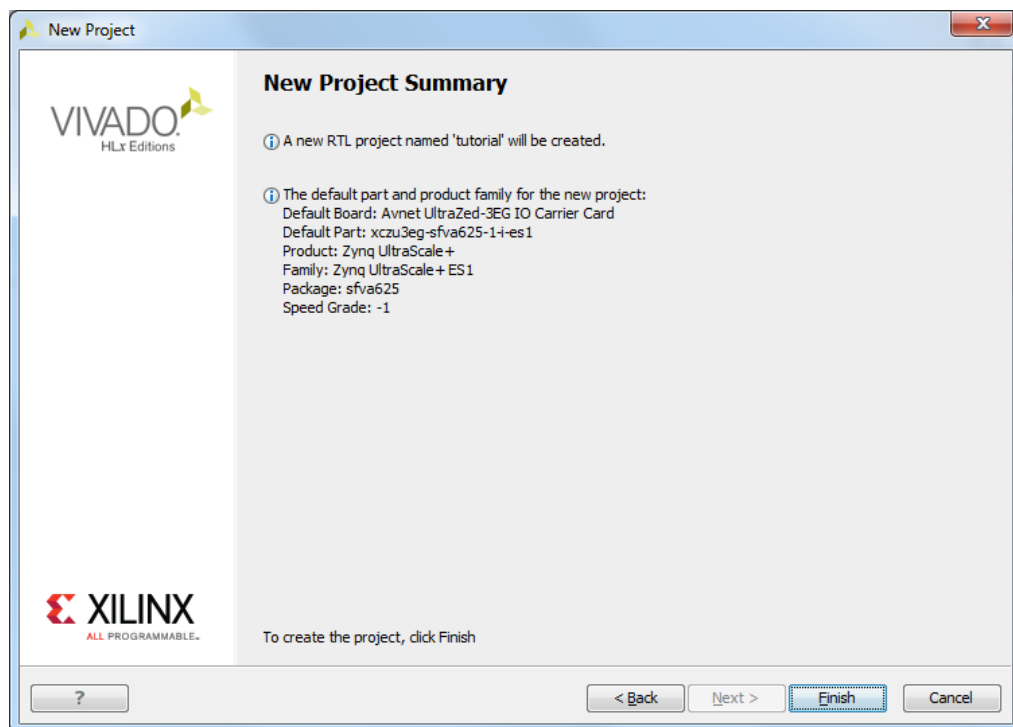

- Select the **RTL Project** type and make sure the **Do not specify sources at this time** box is checked as shown in the following figure. Click **Next** to continue.
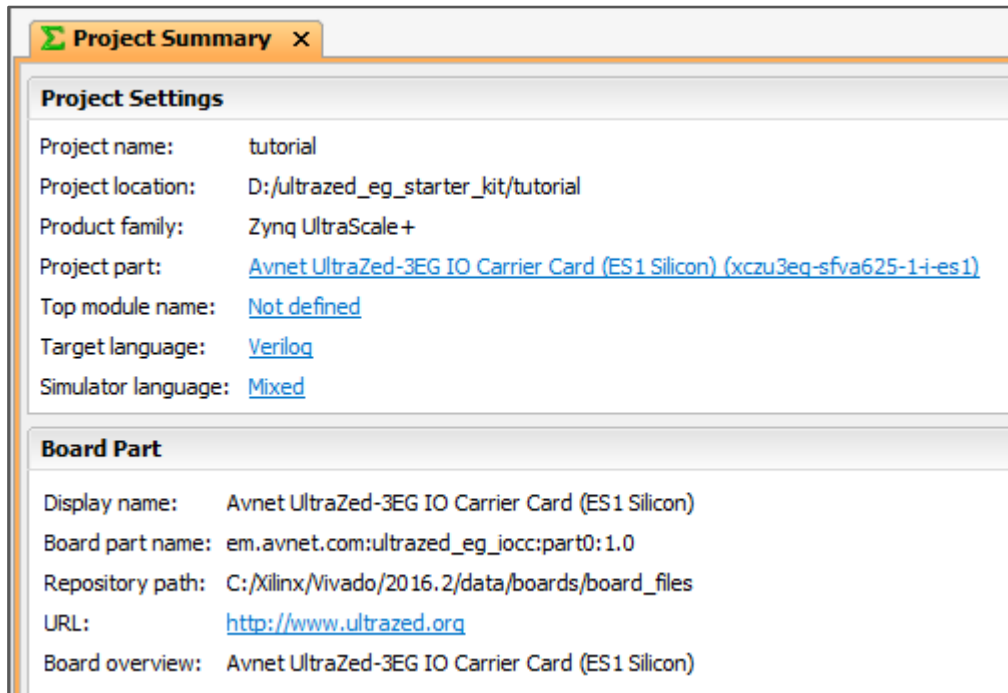
- In the **Default Part** dialog box
  a. Click on **Boards** next to **Select:** as shown below.
  b. Set the **Vendor** to **em.avnet.com**.
  c. Set the **Display Name** to **Avnet UltraZed-3EG IO Carrier Card (ES1 Silicon)**. Set the **Display Name** to **Avnet UltraZed-3EG IO Carrier Card** when using the UltraZed-EG SOM with production silicon.
  d. Set the **Board Rev** to **Latest**.
  e. Click **Next** to continue.

- In the **New Project Summary** dialog box, click **Finish** to continue.
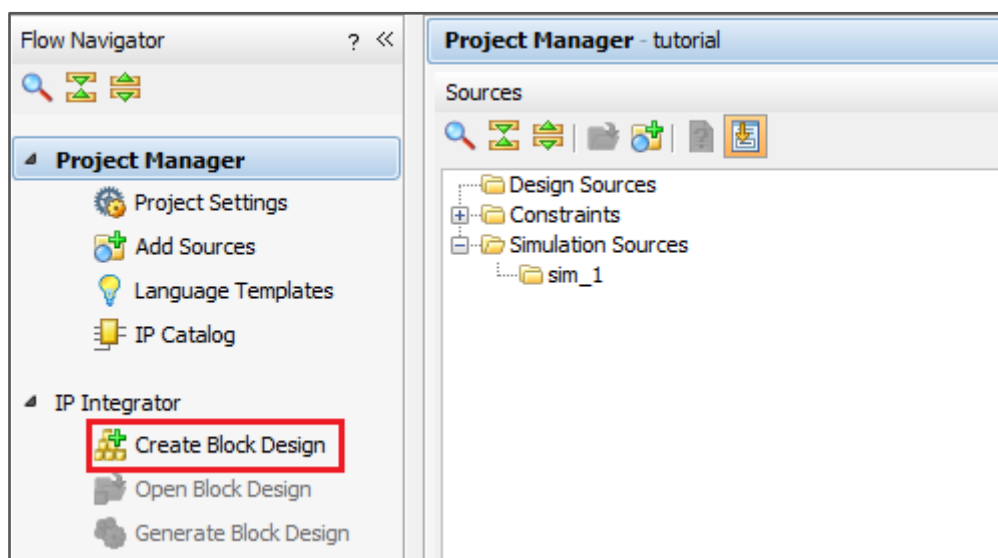
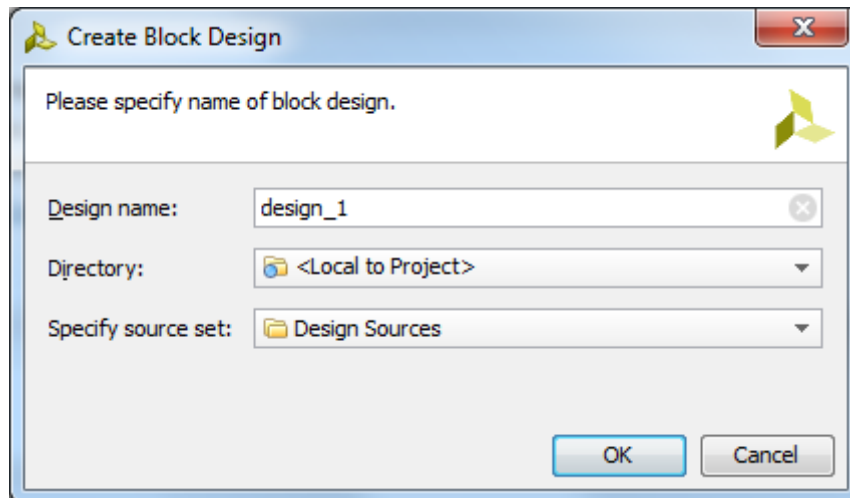The Vivado **Project Summary** should look as shown in the following figure.

2.1 Creating a Block Design

In this section we will be creating a Block Design for the hardware platform. Once the Block Design canvas is created, IP cores can be added to the design form the Vivado **IP Catalog**.

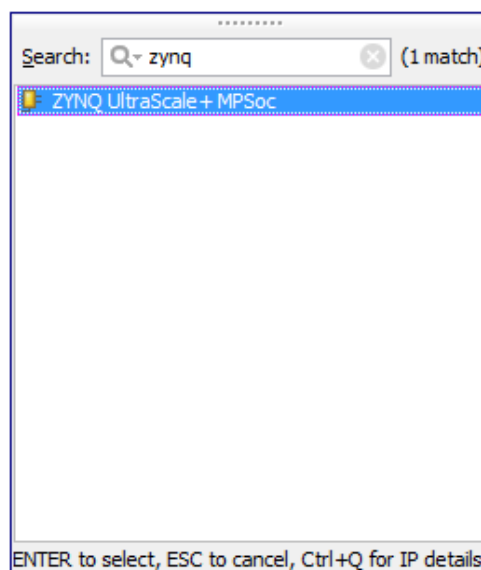- Click on the **Create Block Design** as shown in the following figure.

- When the following dialog box appears, click **OK** to continue. You may change the default **design_1** name to anything you wish. We will be using the default name for this tutorial.
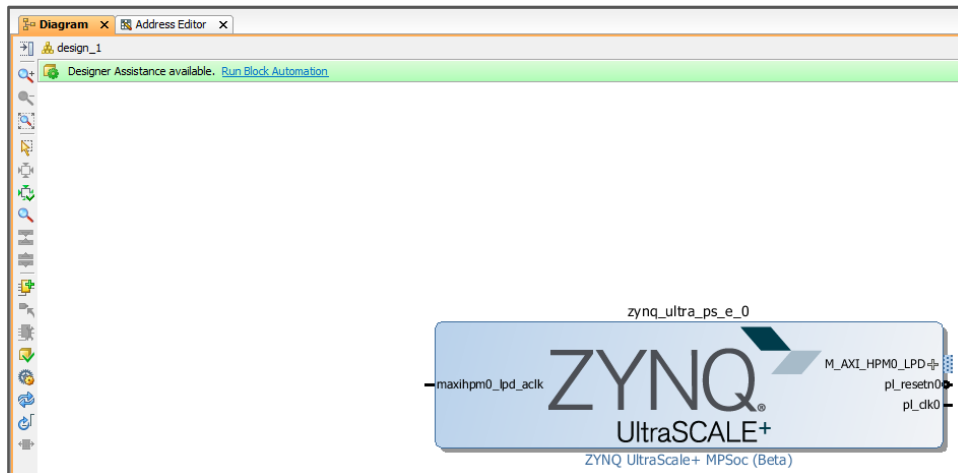

- Click on the **Add IP** icon in the white canvas area as shown in the following figure to begin adding IP cores to the design.
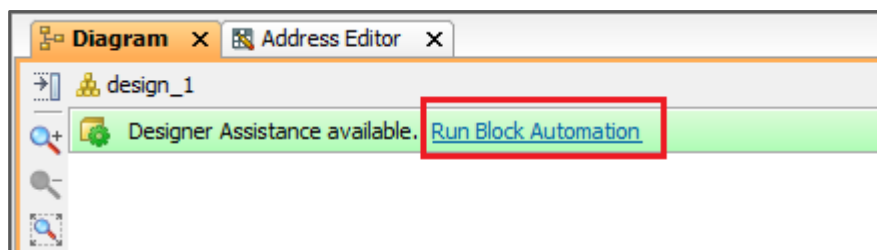

- The first step is to add the Zynq IP core to the design. Type **Zynq** in the **Search** box and then double-click on the **ZYNQ UltraScale+ MPSoC** as shown in the following figure.
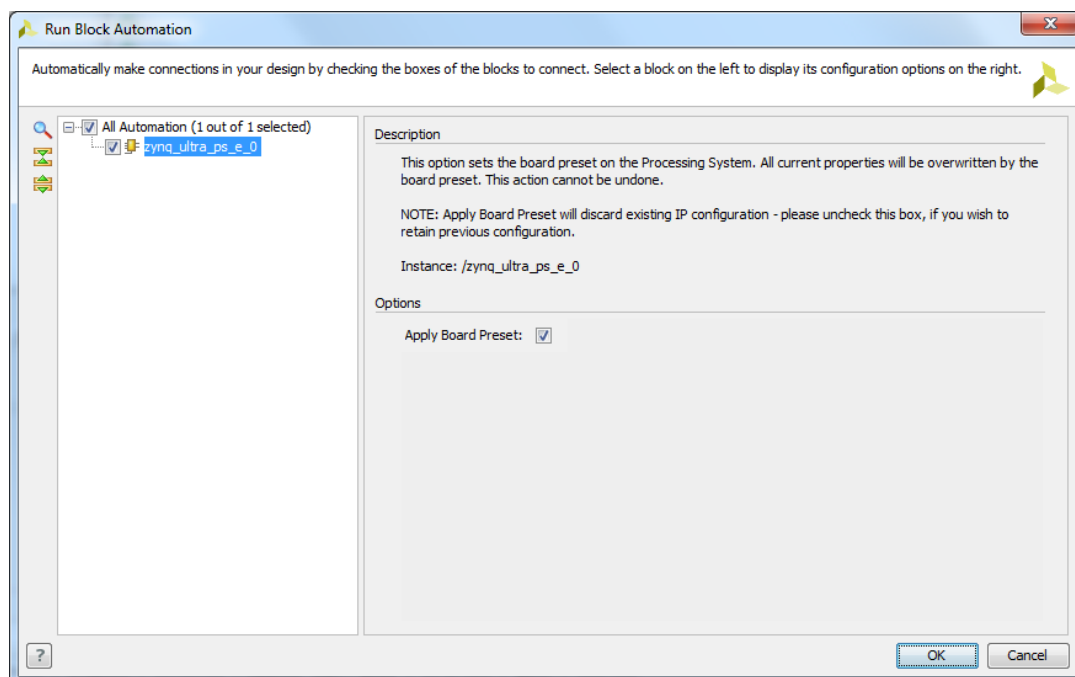
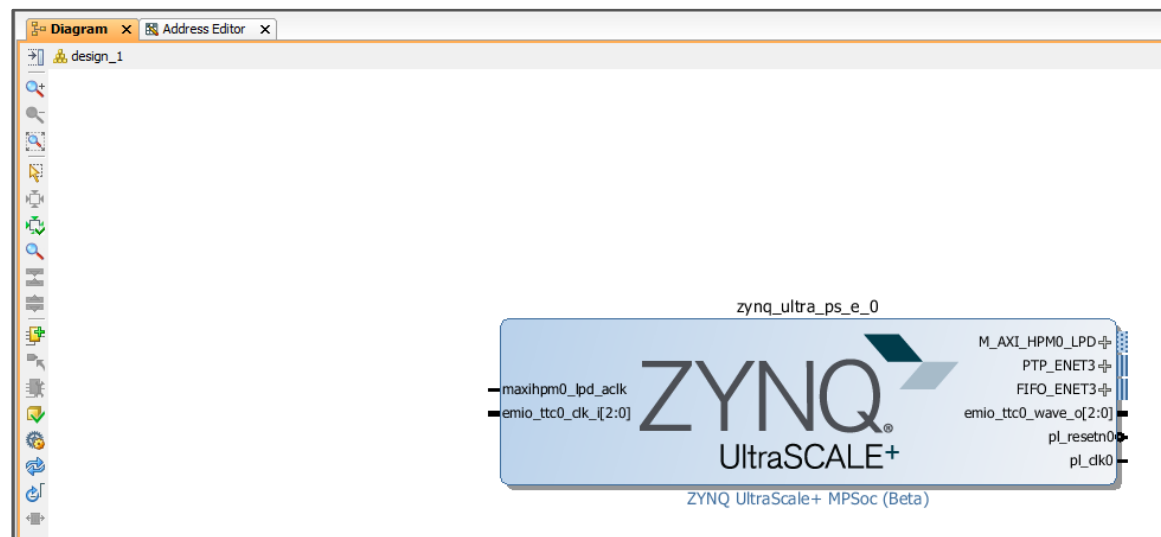The Zynq IP will be added to the design as shown in the following figure.

- The Zynq device has not yet been configured for the **Avnet UltraZed-EG IO Carrier Card**. Click on the **Run Block Automation** to configure the Zynq device with the IO Carrier Card board settings.

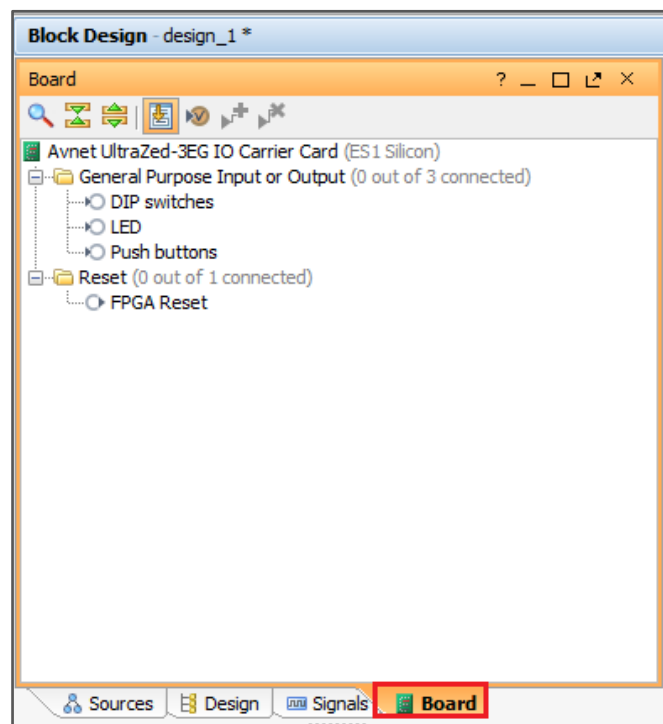- When the following dialog box appears, click **OK** to continue.

- The Zynq device will be configured as shown in the following figure. The Zynq device is now configured with the IO Carrier Card board level settings such as PS DDR4, PS peripheral selections, clocking, etc.
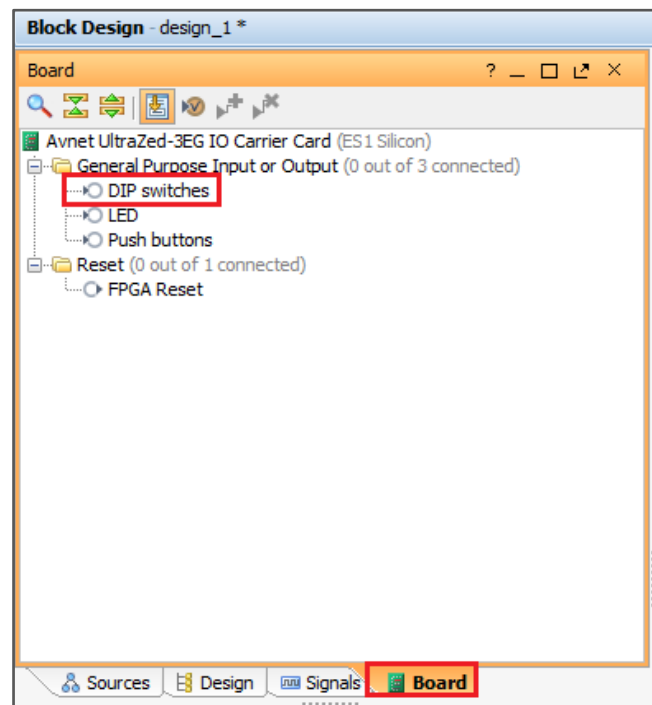

2.2 Adding Peripherals to the Block Design

You are now ready to add peripherals to the design that are connected to the Zynq UltraScale+ MPSoC PL on the IO Carrier Card such as PL LEDs, DIP switches, and Push switches.

- Under **Block Design** window in Vivado, click on the **Board** tab as shown in the following figure. You will see a set of peripherals that can be connected to the Zynq UltraScale+ MPSoC PL on the IO Carrier Card.
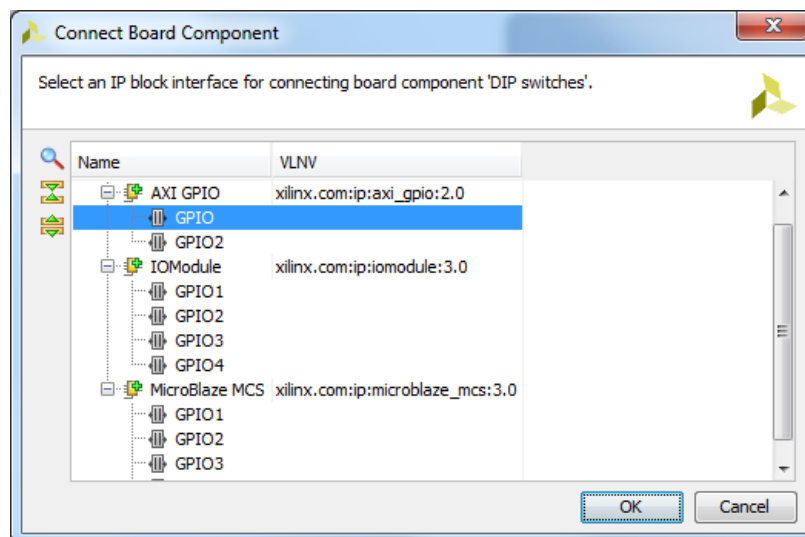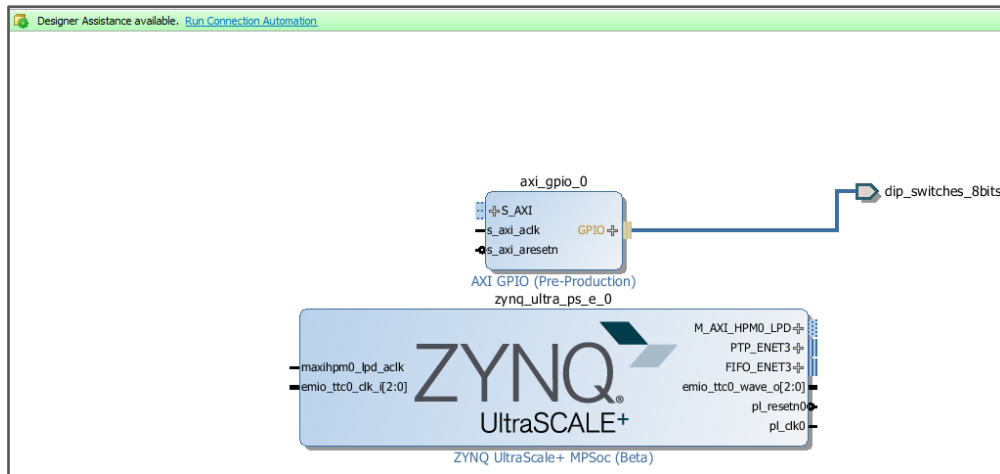
- Double click on the **DIP switches** as shown in the following figure to add the eternal PL 8-position DIP switches to the design. This will add a PL GPIO core to the design so that the DIP switches can be read via the Zynq UltraScale+ MPSoC PS.
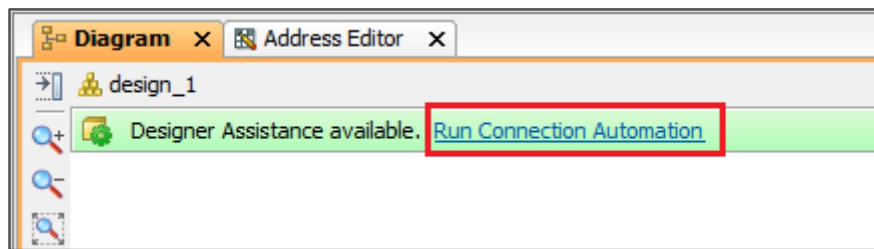

- When the following dialog box appears, make sure the **GPIO** is selected as shown and click **OK** to continue. The GPIO will be used by software to read the DIP switches.
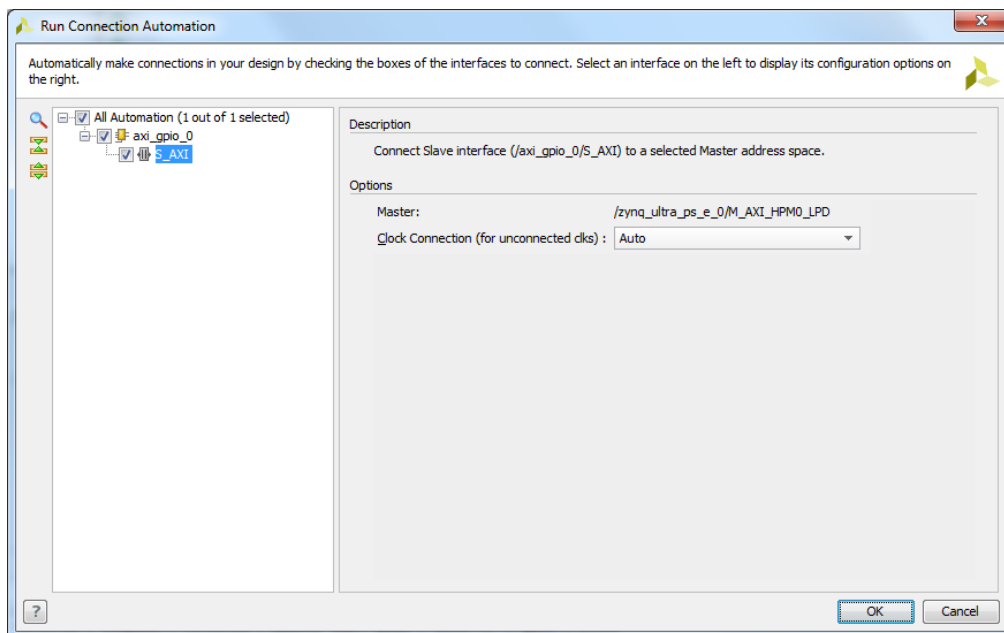
The **axi_gpio_0** IP will be added to the design and the block design will look as shown in the following figure.
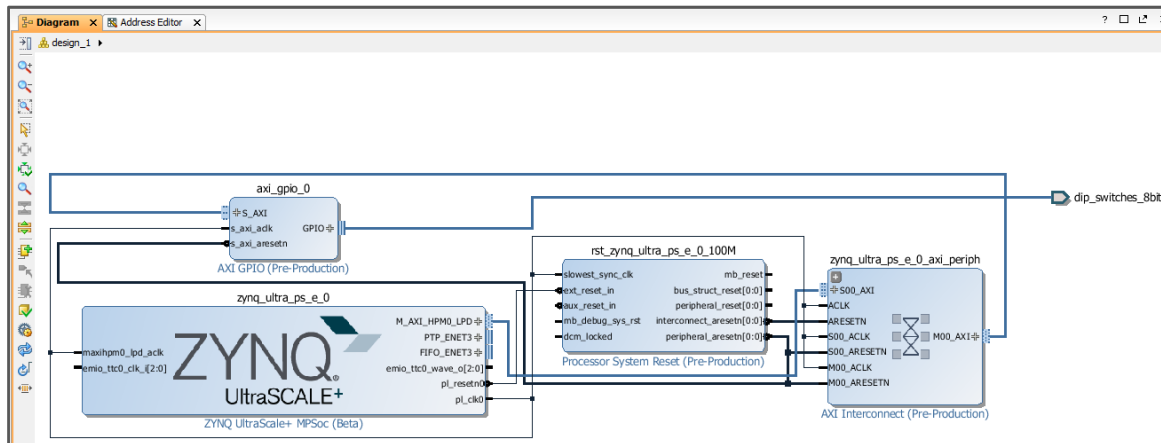

- Click on the **Run Connection Automation** to connect the **axi_gpio_0** IP to the Zynq UltraScale+ MPSoC PS as shown in the following figure.
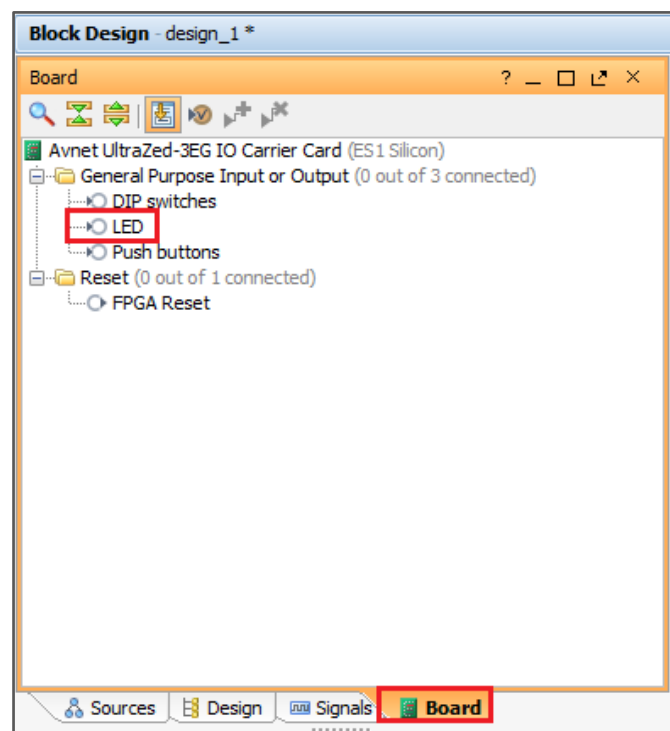

- When the following dialog box appears, click **OK** to continue.
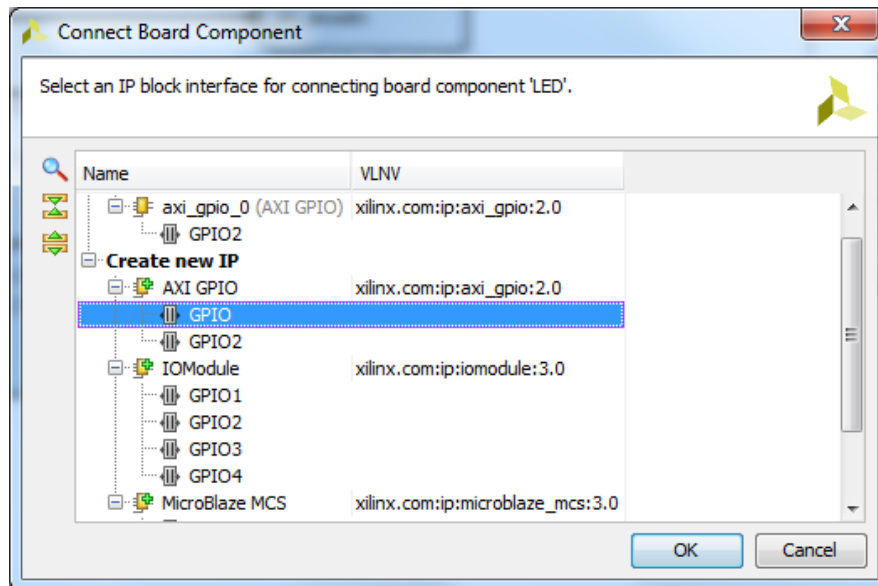
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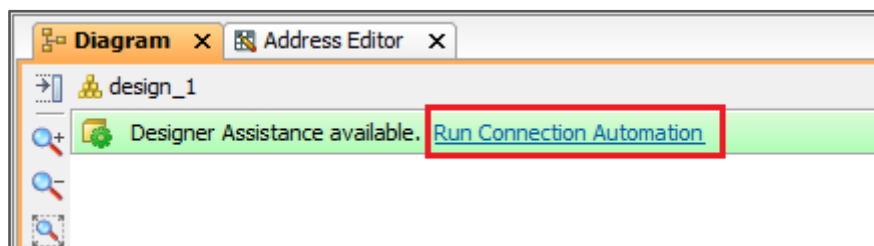The **axi_gpio_0** IP will be connected to the PS as shown in the following figure.

- Double click on the **LED** as shown in the following figure to add the eternal PL LEDs to the design. This will add a PL GPIO core to the design so that the LEDs can be written to via the Zynq UltraScale+ MPSoC PS.
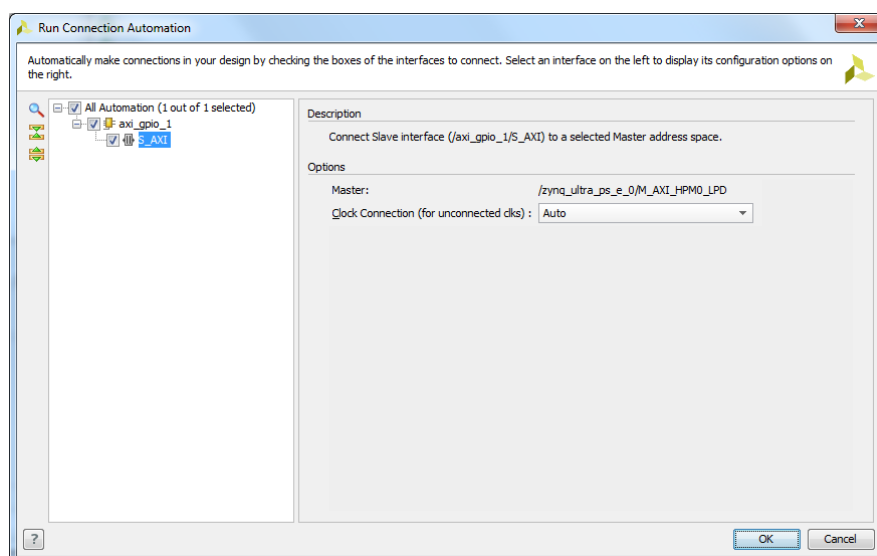
- When the following dialog box appears, select the **GPIO** under the **Create new IP** as shown and then click OK.

- Click on the **Run Connection Automation** to connect the **axi_gpio_1** IP (the new GPIO just added to the design) to the Zynq PS as shown in the following figure.

- When the following dialog box appears, click **OK** to continue.

- Double click on the **Push buttons** as shown in the following figure to add the eternal PL Push switches to the design. This will add a PL GPIO core to the design so that the Push switches can be read via the Zynq UltraScale+ MPSoC PS.

- When the following dialog box appears, select the **GPIO** under the **Create new IP** as shown and then click OK.
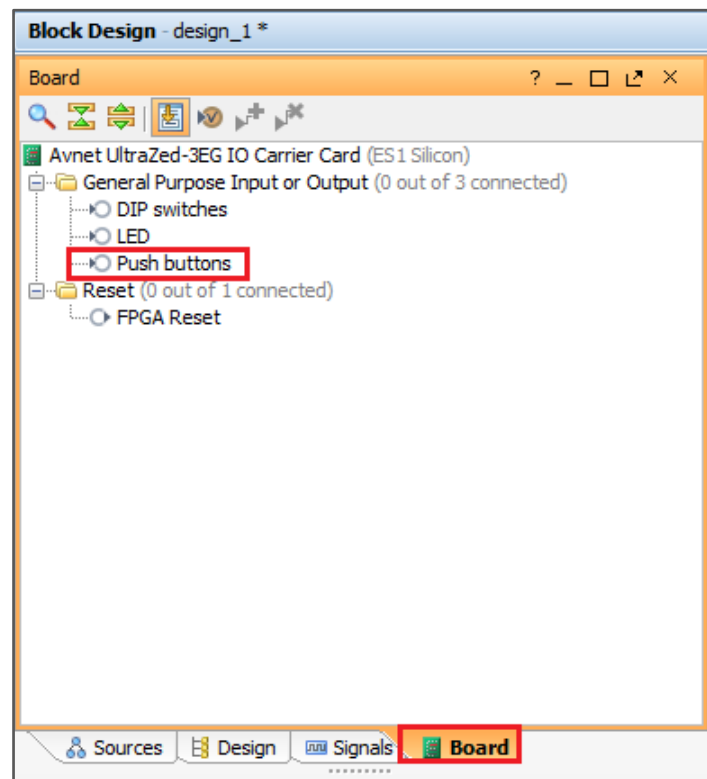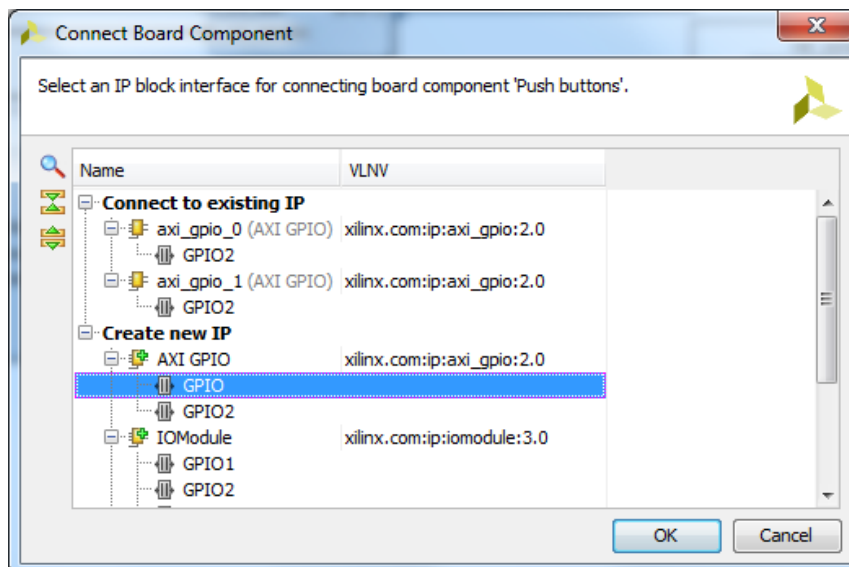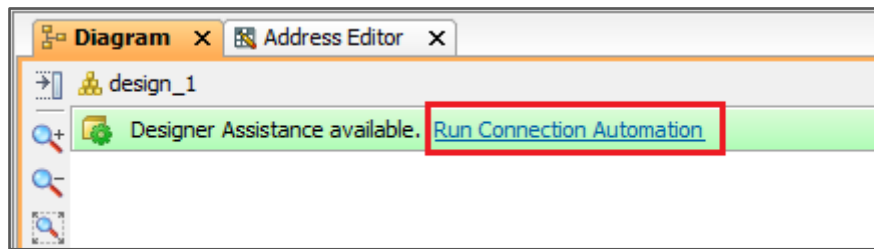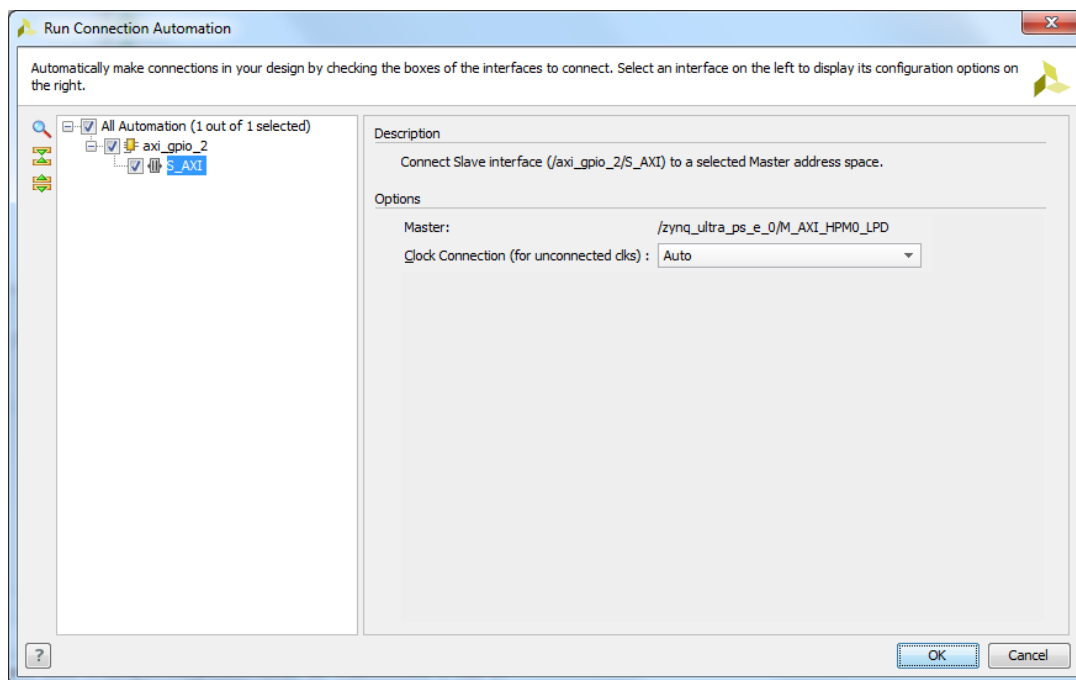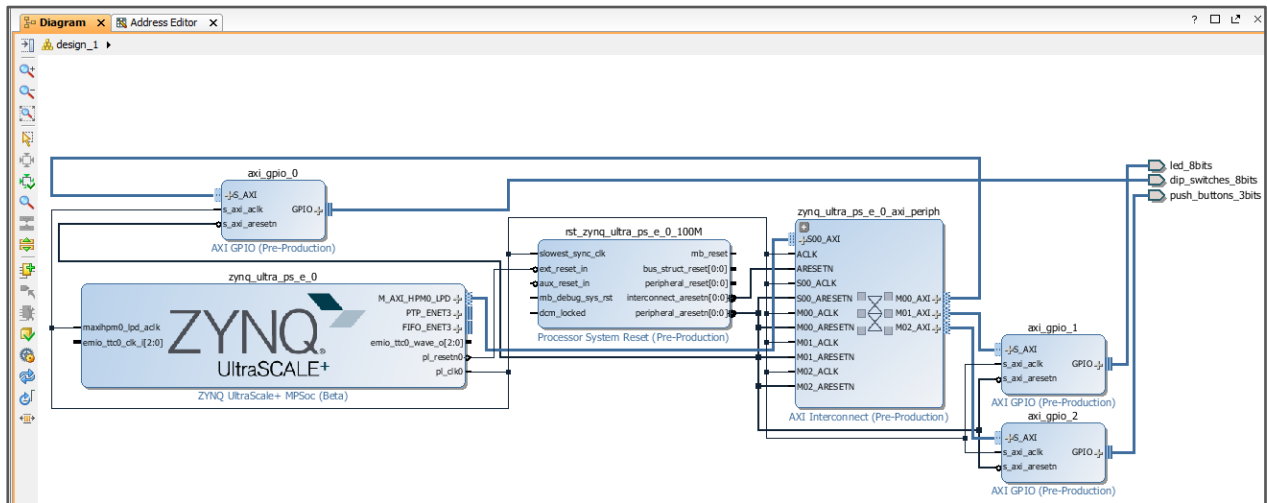
- Click on the **Run Connection Automation** to connect the **axi_gpio_2** IP (the new GPIO just added to the design) to the Zynq UltraScale+ MPSoC PS as shown in the following figure.
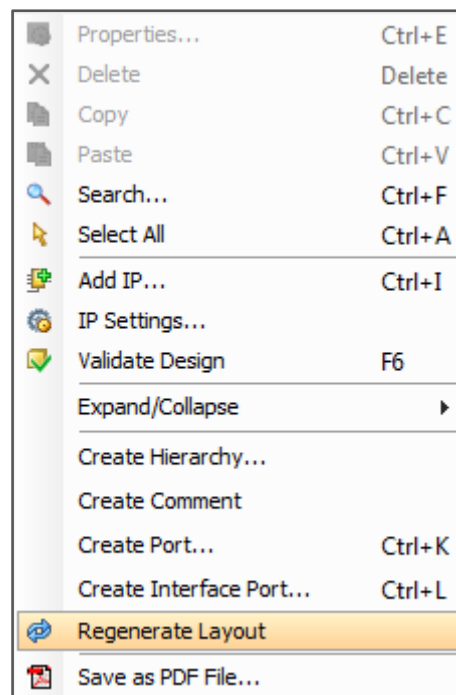

- When the following dialog box appears, click **OK** to continue.

The block design will look as shown in the following figure.

- Right-click in the white space of the block design diagram and select **Regenerate Layout** as shown in the following figure.
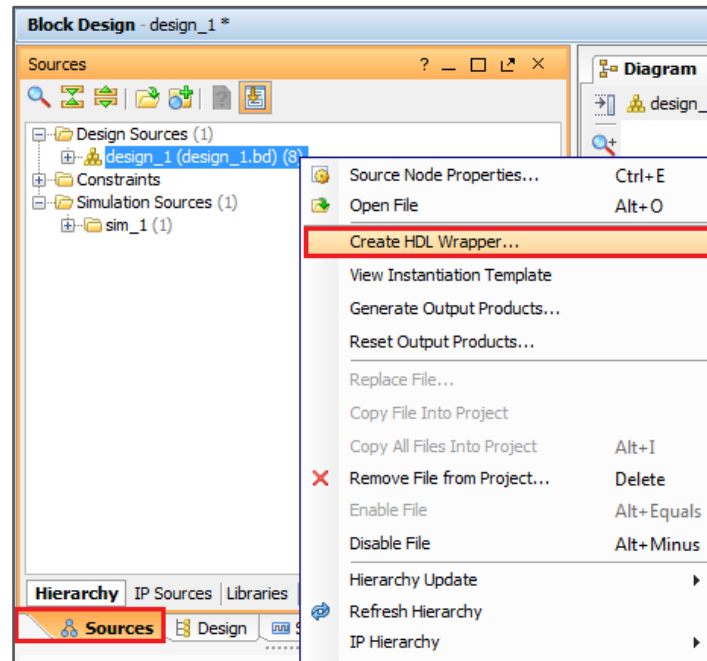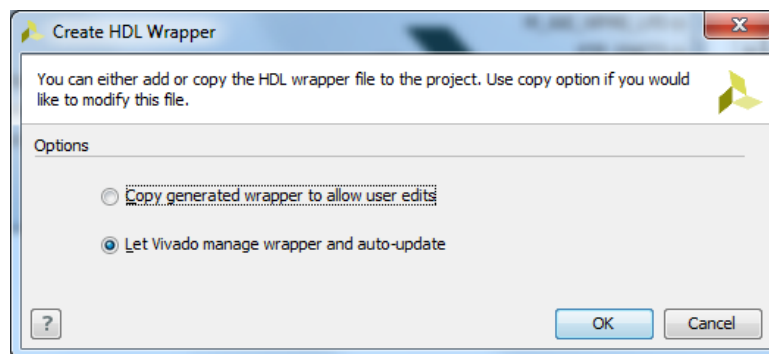
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This will clean up the block design drawing and places all PL peripheral interfaces to the right of the block design as shown in the following figure.

2.3 Validating the Block Design

- Select **Tools > Validate Design** from the Vivado toolbar as shown in the following figure. This will validate the design to make sure all block design connections are valid.

- When the following dialog box appears, click **OK** to continue.
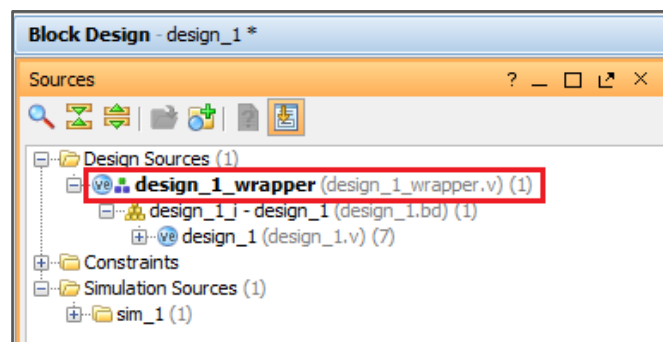
2.4 Creating HDL Wrapper File for the Design

- Click on the **Sources** tab as shown in the following figure. Then right-click on the **design_1 (design_1.bd)** and select **Create HDL Wrapper**. This will create a top-level HDL wrapper file for the design.
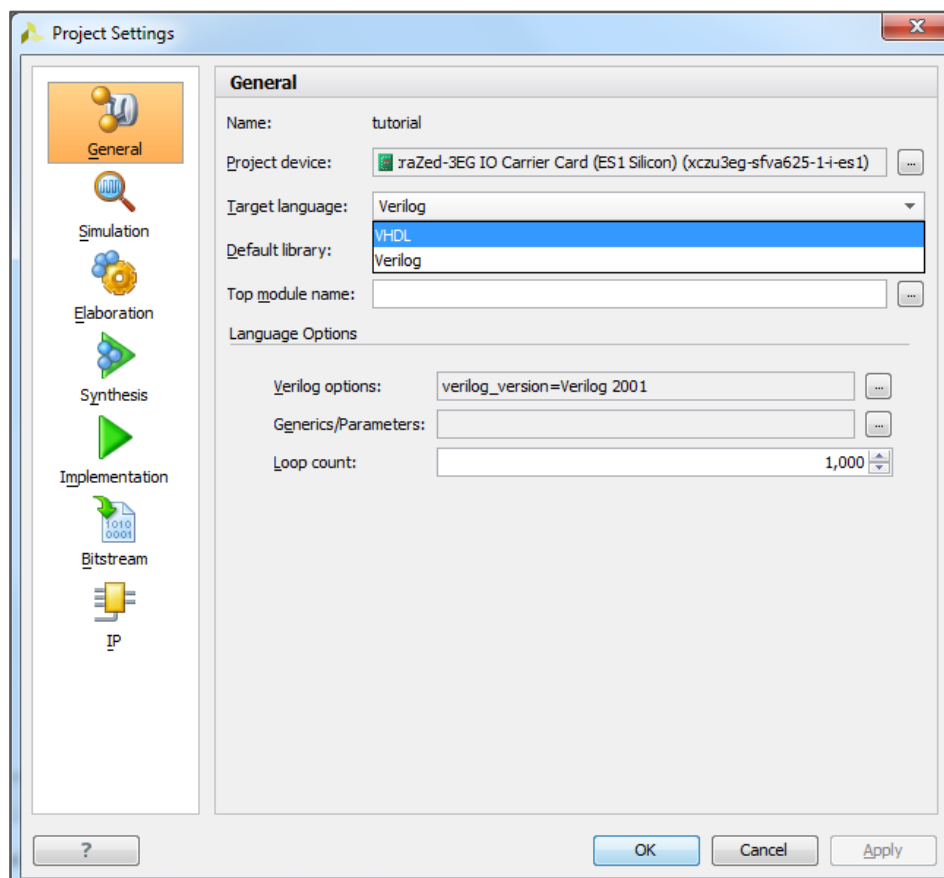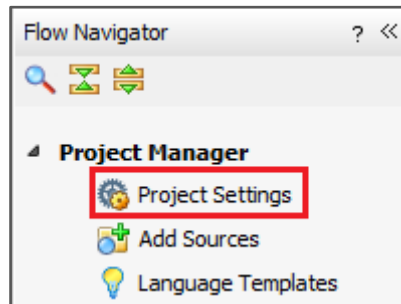

- When the following dialog box appears, click **OK** to continue.

- The top-level Verilog wrapper file will be generated as shown in the following figure.
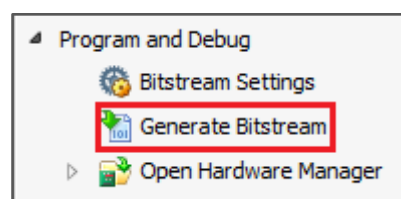
- If you need VHDL wrapper file, set the **Target language** to **VHDL** in the Project Settings as shown below before generating the HDL wrapper file. Click on **Project Settings** in Vivado GUI first and then set the **Target language** in the **Project Settings** dialog box.
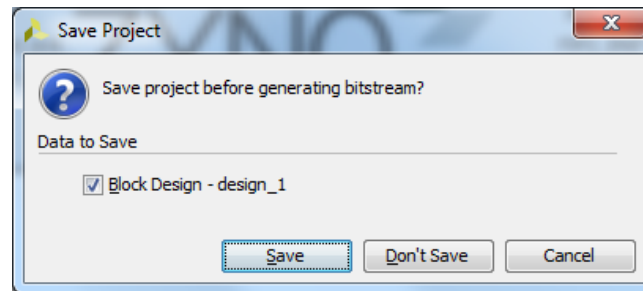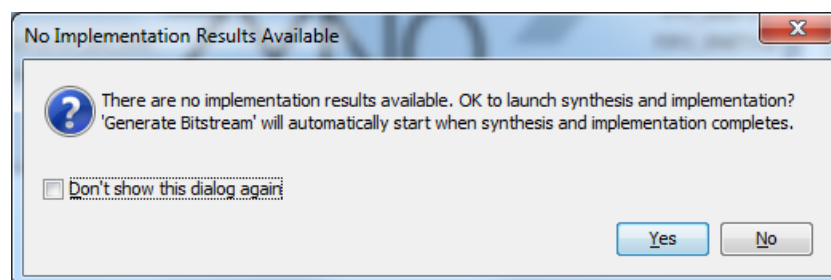
2.5 Generating a Bit File

The generation of the hardware platform using the UltraZed-EG IO Carrier Card Board Definition Files is now completed. You can now build the design and generate a bit file. Click on **Generate Bitstream** in Vivado GUI to generate a bit file for the hardware platform.
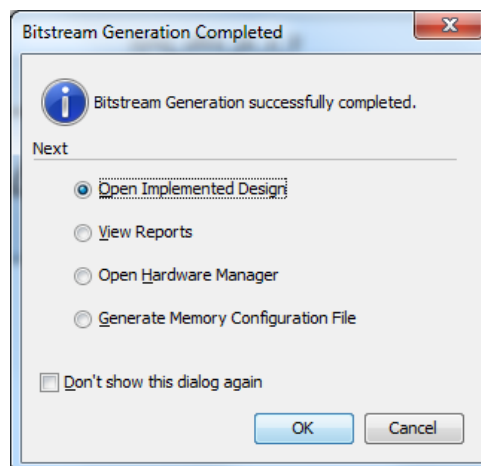
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- When the following dialog box appears, click **Save** to continue.

- When the following dialog box appears, click **Yes** to continue.

- When the following dialog box appears, click **OK** to continue. This will open the implemented design in the Vivado GUI and you should see the device diagram. The implemented design needs to be open prior to exporting the hardware platform to SDK.

The generation of the hardware platform using the UltraZed-EG IO Carrier Card Board Definition Files is now completed. You can now export the hardware platform to the SDK and begin running test software and applications on the hardware platform. Please refer to the UltraZed-EG website www.ultrazed.org/product/ultrazed-EG for a complete tutorial for the UltraZed-EG SOM and Carrier Card.