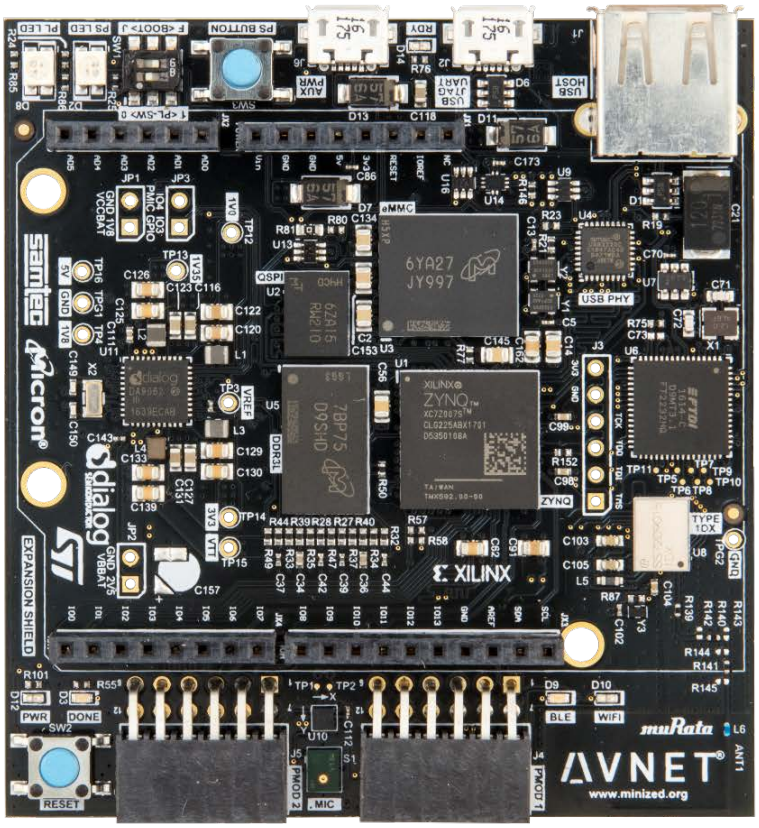
/MINIZED™

AVNET®
Reach Further™



MiniZed Hardware User Guide

Version 2.0

LIT# MiniZed-HW-UG-v1-0-V2

Document Control

Document Version: 2.0

Document Date: 01 May 2020

Prior Version History

Version	Date	Comment
1.0	02 Jun 2017	Initial MiniZed Hardware User Guide
2.0	01 May 2020	Added warning regarding FT2232 JTAG circuit

Contents

Figures

Tables

Reference Documents

[1] Zynq-7000 All Programmable SoC Overview

[2] Zynq-7000 All Programmable SoC DC and AC Switching Characteristics

[3] Zynq-7000 All Programmable SoC Technical Reference Manual

[4] 7 Series FPGAs SelectIO Resources User Guide

[5] Zynq-7000 All Programmable SoC Packaging and Pinout Product Specification

[6] Zynq-7000 All Programmable SoC PCB Design Guide

[7] Xilinx Vivado Design Suite

[8] Xilinx Software Development Kit

[9] Digilent Pmod Interface Specification

[10] Arduino Uno Technical Specs

[11] FT2232H Dual High Speed USB to Multipurpose UART/FIFO IC Datasheet

[12] Murata LBEE5KL1DX Type 1DX 2.4GHz WiFi + Bluetooth Module

[13] Cypress BCM4343W datasheet

[14] Dialog DA9062 Integrated Power Solution Datasheet

[15] USB3320 Hi-Speed USB 2.0 ULPI Transceiver

[16] Micron DDR3L SDRAM MT41K256M16TW datasheet

[17] Micron QSPI Serial NOR Flash Memory datasheet

[18] Micron 8GB eMMC datasheet

[19] 7-inch Zed Touch Display Kit

[20] MP34DT01 MEMS audio sensor omnidirectional digital microphone datasheet

[21] LIS2DS12 3-axis "pico" accelerometer with temperature sensor datasheet

Terminology

Term	Definition
ARM	Advanced RISC Machine
BGA	Ball Grid Array
BLE	Bluetooth Low Energy
BSP	Board Support Package
I/O	Input/Output
I2C	Inter-Integrated Circuit
ECC	Error Correction Code
EDR	Enhance Data Rate
EMIO	Extended MIO
eMMC	Embedded Multi-Media Controller/Card
FSBL	First Stage Boot Loader
GPIO	General Purpose I/O
HR	High Range
JTAG	Joint Test Action Group
LE	Low Energy
LPO	Low Power Oscillator
MEMs	Micro-Electro-Mechanical Systems
MIO	Multiplexed I/O
N/C	Not Connected
OCM	On-Chip Memory
POR	Power On Reset
PDM	Pulse Density Modulation
PL	Programmable Logic
PMIC	Power Management Integrated Circuit

Pmod	Peripheral module (Digilent Inc. trademark)
PS	Processor System
RISC	Reduced instruction set computing
RTC	Real-Time Clock
SDIO	Secure Digital Input Output
SoC	System on a Chip
SPI	Serial Peripheral Interface
SRST	System Reset
SSBL	Second Stage Boot Loader
UART	Universal Asynchronous Receiver/Transmitter
ULPI	USB Low Pin Interface
USB	Universal Serial Bus

1 Introduction

The main purposes of the MiniZed Kit are the following:

- Be a low-cost starter kit for Zynq SoC developers
- Showcase the Zynq 7000S single-core family
- Incorporate the Murata 1DX Bluetooth and Wireless solution
- Demonstrate Bluetooth for peripherals or phone/tablet user interfaces
- Use an on-board microphone as input for PL-PS signal processing reference designs
- Allow for the use of Arduino-compatible, Pmod™-compatible and USB peripherals
- Showcase hardware acceleration for software bottlenecks

2 Block Diagram and Features

This section summarizes the features of the development board, followed by functional descriptions.

2.1 List of Features

The MiniZed Developer Kit supports the following features:

- Zynq single-core System-on-Chip (SoC) device : XC7Z007S-1CLG225C
- Storage
  - Micron 512 MB DDR3L
  - Micron 128 Mb Quad SPI NOR flash
  - Micron 8GB eMMC
- Micro USB connector for on-board JTAG and UART via FTDI device
- Micro USB connector for external power in high power mode
- USB Type A host connector for a USB slave device connection
- Arduino Shield connectors for Arduino-compatible peripherals
- Pmod sockets x 2
- Murata wireless “Type 1DX” module: LBEE5KL1DX
  - based on the Cypress BCM4343W
  - 2.4 GHz Wi-Fi complies with 802.11b/g/n
  - Bluetooth
    - Bluetooth Version 4.1 plus EDR (Enhanced Data Rate)
    - Power Class 1 (10dBm max) and BLE (Bluetooth Low Energy)
  - Leverages certification of reference design that uses PCB antenna
- Dialog PMIC (power-management IC) with I2C interface : DA9062
- Bi-element user LEDs x 2
- Single-color LEDs for Power, Config Done, Wifi, and Bluetooth
- Reset pushbutton & user PS pushbutton x 1
- User PL switch x 1
- ST Micro Accelerometer and Temperature sensor : LIS2DS12
- ST Micro MEMS microphone sensor : MP34DT05

Note that there is no on-board, wired Ethernet interface. All development will have to be done via USB, Wi-Fi, or JTAG interface. Wired Ethernet may be possible using a Pmod.

2.2 MiniZed Block Diagram

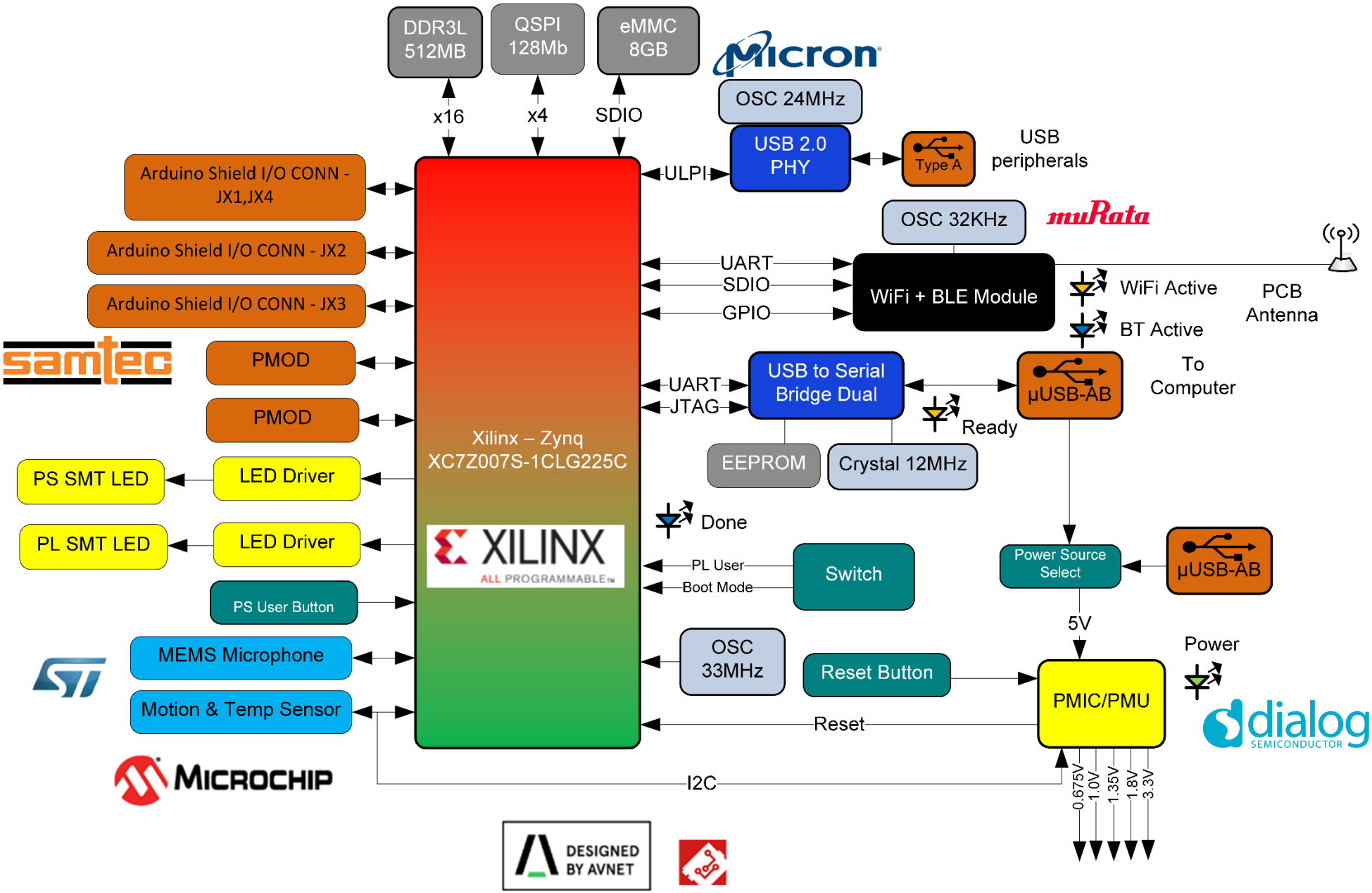


Figure 1 – MiniZed Block Diagram

3 Functional Description

The following sections provide brief descriptions of each feature provided on the MiniZed board.

3.1 Zynq 7Z007S SoC

The Zynq 007S device (in the CLG-225 package) contains:

- Processor System (PS):
  - Single-core ARM® Cortex™-A9
  - Max frequency 667MHz
  - 256 KB on-chip RAM
  - 84 PS I/O pins
  - USB 2.0 OTG, SDIO x 2, UART x 2, SPI x 2, I2C x 2 etc.
- Logic Elements (LE):
  - Programmable logic architecture equivalent to an Artix -7 FPGA
  - 23K Logic Cells
  - 1.8Mb Block RAM (50 x 36Kb blocks)
  - 54 High Range (1.2V to 3.3V) I/O pins
- The 225-pin package is used since this is the lowest cost device in this family
- This package restricts the DDR interface to 16 bits
- Only one USB master interface is supported
- Only 1 of the 2 SDIO controllers in the PS are available directly from the PS, the other through EMIO. The CLG225 does not support booting from SD Card.
- One PS UART is routed to the computer via USB, the other is used for communication with the Bluetooth part of the Murata wireless module. For communication with Shield or Pmod peripherals, one of these UARTs can be re-purposed or another UART can be instantiated in the PL.
- I/O levels of 3.3V are supported for PMOD and Arduino peripherals.
- All MIO pins are 3.3V.

3.1.1 SoC IC Package

The CLG225 package is a 225-pin 13mm x 13mm BGA with a 0.8mm ball pitch. The image below indicates the locations of the various I/O pins as seen from the top.

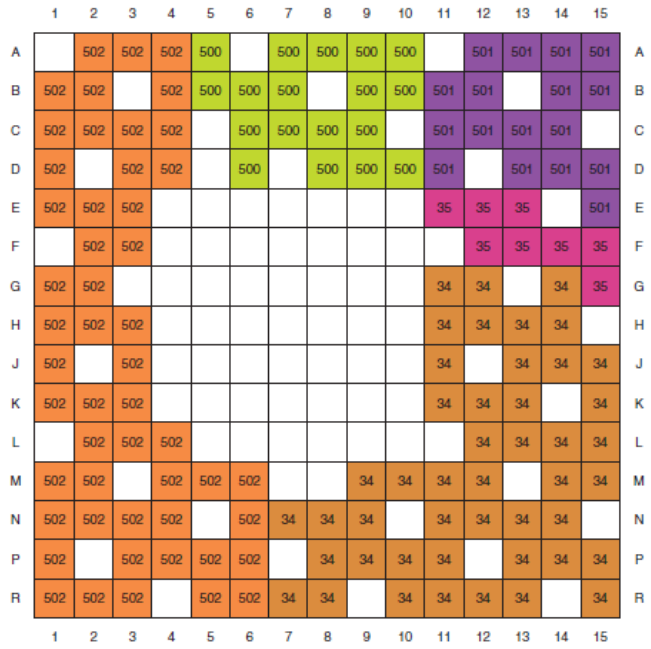


Figure 2 – I/O Bank Pin Locations (Top view)

3.1.2 Device configuration

Device configuration, i.e. the programming of both the PS and the PL, can be achieved in a number of ways:

- Using JTAG via the on-board USB-to-JTAG circuitry to configure the SoC using the Xilinx SDK, which is based on Eclipse (see [8])
- Loading an image from the QSPI flash device
- Loading the First Stage Boot Loader (FSBL), Second Stage Boot Loader (SSBL) and PL bitstream from QSPI flash so that the Petalinux components can be loaded from either the on-board eMMC or from an external mass storage device such as a Micro SD (uSD) card plugged into a Pmod socket using SDIO

3.1.3 Debug interface

Historically the use of a JTAG debugger involved a JTAG connector and the use of an additional JTAG pod/cable. The MiniZed board has on-board JTAG circuitry that allows JTAG programming and debug using a standard USB cable.

The JTAG circuitry used on the Avnet MiniZed is a Xilinx solution based on the FTDI FT2232. As stated in https://www.xilinx.com/support/answers/68889.html, "the proprietary solution is not documented or supported, and cannot be provided to customers as a reference."

Please do NOT use the FT_PROG tool in conjunction with the MiniZed. The only way to fix it after erasing it is to send it back to the factory, which is more expensive than just buying a new MiniZed.

- The USB-to-JTAG interface uses a 2-port USB-to serial converter from FTDI, the FT2232.
- To use the FT2232 device, the computer must have the FTDI driver installed, as well as Vivado 2017.1 or later. (see [7])
- The first FT2232 port is used for USB-to-JTAG, while the second is used for USB-to-UART. The USB-to-UART enumerates as a COM port on the computer when the EEPROM is correctly programmed.
- If looking to add an on-board USB-to-JTAG configuration solution to a custom board, please consider adding a JTAG-SMT module to your board, like this:
  http://avnet.me/jtagsmt3
  http://avnet.me/jtagsmt3-bulk

3.1.4 I/O Levels

The MiniZed's Zynq SoC allows programmable voltage levels for PS I/O pins (1.8V or 3.3V) and for PL I/O pins (1.2V to 3.3V).

- PS I/O pin assignments are typically the result of trade-offs between functions, as they are multiplexed onto the same bonded out I/O pins, known as MIO pins.
- The MIO pins are divided into two banks, i.e. Bank 0 = MIO0-15 and Bank 1 = MIO16-53. In Vivado the I/O voltage levels for both these banks are set to 3.3V (and not 1.8V).
- Peripherals such as SDIO, UART, I2C and SPI can be selected to interface directly to the PL, in which case they are mapped to EMIO (Extended MIO) pins. These pins can be used in the PL and/or can be routed to PL I/O pins
- All the MiniZed's PL I/O pins are HR (high range, i.e. 1.2V to 3.3V). All PL banks are set to the 3.3V range.
- The 54 PL pins are defined to be 27 differential signal pairs. When the bank I/O supply is 3.3V, as for most MiniZed PL banks, LVDS is supported as input only.

3.1.5 Power Banks

There are various I/O banks that can be powered separately. The table below shows how those I/O banks are powered on the MiniZed board.

Table 1 – MiniZed Zynq Bank I/O voltages

SoC Side	Purpose	Bank	Voltage
PS	Configuration	0	3.3V
	MIO0 - MIO15, PS_CLK, PS_POR	500	3.3V
	MIO16 – MIO53, PS_SRST	501	3.3V
	DDR3L	502	1.35V
PL	HR I/O (46 pins)	34	3.3V
	XADC, HR I/O (8 pins)	35	3.3V

Table 2 – MiniZed Zynq Core and AUX voltages

SoC Side	Purpose	Voltage
PS	PS Core (VCCPINT)	1.0V
	VCCPAUX	1.8V
PL	PL Core (VCCINT, VCCBRAM)	1.0V
	VCCAUX	1.8V

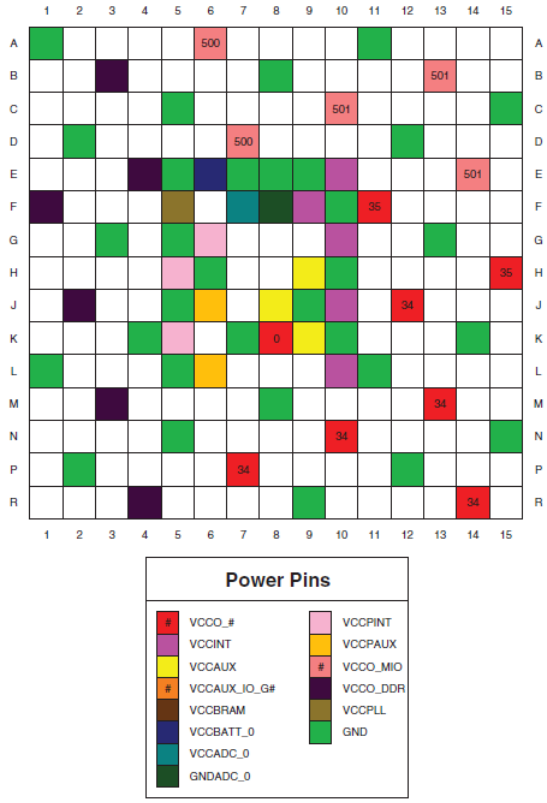


Figure 3 – Top View of 7Z007S Power Pins

3.2 Storage

The Zynq PS has 256 KBytes of on-chip RAM. The MiniZed supports 3 types of external memory:

- 512 MBytes of DDR3L, which is RAM for data and program storage
- 128 Mbits of QSPI NOR Flash
- 8 Gbytes of eMMC or SD Card via external PMOD (not included in kit)

3.2.1 Micron DDR3L memory

The MiniZed has a 4Gb (512 MB) DDR3L Micron MT41K256M16TW-107 memory device

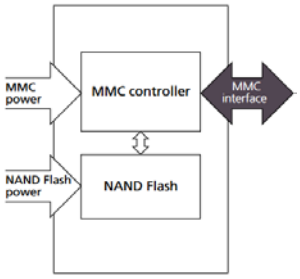
- The CLG225 package Zynq deice only supports a 16-bit wide memory interface (not x32).
- This is a 1.35V device in a 96-ball 8mm x 14mm package
- DDR termination voltage and reference are provided by the Dialog DA9062 PMIC
  - DDR termination voltage of 0.675 V is provided

3.2.2 Micron QSPI flash memory

The QSPI interface is a 3.3V NOR Micron MT25QL128ABA8E12-1SIT flash device.

The MiniZed's 128Mbit QSPI device can be expected to be large enough to run almost any bare metal application. It is also possible to run Petalinux from the QSPI dependent on how large of a build it is. However in most Petalinux builds the QSPI will be used to store the First Stage Boot Loader.

3.2.3 Micron on-board eMMC memory



Embedded Multi-Media Controller/Card (eMMC) is a mechanism to allow the ARM controller access to large banks of NAND flash without the requirement to actively manage the NAND.

The MiniZed board has an 8GB eMMC Micron MTFC8GAKAJCN-4M IT device.

- MiniZed is designed to operate the eMMC SDIO interface in high-speed mode, up to 50 MHz.
- The 3.3V device allows for a 4-bit interface, which means that 4 of the 8 data lines can be used for a 6-wire SDIO interface to the Zynq device.
- Block management is implemented on the device. The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.
- Zynq cannot boot directly from eMMC. The FSBL has to be in the QSPI flash device to boot from eMMC.

3.2.4 External SD card

Note that the 7Z007S in the CLG225 package cannot use an SD card for **primary** boot since that requires that the SD Card reside on the SDIO peripheral on MIO pins 40-45, and these pins are not available in the CLG225 package. This means that primary boot must be from QSPI flash or from JTAG.

- A (micro) SD card can be used if it is accessed via a Pmod slot.
- This will require the SDIO interface to be moved programmatically from hard-wired MIO pins to EMIO pins. Two GPIO pins for CD and WP will also have to be used. This is illustrated in the diagram below.
- Using EMIO will reduce the SDIO bus max clock speed from 50MHz (MIO) to 25MHz (EMIO).

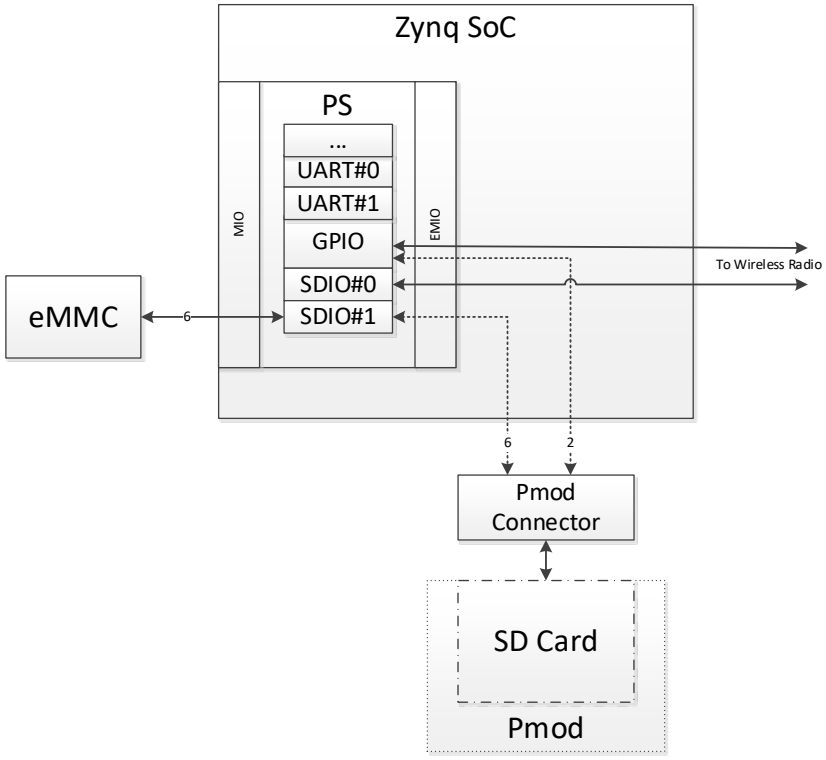


Figure 4 – How a Pmod Micro SD Card Could be Used

An example of such an SD card Pmod is the Avnet AES-PMOD-SD, which takes a full-sized SD card and can be found at https://www.avnet.com/shop/emea/p/kits-and-tools/development-kits/avnet-engineering-services-ade--1/aes-pmod-sd-3074457345629643403/ .

3.3 Power Supply

3.3.1 Power requirements

The MiniZed requires support for the input and output voltages and currents shown in Table 3.

Table 3 – Board power requirements

Bank	Voltage	Current (A)
Vccint / Vccpint	1 V	1.5
Vccaux / Vccpaux	1.8V	0.5
Vcco (DDR)	1.35V	1
Vcco 3.3	3.3V	1
DDR V_{TT}	0.68V	0.5
DDR V_{REF}	0.68V	0.1
Vin	5V	2.4

All supplies require 5% tolerance. These current values reflect the worst case power consumption of both the Zynq device (taken from Xilinx Power Estimator tool) as well as the other on-board circuitry.

3.3.2 Optional external power supply

A single USB 2.0 port is only required to provide 500mA. The power budget for the board shows that this power level is easily exceeded when the Zynq device operates under heavy utilization.

- A secondary micro USB power input is provided.
- When the MiniZed user wants to use more current, he/she will have to provide power from a secondary micro USB input.
- In the case of having a large input source, user can populate R114 which will link the two power inputs thus requiring only the single input source.
- A “power kit” that consists of a 5V supply and a USB cable can be sold as an add-on item when ordering a MiniZed board.
- The two micro USB inputs are connected directly, with each supply being protected by a blocking diode as in the image below.

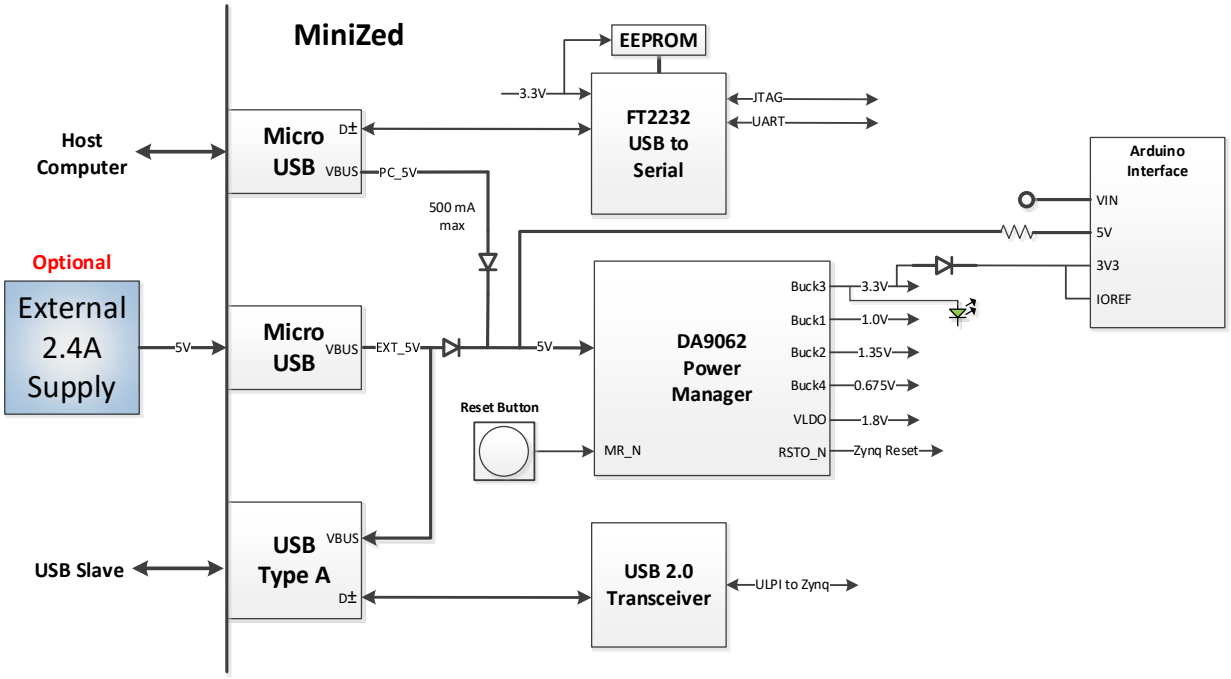


Figure 5 – Power Source Selection and Diode

- Also shown above is the powering of an Arduino-compatible shield.
  - A shield can be powered from the MiniZed through 5V and 3.3V. Both supply voltages have a small diode drop that is proportional to the current drawn. If the shield draws 500 mA, there could be a 0.3V drop.
  - A blocking diode protects the MiniZed supply output in the case of the shield being powered independently.
  - In the case of it being powered independently, the shield 5V supply is not protected. The user can remove the resistor in the 5V path to disconnect the 5V source if this should be a problem.
  - The Arduino VIN pin can be used to power a board from the shield. This use case is not supported, but the signal will be taken to a hole in the PCB.

3.3.2.1 *Power-pack add-on kit*

This MONOPRICE AVTCB-10273 external input supply is rated for 2.4A at 5V, allowing sufficient power to feed:

- The MiniZed Board with the PS and PL both running at Maximum frequency and utilization
- All on-board peripherals, such as the Wi-Fi and Bluetooth active
- All slave devices such as a USB slave, Arduino shield and Pmod peripherals active

This Kit includes an AC/DC adapter (5V >= 2A) with a USB Type A connection along with a USB Type-A to microUSB cable.

https://www.monoprice.com/product?c_id=103&cp_id=10321&cs_id=1032101&p_id=14578&seq=1&format=2

Figure 6 – AC/DC Adapter

A blocking diode is used to protect this input from back-feeding from other potential power sources.

3.3.3 Power Tree

- The PS and PL subsystems are powered off the same supplies to minimize board size and cost. Sequencing requirements are as follows
  - 1V→ 1.8V → 1.35V/3.3V/0.68V For graphical representation see Figure 8
- The DA9062 provides 4 switching buck regulators and 4 LDO regulators capable of supplying the voltage and currents we need. It also includes a watchdog and reset controller.
- The DA9062 is a programmable device. When programmed with the MiniZed configuration, the programmed part number is DA9062-10AM1. You can purchase this Dialog Part from Avnet at https://www.avnet.com/shop/us/p/uncategorized/dialog-semiconductor/da9062-10am1-3074457345632042209/. The device also has an on-board RTC (Real-Time Clock). The RTC count can be read back via I2C. Spare GPIO's located at JP3 can also be driven or read via I2C. The RTC can be backed up via a Seiko Instrument XH311HG-IV07E supercap (not populated by default at C157) or from an external battery supply located at JP2.

3.3.4 Module Reset

The DA9062 features a reset controller built into the device. This function is be used for module reset. A reset button is fed into the GPIO2 pin of the power supply, which is programmed with an internal de-bounce function.

The diagram below shows the reset structure.

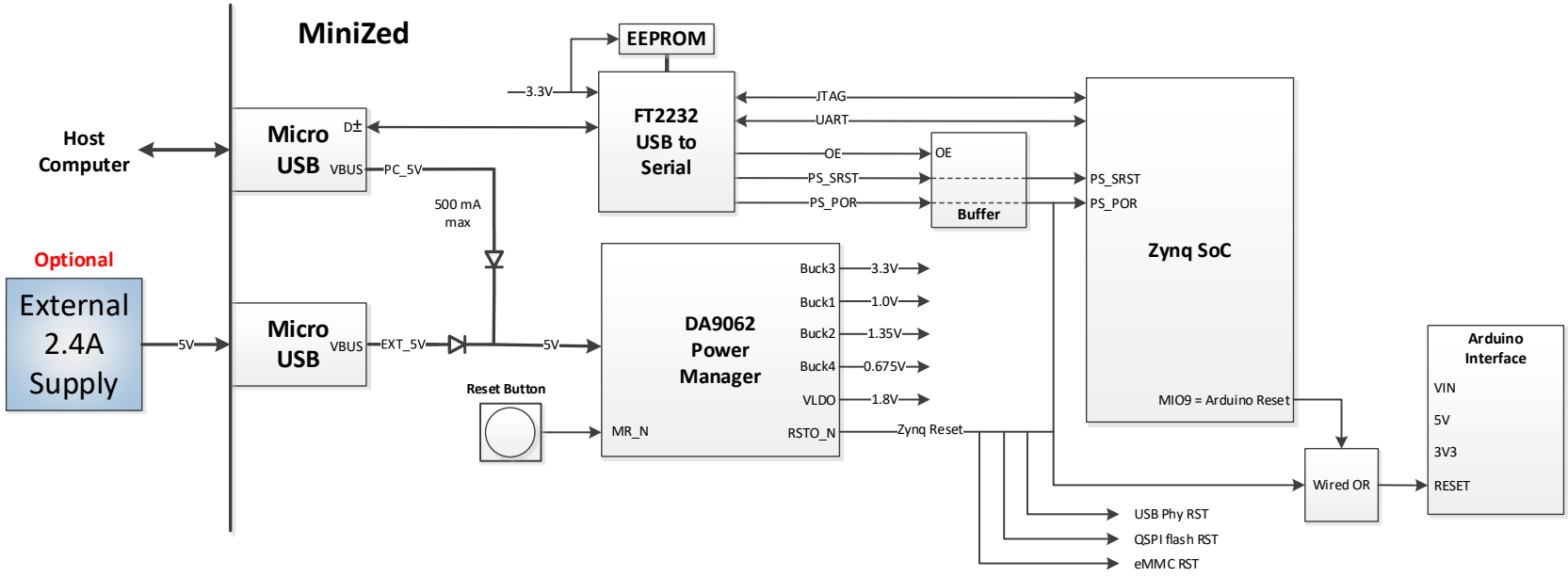


Figure 7 – MiniZed Reset Structure

The power-on and reset timing sequence is shown below.

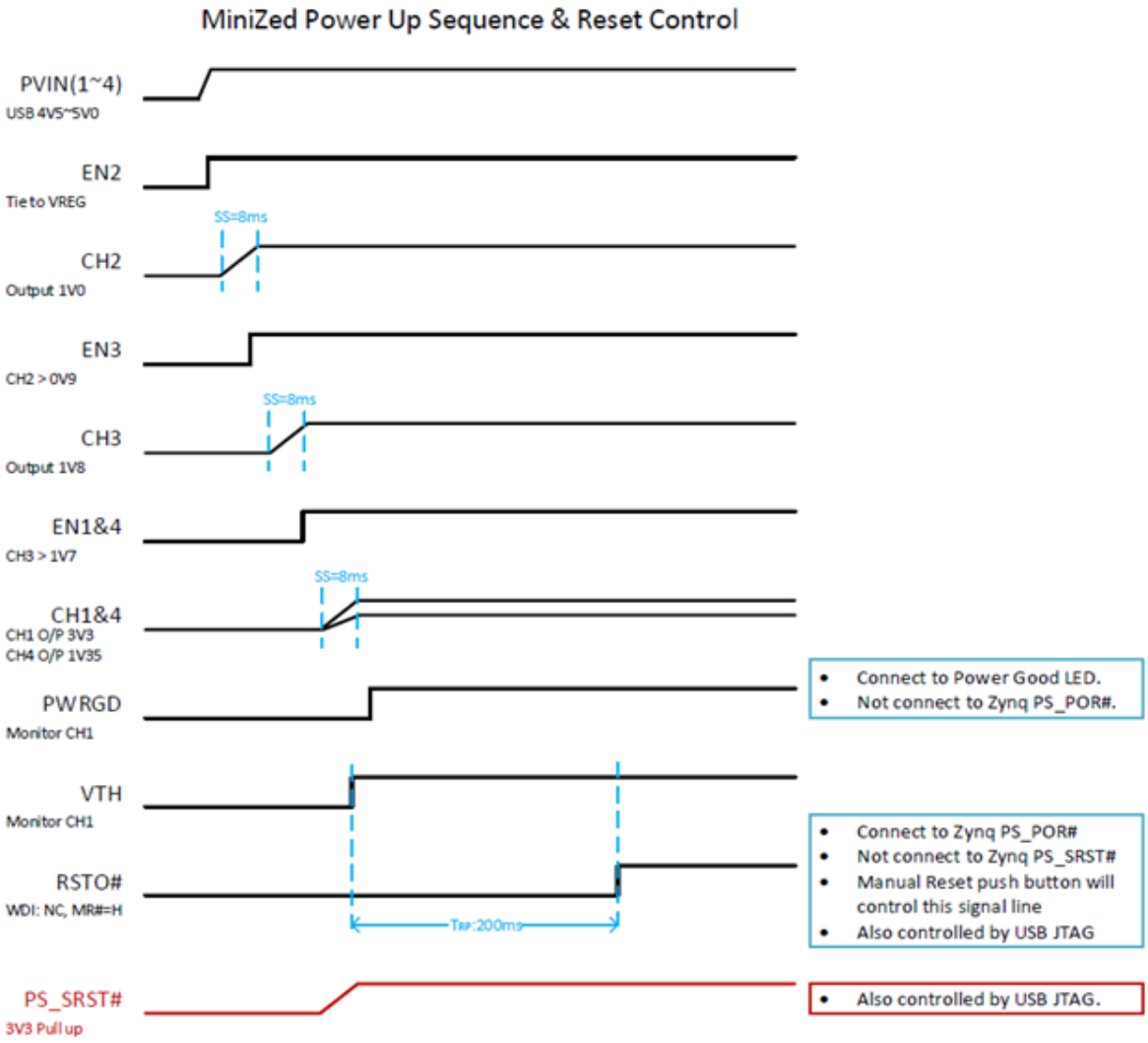


Figure 8 – Power-on and Reset Timing

3.4 Clocking

The following MiniZed board clock sources are provided

- Zynq PS clock - 33.33 MHz Microchip DSC1001DI1-033.3333T Oscillator
  - An internal PLL can be used to set the operating frequency, up to 667MHz
- USB OTG PHY - 24 MHz Microchip DSC1001DI1-024.0000T Oscillator
- USB-to-serial FTDI device - 12 MHz Abracon LLC ABM8G-12.000MHZ-B4Y-T Crystal
- Murata 1DX wireless module LPO (low power oscillator) - 32768 Hz Abracon LLC ABS07AIG-32.768KHZ-1-T Crystal

3.5 Wireless Radio Module

The Murata LBEE5KL1DX is a module that supports

- Wi-Fi 802.11b/g/n
- Bluetooth 4.1/EDR

3.5.1 Wireless Antenna

The Murata module does not have a built-in antenna. The MiniZed implements the Murata PCB design guidelines for a PCB antenna that is shaped by copper on layers in the PCB. By doing this, the Murata module certification is inherited.

3.5.2 Wireless software support

The 1DX module is based on the Cypress CYW4343W, which is a Cypress Semiconductor IEEE 802.11 b/g/n MAC/Baseband radio with Bluetooth 4.1. Standalone Zynq projects are not supported, only Linux using either the bcmdhd or brcmfmac Broadcom drivers as demonstrated in our reference designs are supported.

3.5.3 Wireless module layout

Layout of the wireless module was critical. The Murata layout guidelines were followed exactly. The Murata documents detailing the layout are confidential. If you would like to review them, then you must sign up at https://my.murata.com.

3.5.4 Zynq to wireless module interface

The diagram shows how the Zynq PS peripherals are connected to the 1DX module.

- All wireless I/O are connected via EMIO
- All 4 UART signals (Tx, Rx, CTS and RTS) are used for the Bluetooth/BLE interface
- All 6 SDIO signals are used for the Wi-Fi interface
- 4 of the 1DX GPIO signals are connected for handshaking
  BT_REG_ON
  BT_HOST_WAKE
  WL_REG_ON
  WL_HOST_WAKE
- The PCM interface is not connected. This is typically used for driving a Bluetooth speaker directly.

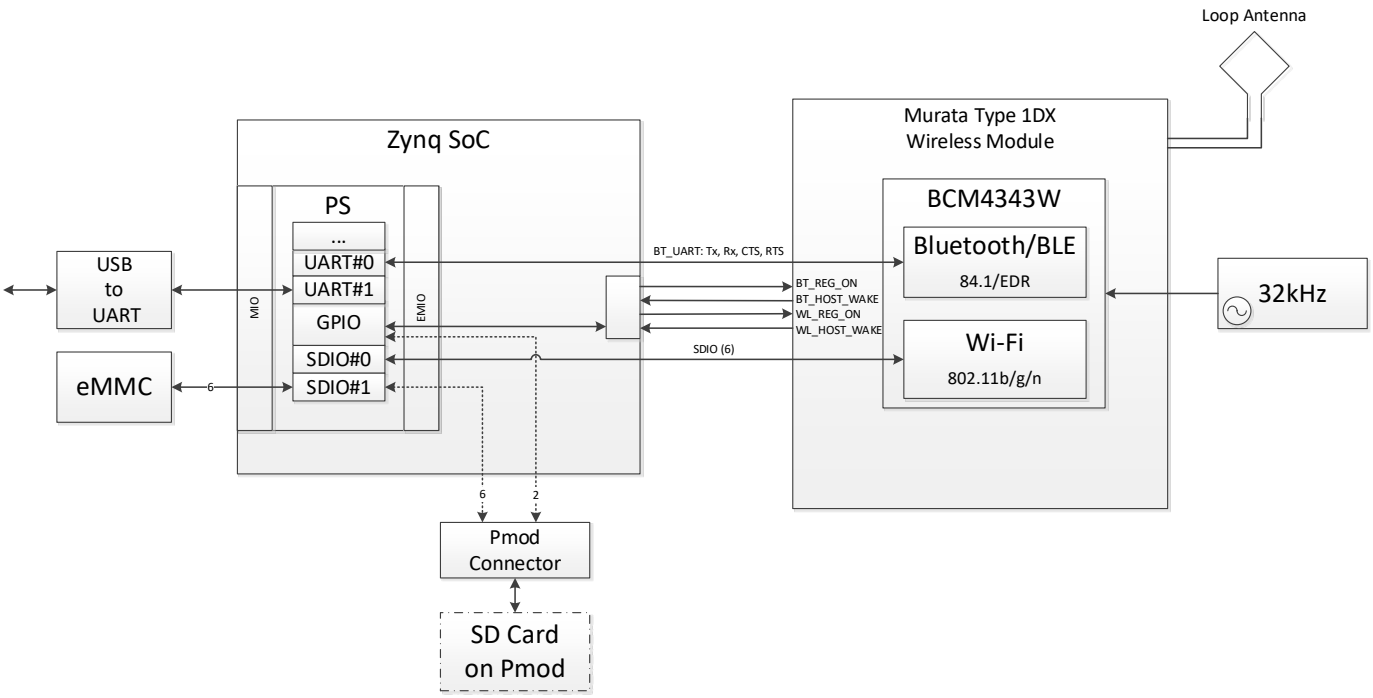


Figure 9 – Zynq Interface to the Wireless Module

3.6 USB Host Interface

This interface is the same as what has been used on previous Avnet boards. It allows USB slave devices such as a mouse, keyboard or USB camera to be connected to the PS. Typically Linux drivers will be used for these devices.

- On MiniZed OTG mode is not supported, **USB is Host mode only**.
- The Microchip USB3320C USB 2.0 transceiver uses the ULPI (USB low-pin interface) that the Zynq PS provides.
- The USB phy uses a 24MHz clock input.
- A USB Type A USB0 connector is provided for these USB slave peripherals.
- The I/O voltage, VDDIO, is set to 3.3V. The USB PHY interfaces with PS MIO bank #1 which is shared with the USB-JTAG/UART circuit and is set to 3.3V.

3.7 Arduino-compatible Shield connectors

Arduino Revision 3 (R3) is currently the latest revision of the Arduino shield interface standard. See [10].

3.7.1 Shield power and signal levels

As shown in Figure 10, there is a 5V power pin that can be used to supply power to a shield. There is a resistor that can be removed to disable this 5V input. This is done for the cases in which the shield is powered independently.

- Only 3.3V shields are supported because the Zynq I/O's are not 5V tolerant.
- The analog A0 to A5 pins are not supported.
- To power a shield from MiniZed, the MiniZed board must be powered from an external power supply. In this case a 500mA budget is supported. The power supply must be designed such that a shield itself can also be powered from an independent source without causing harm to the MiniZed itself.

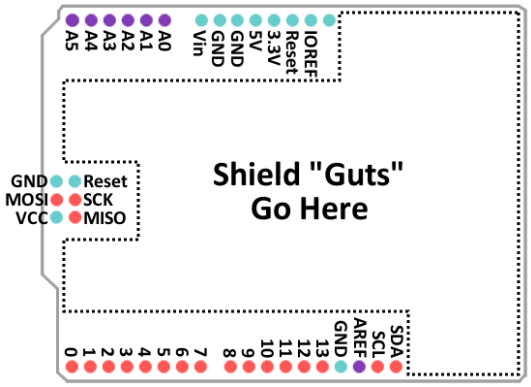


Figure 10 – Arduino R3 Pins

3.7.2 Shield connector layout

Figure 11 shows the spacing of the Arduino connectors.

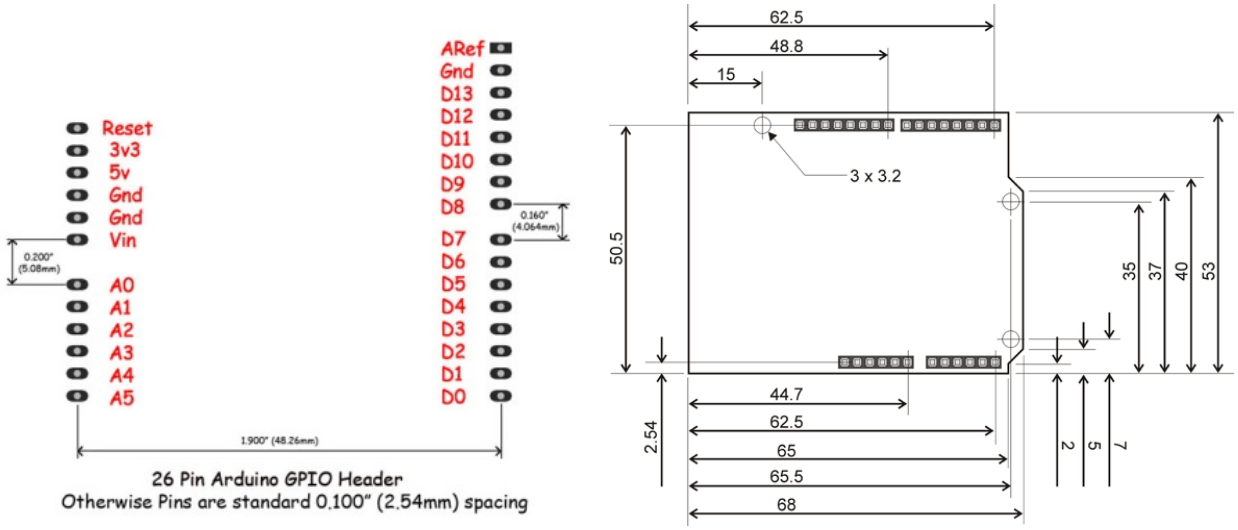


Figure 11 – Arduino (not R3) Measurements

A variety of use cases for Arduino boards exist. Figure 12 shows a number of common interfaces.

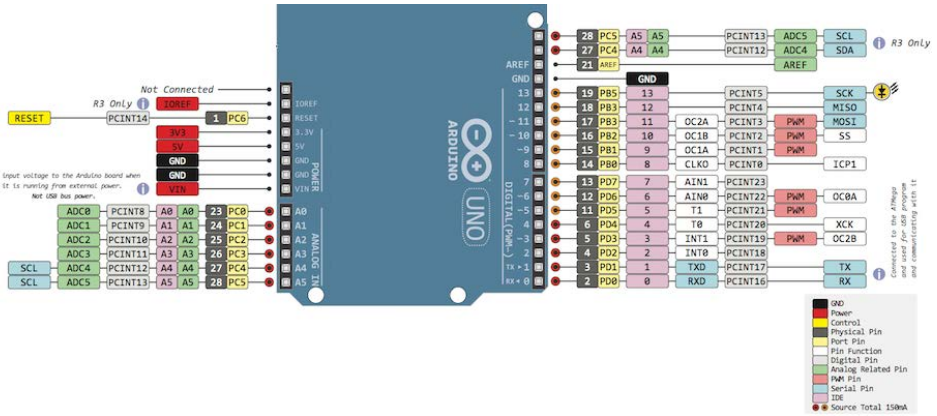


Figure 12 – Reference Arduino R3 Footprint (Arduino UNO Board)

3.7.3 Arduino interface connector pin assignments

In Figure 10 the 2x3 pin header in the middle on the left is the Arduino's ICSP (in-circuit As the ARD_D0 to ARD_D13 signals all originate in the SoC's FPGA fabric, these allocations are flexible and can be re-assigned through firmware for each use case. The tables below show the PCB signal assignments for the 4 Arduino connectors shown in Figure 12.

Table 4 – Pinout for the ARJ1 Arduino Header Socket Strip

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
ARJ1	1	VIN	N/C	N/C
	2	GND	GND	N/C
	3	GND	GND	N/C
	4	5V	5V0 AS	N/C
	5	3V3	3V3 AS	N/C
	6	RESET	ARDUINO_RST	N/C
	7	IOREF	IOREF	N/C
	8	NC	N/C	N/C

Table 5 – Pinout for the ARJ2 Arduino Header Socket Strip

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
ARJ2	1	AD5	ARDUINO_A5	E11
	2	AD4	ARDUINO_A4	E12
	3	AD3	ARDUINO_A3	E13
	4	AD2	ARDUINO_A2	F12
	5	AD1	ARDUINO_A1	F13
	6	AD0	ARDUINO_A0	F14

Table 6 – Pinout for the ARJ3 Arduino Header Socket Strip

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
ARJ3	1	IO8	ARDUINO_IO8	M9
	2	IO9	ARDUINO_IO9	N9
	3	IO10	ARDUINO_IO10	M10
	4	IO11	ARDUINO_IO11	M11
	5	IO12	ARDUINO_IO12	R11
	6	IO13	ARDUINO_IO13	P11
	7	GND	GND	N/C
	8	AREF	AREF	N/C
	9	SDA	ARDUINO_SDA	F15
	10	SCL	ARDUINO_SCL	G15

Table 7 – Pinout for the ARJ4 Arduino Header Socket Strip

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
ARJ4	1	IO0	ARDUINO_IO0	R8
	2	IO1	ARDUINO_IO1	P8
	3	IO2	ARDUINO_IO2	P9
	4	IO3	ARDUINO_IO3	R7
	5	IO4	ARDUINO_IO4	N7
	6	IO5	ARDUINO_IO5	R10
	7	IO6	ARDUINO_IO6	P10
	8	IO7	ARDUINO_IO7	N8

3.8 Pmod connectors

Two 12-pin Pmod connectors are provided. The distance between the centers of the two Pmod connectors is 900 millimeters apart. This is so that modules with two Pmod connectors can also be used. For general details on Pmod-compatible interfaces, refer to [9].

In order for the Avnet Touch Display (see [19]) to be used, the Pmod signals were routed differentially on MiniZed. You must assign the I/Os as TMDS33 differential pairs.

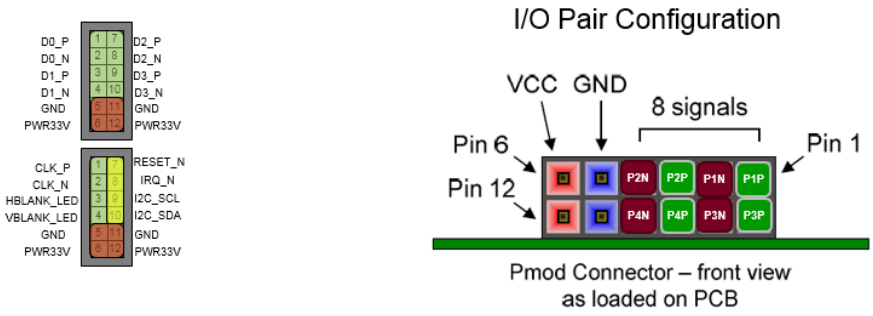


Figure 13 – Avnet Touch Display Pmod Pin Assignments

As the Zynq I/O's are not 5V compatible, only 3.3V Pmod (PMOD_LP) devices are supported.

Use cases show that the most common Pmod interfaces use UART, SPI, or I2C configurations, as shown in the following tables. Allocations for PMOD signals from EMIO pins originate in the Zynq's FPGA fabric, these allocations are flexible and can be re-assigned for some use cases.

Table 8 – PMOD#1-LP 2x6 Connector Pinout

Pin	Signal	UART	I2C	SPI
1	PMOD1_D0_P	CTS	SCL	SS
2	PMOD1_D0_N	TXD	SDA	MOSI
3	PMOD1_D1_P	RXD	SCL	MISO
4	PMOD1_D1_N	RTS	SDA	SCK
5	GND			
6	VCC=3.3V			
7	PMOD1_D2_P	INT	INT	INT
8	PMOD1_D2_N	GPIO	GPIO	RESET
9	PMOD1_D3_P	SCL	SCL	N/A
10	PMOD1_D3_N	SDA	SDA	N/A
11	GND			
12	VCC=3.3V			

Table 9 – PMOD#2-LP 2x6 Connector Pinout

Pin	Signal	UART	I2C	SPI
1	PMOD2_D0_P	CTS	SCL	SS
2	PMOD2_D0_N	TXD	SDA	MOSI
3	PMOD2_D1_P	RXD	SCL	MISO
4	PMOD2_D1_N	RTS	SDA	SCK
5	GND			
6	VCC=3.3V			
7	PMOD2_D2_P	INT	INT	INT
8	PMOD2_D2_N	GPIO	GPIO	RESET
9	PMOD2_D3_P	SCL	SCL	N/A
10	PMOD2_D3_N	SDA	SDA	N/A
11	GND			
12	VCC=3.3V			

3.9 Pull-up resistors

For I2C (as for other open-drain signals) a pull-up is required for the SCL and SDA lines. Those lines can be re-purposed for other uses. Alternatively, weak internal pull-ups in the Zynq I/O cell can be activated.

- For MiniZed the assumption will be that most external peripherals that have I2C will have pull-ups on the peripheral itself and that if they are not there, weak SoC pull-ups should be enough.
- For the Arduino I2C interface, two 4.75k pull-ups are provided but will not be populated by default. Their REFDES are NTR7 and NTR8.
- For Pmod interfaces, no pull-ups will be provided.

3.10 Sensors

The MiniZed allows for the use of a variety of external peripherals via the USB, Arduino and Pmod interfaces. It also has some on board sensors.

3.10.1 Microphone Input

A MEMS (Micro-Electro-Mechanical Systems) microphone is included on the board. This microphone has a simple digital output which allow for audio signals to be processed in the PL.

The MP34DT05 from ST Micro is a 4mm x 3mm omni-directional digital microphone.

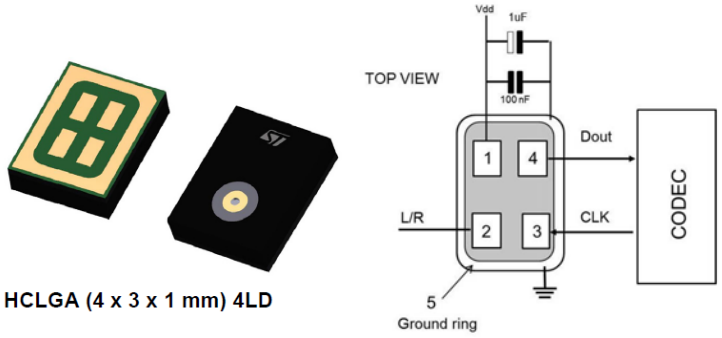


Figure 14 – Microphone Input

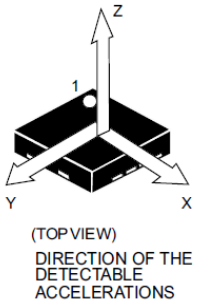
- The MP34DT05 is a low distortion digital microphone with a 64dB signal-to-noise ratio and –26 dBFS ± 3dB sensitivity
- It operates on 1.8V. Level translators are implemented to interface to the 3.3V Zynq interface.
- The input clock pin is nominally 2.4 MHz, but it is currently using 2.5MHz to drive it as a divisor of 160MHz
- Alternate clock cycles are used to clock data for left and right channels. The output is in PDM (pulse-density modulation). This format can be used to drive CODEC's directly, but in MinIZed's case, it is processed inside the FPGA. PDM can be de-modulated by passing it through a Low Pass Filter.

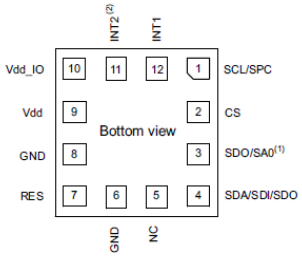
Table 10 – Audio Sensor Pinout

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
S1	1	Vdd		N/C
	2	LR		N/C
	3	VLK	AUDIO_CLK	L12
	4	DOUT	AUDIO_DO	M12
	5	GND	GND	N/C

3.10.2 Motion & Temperature sensor

The LIS2DS12 from ST Micro is a MEMS 3-axis accelerometer with an embedded temperature sensor.





- 1.8V supply
- 16-bit data
- Selectable full scale 2g/4g/8g/16*g*
- 256-level FIFO
- The I2C interface is used and will be shared with the Arduino I2C interface
- Since this is a 1.8V device, level translators to/from 3.3V logic levels is used
- Temperature is relative, not absolute

Table 11 – Motion & Temperature Sensor Pinout

Connector	Pin	Connector Pin Name	PCB Signal	Zynq Pinout
U10	1	SCL/SPC	SCL_L	N/C
	2	CS		N/C
	3	SDO/SA0/MDSA		N/C
	4	SDA/SDI/SDO	SDA_L	N/C
	5	NC	N/C	N/C
	6	GND	GND	N/C
	7	GND	GND	N/C
	8	GND	GND	N/C
	9	VDD	1V8	N/C
	10	VDD_IO	1V8	N/C
	11	INT2/MSCL	TP2	N/C
	12	INT1	TP1	N/C

3.11 User interface

LED's and buttons allow for feedback and control.

3.11.1 Board LED's

A few single-color LED's give user indication of the board status:

- A green LED indicates board power.
- A blue LED indicates that the SoC programming is Done.
- Another blue LED indicates that Bluetooth is active.
- A yellow/amber LED indicates that Wi-Fi is active.

3.11.2 SoC LED's

Two bi-filament LED's are be connected to the Zynq device.

- Each led uses two lines and it can therefore be in 4 states: off, red, green or amber.
- One LED connects to the PS and the other to the PL. This will allow for GPIO from both sides.
- The PL LED is shared with two Arduino pins (A3 and A4). So that these signals do not affect signal integrity, they are isolated by FETs.

3.11.3 Push buttons

- A pushbutton switch feeds into the power supply, where it is de-bounced and used to trigger a hard power-on reset.
- Another pushbutton switch is connect to the PS and can be used as a MIO input.

3.11.4 Switches

- A single surface mount 2 bit DIP switch (dual switch) is installed.
  - Bit one is used as a user input into the PL.
  - Bit two is used for JTAG/QSPI boot selection.

4 Zynq-7000 AP SoC I/O Bank Allocation

4.1 PS pin Allocations

There are 86 I/O pins that are directly connected to the PS.

- Multiplexed I/O (MIO) account for 32 of these 86 pins
- There are two banks of MIO pins (0-15 and 16-53)
  - Many MIOs in the 16-53 range are not available on CLG225 Package hence the reference to only 32 MIO pins below
- The I/O voltage levels for both MIO banks are set to 3.3V signals.

This is how functionality is assigned to PS pins:

Table 12 – PS I/O pin assignments

Function	Total I/O
MIO pins	32
DDR	51
PS Clock (PS_CLK)	1
PS Power-On Reset (PS_POR)	1
System Reset (PS_SRST)	1
Total:	86

Table 13 – Allocation of MIO pins

Function	MIO Pin Number(s)	Total I/O
QSPI	1-6	7
Feedback Clock	8	
SDIO #1 (eMMC)	10-15	6
USB #0	28-39	13
Phy Reset	7	
UART #1	48,49	2
Bi-filament LED	52,53	2
User pushbutton	0	1
Arduino Reset signal	9	1
Total:		32

The image below shows how the 32 available MIO pins are assigned in Vivado when configuring the Zynq processing system:

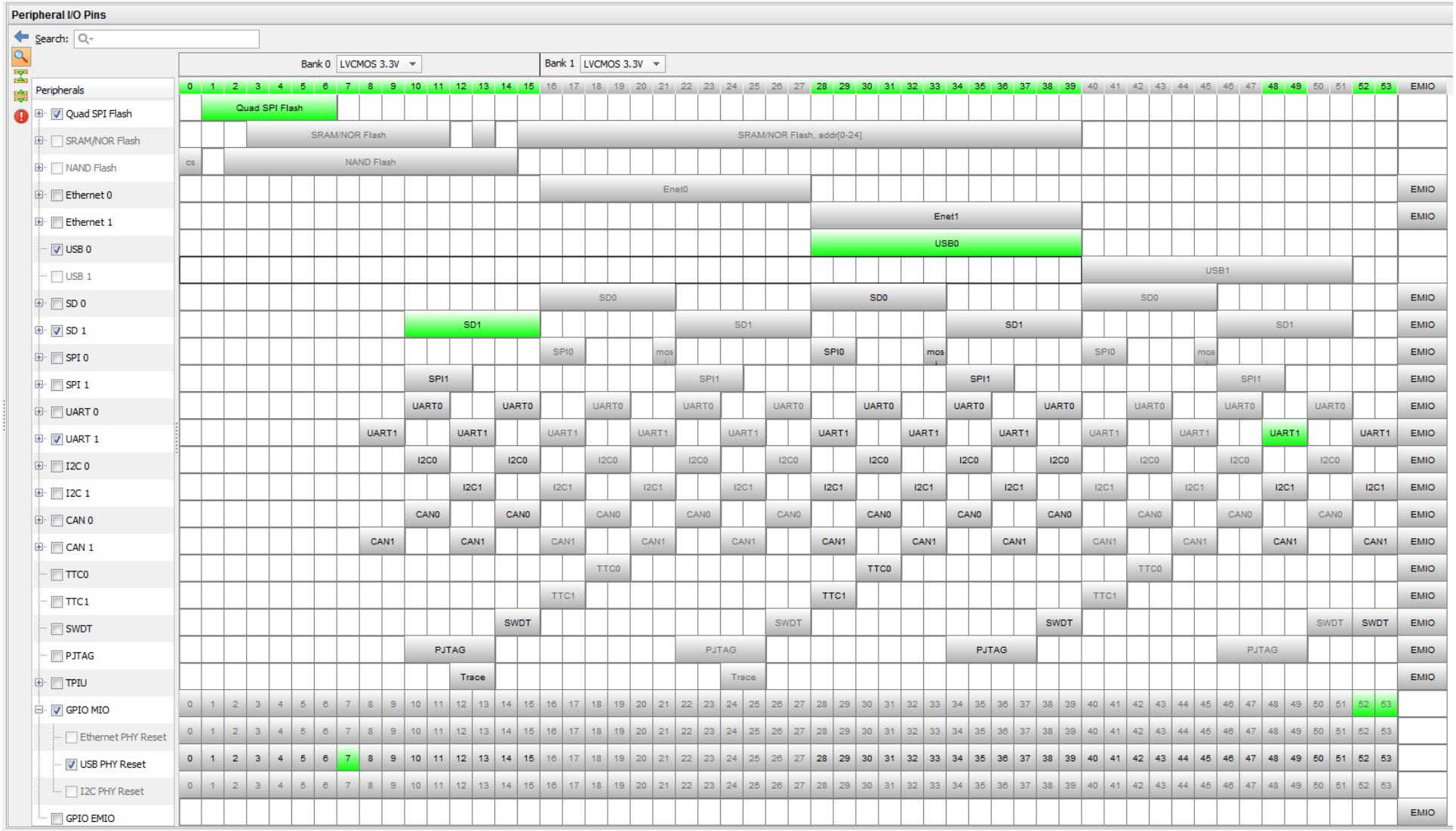


Figure 15 – Vivado Assignment of PS Peripheral I/O Pins

4.2 PL pin Allocations

Below are the assignments for the 54 PL I/O pins.

Table 14 – PL I/O Pin Assignments

I/O Bank	Voltage	Function	MIO Pins	Total I/O
34	3.3V	Wireless module		14
		BT_UART (with RTS,CTS)	4	
		SDIO	6	
		GPIO from Zynq	4	
		PCM	0	
		PMOD #1		8
		PMOD #2		8
		Arduino		22
		Data 0-7	8	
		Data 8-13	6	
		I2C (with Motion & Temperature sensor)	2	
35	3.3V	Address (shared with User Switch & LED)	6	
		Microphone		2
		Spare		0
		Total:		54

5 Boot Modes

This section is intended to show all of the user-adjustable boot mode switches and their default settings on MiniZed.

The Zynq pins MIO2 to MIO8 determine from which device it will boot. Some of these pins are shared with the QSPI device.

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common(1)				0	0	0	**JTAG Chain Routing(2)** 0: Cascade mode 1: Independent mode
NOR Boot(3)				0	0	1	
NAND				0	1	0	
Quad-SPI(3)				1	0	0	
SD Card				1	1	0	

- A pull-down resistor is placed on both the VMODE pins, MIO7 and MIO8, to signify 3.3V signal levels for both MIO pin banks
- The MiniZed design is cascaded boot mode by default, i.e. MIO2 pulled low. A 3-pad resistor jumper is provided (JT1) so that MIO2 can be tied high in order for an independent JTAG chain to be used.
- MIO3 is pulled low, as NOR boot is not supported
- MIO4 is pulled low, as NAND and SD card boot is not supported
- The MIO5 selection (boot from JTAG or QSPI flash) is determined by a surface mount switch, connected as follows

Table 15 – Boot Mode Switch Selections

Boot Mode		Default Setting	Function
SW1	PS_MIO[5]	J (VCC)	PS-PL JTAG Cascaded
SW1	PS_MIO[5]	F (GND)	QSPI Boot Mode

- In this case the boot mode select switch will be one of two switches in a dual surface mount switch (SW1). The second switch will go to the PL as a user select input. See Figure 16 for MiniZed Switch Location and for Boot Mode configuration see Figure 17.

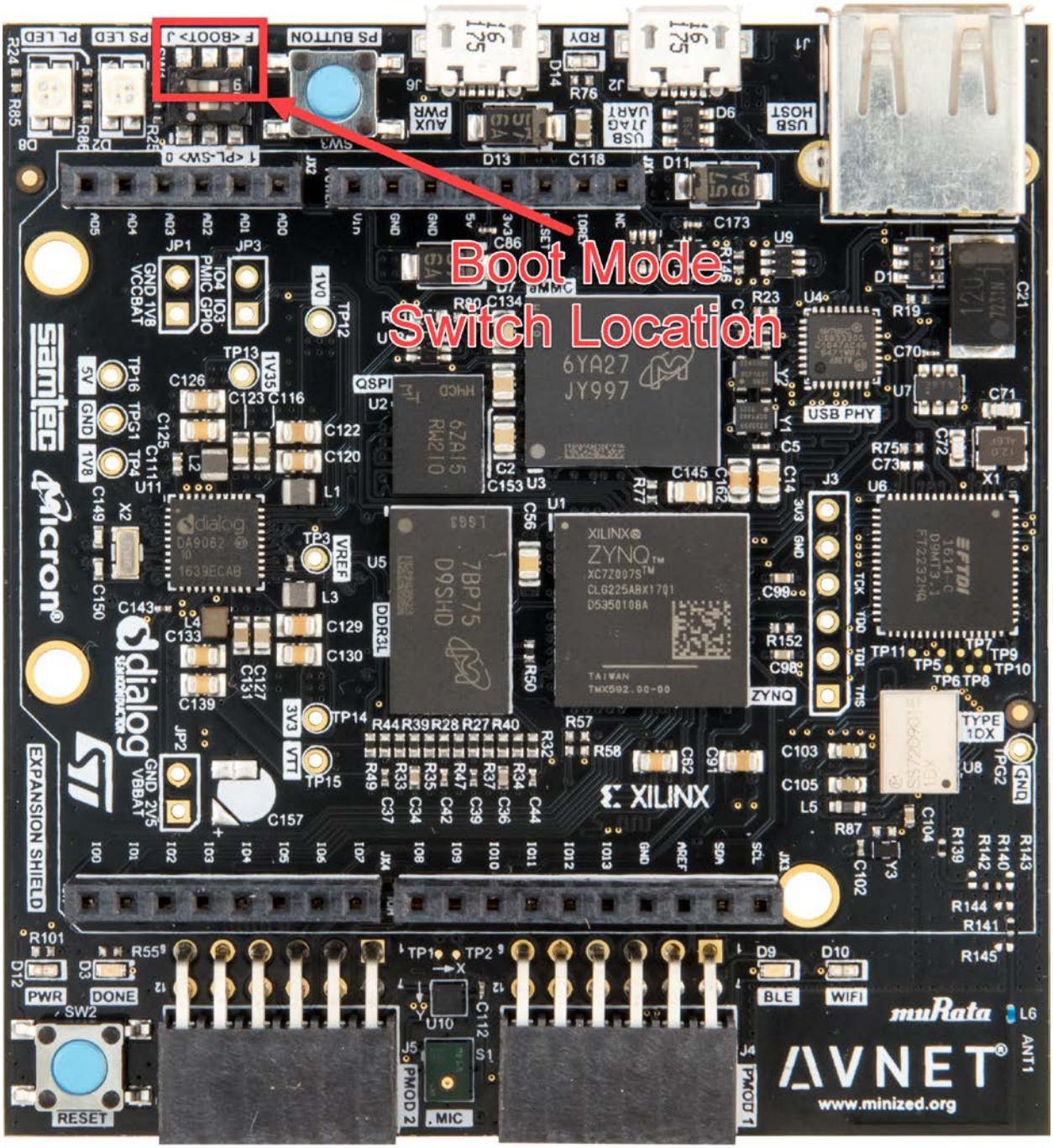


Figure 16 – MiniZed Switch Location

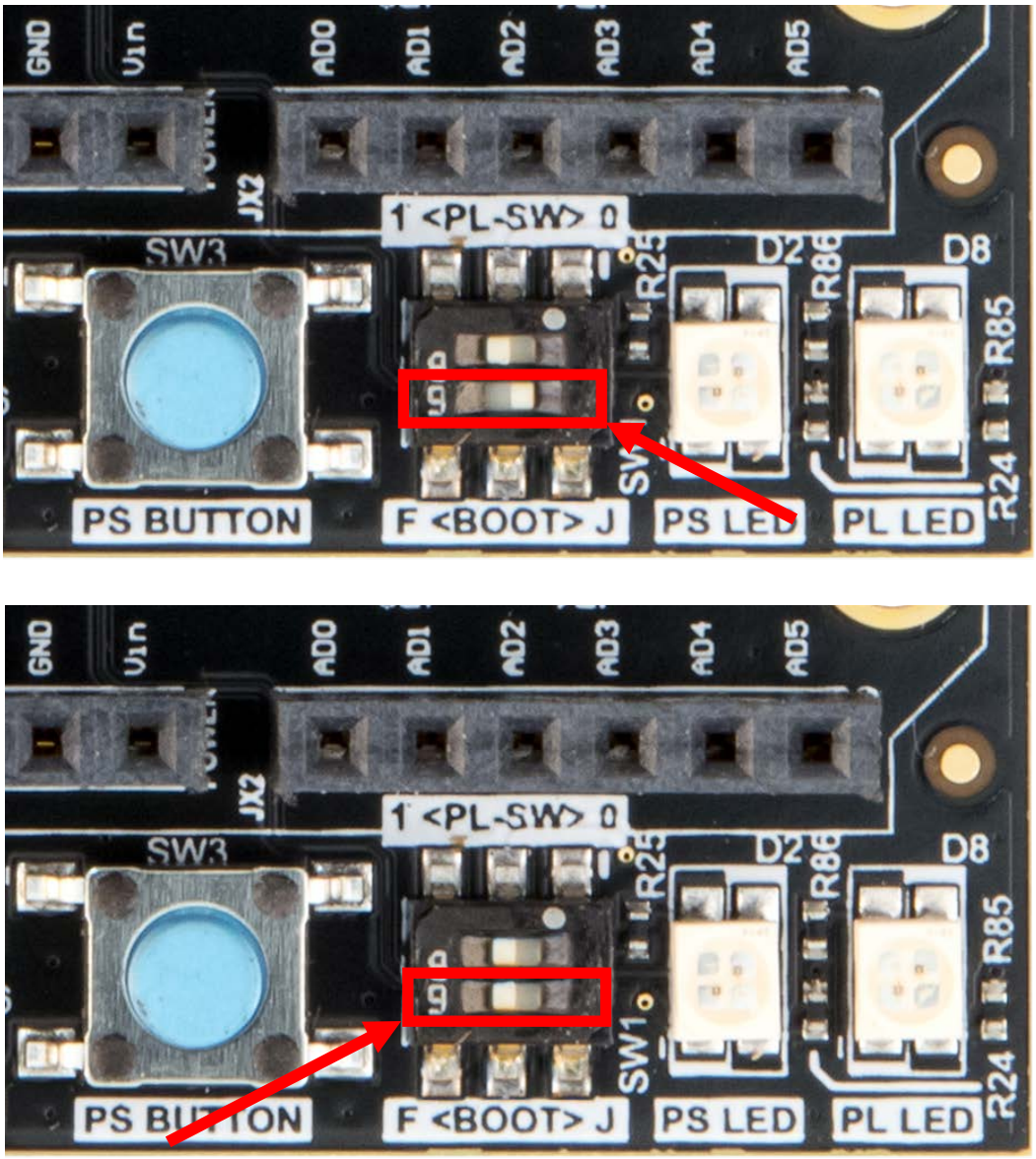


Figure 17 – Boot Modes (JTAG Top) (QSPI/Flash Bottom)

Mechanical

5.1 Weight

The MiniZed weighs 36 grams.

5.2 Measurements

MiniZed's step model is available on http://avnet.me/minized. The MiniZed measures 2.80" x 3.00" (71.12 mm x 76.2 mm)

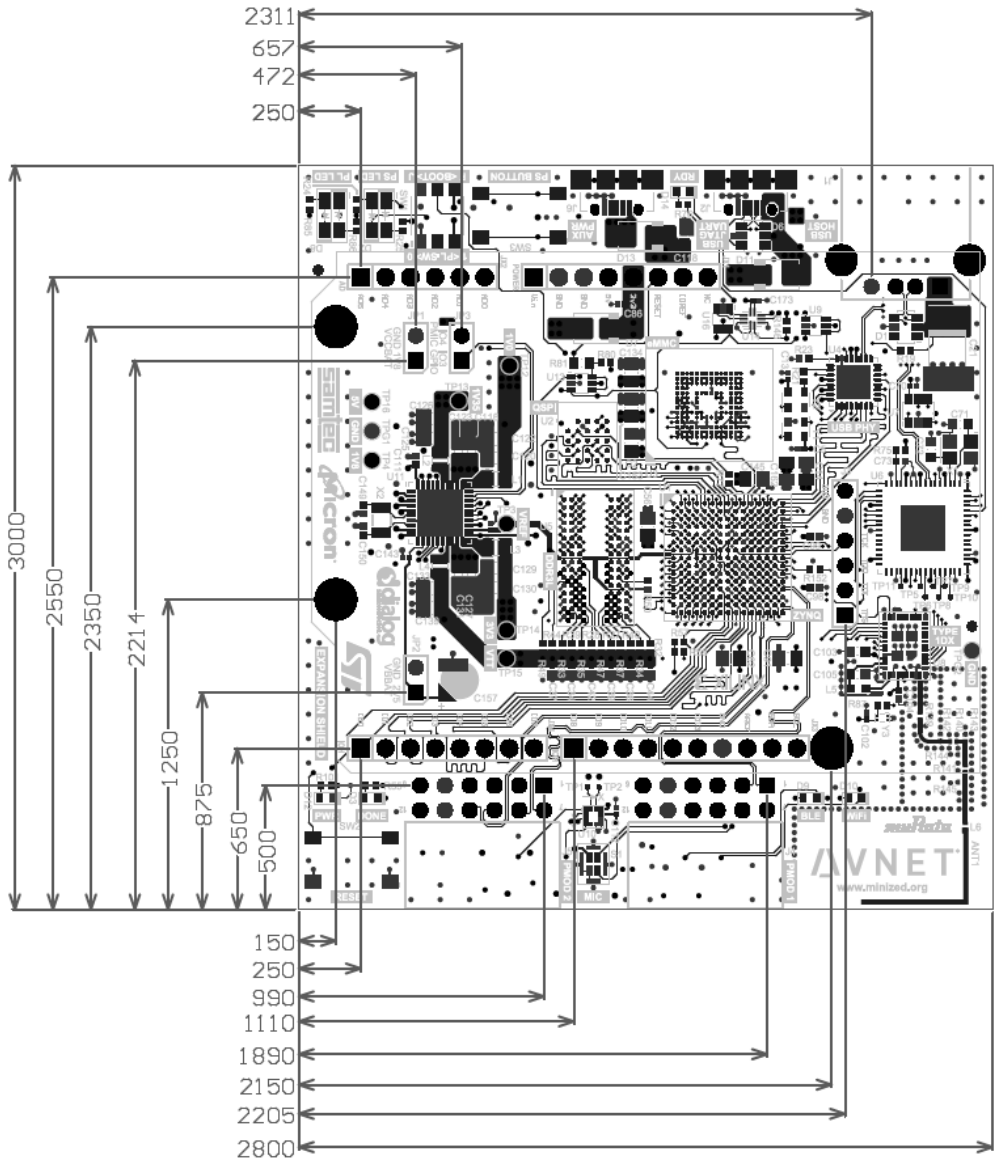


Figure 18 – MiniZed Top-Side Mechanical (Thousandths of an Inch)

6 Ordering Information

Part Number and hardware description for products mentioned above.

Table 16 – Ordering Information

Part Number	Hardware
AES-MINIZED-7Z007-G	MiniZed
AES-PMOD-SD	Avnet PMOD External SD Card Evaluation Module
AVTCB-10273	MONOPRICE 5V, 2.4A AC/DC Power Supply

7 Disclaimer

Avnet assumes no liability for modifications that the owner chooses to make to their MiniZed.