

Application note No. 1: building the hardware

Imaging solutions project objectives

ES FISSENTED BY An Avnex Combany This is the first of three application notes for creating imaging solutions using the 96Boards onsemi Dual Camera Mezzanine and Ultra96V2.

In this project, we demonstrate how to build the hardware design by using the 96Boards onsemi Dual Camera Mezzanine with the Avnet Ultra96V2 board.

The expected outcome of this project is a Xilinx Shell Archive (XSA) for use in the development of higher-level applications running in PetaLinux. This project will also explain the major elements of the hardware design in the Vivado® Design Suite to ensure later concepts and procedures are understood. We recommend the project outlined in this application note be created on a Xilinxsupported 64-Bit Linux operating system. The two subsequent application notes require creation and use of embedded Linux.

Getting started: requirements

The following hardware is required to follow this series of application notes:

- Ultra96V2 •
- Ultra96V2 power supply •
- 96Boards onsemi Dual Camera Mezzanine
- SD card

To implement this series of application notes, you will need the following Xilinx software installed:

- Vitis 2020.1, including Vivado 2020.1
- PetaLinux 2020.1 •
- Git •
- **Terminal application**

You'll need a few licenses for this implementation. Bitstreams for the Xilinx ZU3EG device can be generated license-free as part of the Xilinx Vivado webPACK. However, some of the IP used within this design requires an additional license. This license is provided with the Ultra96V2 and is marked "OEM Zyng ZU3 Ultra96 Vivado Design Edition with SDSoC Voucher Pack." Redeem this license and install it on the machine you're using to implement the project. Once it is installed, you can use the license manager (see Figure 1) to see the licensed IP, including the on-screen display.

VIVADO.	License Ma	anager				€ XILIN
4 Get License			View Lic	ense Status		
Set Proxy Obtain License Load License Manage License Manage License Manage License	Certificate Based Li	censes:			Filter: 🗹 Hide	e Free <u>B</u> uilt-in Licenses
✓ View License Status	License Name	Tools/IP	Expiration Date	VerNon Limit	License Type	Location
View System Information	board vivado de	Tools	Permanent	2022 02	Nodelocked	/home/adjuvo/ Xili
 U View Host Information 	mini csi2 rx ctrl	IP:Bought	Permanent	1.0	Nodelocked	/home/adjuvo/.Xili
	mipi_csi2_rx_ctrl	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	mipi csi2 tx ctrl	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	mipi csi2 tx ctrl	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili I
	mipi dsi tx ctrl	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili l
	mipi dsi tx ctrl	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	v cresample	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	v cresample	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili I
	v hdmi	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	v hdmi	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	v mix	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	v mix	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	v osd	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	v osd	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	v osd v1 0	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	V DFOC SS	IP-Bought	Permanent	1.0	Nodelocked	/home/adjuvo/ Xili
	v proc ss	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	y rab2ycrcb	IP-Bought	Permanent	1.0	Nodelocked	/home/adjuvo/ Xili
	v rgb2ycrcb v2	IP-Bought	Permanent	1.0	Nodelocked	/home/adiuvo/ Xili
	v rgb2vcrch v2	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/ Xili
	v rgb2vcrcd	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/ Xili
	vtc	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/ Xili
	vtc	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/ Xili
	v tog	IP:Bought	Permanent	1.0	Nodelocked	/home/adiuvo/.Xili
	v tog	IP:Bought	Permanent	2022.02	Nodelocked	/home/adiuvo/.Xili
	v verch2rah v2	ID-Dought	Pormonont	1.0	Nodolockod	/homo/adiuwo/ Vili
						•
					Clear	Cache <u>R</u> efresh

Figure 1. Check that the correct license is installed using the license manager.

Introduction to image sensor flexibility

The 96Boards onsemi Dual Camera Mezzanine provides support for two imaging sensors and is designed to be flexible, allowing support for a range of image sensors of varying color spaces and resolutions. To support a flexible integration, both image sensors are connected to an image coprocessor (Image Signal Processor or ISP) on the 96Boards onsemi Dual Camera Mezzanine (see Figure 2). The ISP merges the images into one and outputs a mobile industry processor interface (MIPI) stream to the Ultra96 board, where the image is recovered and processed by the Xilinx ZU3EG MPSoC.



Figure 2. 96Boards onsemi Dual Camera Mezzanine architecture

MIPI is a high-bandwidth, point-to-point protocol used to transfer image sensor or display information over several differential serial lanes. Like most protocols, it works on the OSI model with different layers of implementation. The lowest level of the MIPI protocol is the DPHY, which defines the number of lanes, clocking and the transition between differential (scalable low voltage swing, or SLVS) and single-ended signalling (LVCMOS).

This combination of high-speed differential and low-speed, single-ended signalling enables the highbandwidth transfer of the image/display data using a higher-level protocol such as CSI-2 or DSI. The low-speed communication enables the low-level protocol information to be communicated at lower power. Each MIPI DPHY link may have between one and four high-speed serial links operating at up to 2.5 Gbps or 10 Gbps across all four lanes. Data transfer over these lanes occurs at double the data rate and is synchronous to the clock lane.

The 96Boards onsemi Dual Camera Mezzanine comes with two CAV10-000A image sensors as standard. These offer a 1-megapixel resolution (1280 pixels by 800 lines) and output a grayscale image. To support high-speed operations the sensors offer a global shutter, which prevents artifacts that might appear in the image if a rolling shutter was used to capture high-speed images (see Figures 3 and 4).



Figure 3. Rolling shutter line by line read out



All Pixels Read After Integration



Grayscale imaging is popular for many industrial applications. In fact, one of the first operations in many image-processing systems is to convert the image from color to grayscale. For example, see this edge detection application where the first stage is converted to grayscale. Grayscale provides luminance information on the image, which is one of the most important factors in finding visual features. Elements such as brightness, contrast, edges, shape, contours, texture, perspective and shadow can be identified without the need for a color image.

Assembling Ultra96V2 and 96Boards onsemi Dual Camera Mezzanine

1. Ensure that the Ultra96V2 is powered off and the power supply is disconnected (see Figure 5).



Figure 2. Ultra96V2 and 96Boards onsemi Dual Camera Mezzanine board ready for assembly

2. Gently align the 96Boards onsemi Dual Camera Mezzanine board. Carefully align the high-speed and low-speed connector and press the two boards together.



Figure 3. Aligning the high-speed and low-speed connectors

3. Once both boards are mated, connect the power supply to the Ultra96V2 such that it is ready to power up when required (see Figure 7).



Figure 4. Assembled system ready for testing

Hardware project creation

1. Create a directory for the 96Boards onsemi Dual Camera Mezzanine. In Linux, use the command *mkdir -p <directory name>* once the directory is created cd into it (see Figure 8).

File Edit View Search Terminal Help	
CVD.c	slxplugin_download.tgz
CVD.cpp	slx_workspace
cvd.h	snap
cvd_tb.c	Templates
Desktop	u50_wksp
Documents	Videos
Downloads	vitis_2019_2
examples.desktop	vitis_pid11242.str
'FNP License-LicenseFile.lic'	vitis_pid11774.str
hdl_projects	vitis_pid13573.str
HLS	vitis_pid15044.str
home-share	vitis_pid6004.str
licenses	vitis_pid6459.str
<u>men</u> tor_intel	vivado_3697.backup.jou
mgc	vivado_3697.backup.log
minized	vivado.jou
Music	vivado.log
Packages	workspace
petalinux_2020.1	workspace_slx
Pictures	xilinx-zynqmp-common-v2020.1
proxy.txt	xrc.log
Public	
adiuvo@Adiuvo:~\$ cd hdl_projects	
adiuvo@Adiuvo:~/hdl_projects\$ m	kdir -p avnet_imaging

Figure 8. Creating the new directory

2. The next step is to clone the Avnet bdf repository (see Figure 9). From the command line inside the directory you just created, enter the command *git clone <u>https://github.com/Avnet/bdf.git</u>*

File Edit View Search Terminal Help		
examples.desktop	vitis pid11242.str	
'ENP license-licenseFile.lic'	vitis pid11774.str	
hdl projects	vitis pid13573.str	
HLS	vitis pid15044.str	
home-share	vitis pid6004.str	
licenses	vitis pid6459.str	
mentor intel	vivado 3697.backup.jou	
mgc	vivado_3697.backup.log	
minized	vivado.jou	
Music	vivado.log	
Packages	workspace	
petalinux_2020.1	workspace_slx	
Pictures	xilinx-zynqmp-common-v2020.1	
proxy.txt	xrc.log	
Public		
adiuvo@Adiuvo:~/hdl_projects/av	<pre>net_imaging\$ git clone https://github.com/Avnet/bdf.git</pre>	
Cloning into 'bdf'		
remote: Enumerating objects: 70	, done.	
remote: Counting objects: 100%	(70/70), done.	
remote: Compressing objects: 10	0% (54/54), done.	
remote: Total 327 (delta 27), r	eused 57 (delta 16), pack-reused 257	
Receiving objects: 100% (327/32	7), 23.20 MiB 3.54 MiB/s, done.	
Resolving deltas: 100% (124/124), done.	
adiuvo@Adiuvo:~/hdl_projects/av	net_imaging\$	

Figure 9. Cloning the Avnet bdf repository

3. The final repository to clone for this application note is the HDL repository (see Figure 10). Use the command git clone https://github.com/Avnet/hdl.git

nining utual in	
Music vivado.log	
Packages workspace	
petalinux_2020.1 workspace_slx	
Pictures xilinx-zynqmp-common-v2020.1	
proxy.txt xrc.log	
Public	
adiuvo@Adiuvo:~/hdl_projects/avnet_imaging\$ git clone https://github.com/Avnet/bdf.git	
Cloning into 'bdf'	
remote: Enumerating objects: 70, done.	
remote: Counting objects: 100% (70/70), done.	
remote: Compressing objects: 100% (54/54), done.	
remote: lotal 327 (delta 27), reused 57 (delta 16), pack-reused 257	
Receiving objects: 100% (32//32/), 23.20 MiB 3.54 MiB/s, done.	
Resolving deltas: 100% (124/124), done.	
adluvogAdluvo:~/ndl_projects/avnet_imaging\$ git Clone nttps://github.com/Avnet/ndl.git	
control into not	
remote: Enumerating objects: 207, uone.	
remote: Contractor above (26/26/), unie.	
remote: Complexity objects: 100% (114/114), $001e$:	
Tendet indiat 424 (detta 180), reused 200 (detta 103), pack-reused 4337	
Receiving objects. 100% (4024/4024), 3.42 mto 4.41 mto/s, done.	
adjuvo(Adjuvo:~/hdl projects/avnet imaging)	



4. With the repositories cloned, the next step is to ensure we check out the correct branch from the master. For the bdf repository, we want to work from the master branch. To do this, we cd into the newly cloned bf folder and execute the command *git checkout master* (see Figure 11).



Figure 11. Checking out the bdf master branch

5. For the HDL branch, we want to check out the 2020.1 branch. Use the command *git checkout* 2020.1 again from within the HDL folder (see Figure 12).



Figure 12. Checking out the 2020.1 branch of the HDL repository

6. With the repositories cloned and the correct branches checked out, the project can be created by using the project build script (see Figure 13). From within the HDL folder, CD into scripts and execute the command *Vivado -mode batch -source ./make_ultra96v2_dualcam.tcl*



Figure 13. Building the project using the project script

7. Following this command, the script will create the Vivado project, synthesize the design and implement the design for the Zynq ZU3EG device used on the Ultra96V2. This may take some time, depending upon the capabilities of the build machine. A typical build time may take about an hour.

Understanding the hardware project

With the project created, we can now explore the design that was created in Vivado (see Figure 14). To do this, we need to launch the Vivado GUI and open the project just created.

- 1. In the terminal window, enter the command Vivado and this will launch the Vivado GUI.
- 2. In the Vivado GUI, open the project ultra96V2_2020_1 under the Ultra96v2_dualcam directory in the HDL/Projects directory

<u>Eile Edit Flow Tools Reports</u>	Window Layout View Help Q- Quick Access					write_bitstream Complete 🗸
_ b _i < i ≠ i th i th i × i ▶ i ₽	🛊 Σ ½ //)/					💷 Default Layout 🗸 🗸
Flow Navigator 😤 🕆 ? 🗕	PROJECT MANAGER - ULTRA96V2					? ×
PROJECT MANAGER	Sources 2 D IS	×	Project Summary			2.0.6.×
Settings			Overview Deckhoo			
Add Sources		*	Overview i Dasriboa	10		0
Language Templates	Design Sources (1) Design Sources (1) Design Sources (1) ULTRA96V2 wrapper (ULTRA96V2 wrapper.v) (1)		Settings Edit			
👎 IP Catalog	> Constraints (1) Simulation Sources (1)		Project name:	ULTRA96V2	trate dual and UTRACE 2020.1	
 IP INTEGRATOR 	> 🖾 Utility Sources		Product family:	Zyng UltraScale+	101490V2_0041040100110490V2_2020_1	
Create Block Design			Project part:	Ultra96v2 Single Board Computer (xczu3eg-sbva484-1-i)	
Open Block Design			Top module name:	UITRA96V2_wrapper		
Generate Block Design			Target language: Simulator language:	Verllog 占 Mixed		
 SIMULATION 	Hierarchy IP Sources Libraries Compile Order					
Run Simulation			Board Part			
	Properties ? _ 🗆 🖾	×	Display name:	Ultra96v2 Single Board Computer		
 RTL ANALYSIS 	$(\Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow \Rightarrow $	•	Board part name:	avnet.com:ultra96v2:part0:1.1		
> Open Elaborated Design			Connectors:	Nev 2 No connections		
			Repository path:	/home/adiuvo/hdl projects/avnet imaging/bdf		0 11
STNTHESIS Due Conthesis			URL:	http://avnet.me/ultra96-v2		
 Run synchesis Once Cathering Design 	Select an object to see properties		Board overview:	Ultra96v2 Single Board Computer		
> Open synthesized besign						
 IMPLEMENTATION 			Synthesis		Implementation	Summary Route Status Failed Nets
Run Implementation			Status:	✓ Complete	Status: 🗸 wri	te bitstream Complete!
> Open Implemented Design				• • • • · · ·		
	Tcl Console Messages Log Reports Design Runs x					? _ D B
 PROGRAM AND DEBUG 	0, ₹ ≜ 4 ≪ ▶ ≫ + %					
Generate Bitstream	Name Constraints Status WNS	TN	S WHS THS TPWS	Total Power Failed Routes LUT FF BRAM URAM	DSP Start Elapsed	Run Strategy
> Open Hardware Manager	✓ ✓ synth_1 (active) constrs_1 synth_design Complete!			0 0 0.0 0	0 2/9/21, 9:21 PM 00:01:16	Vivado Synthesis Defaults (Vivado Synthesis 2
	✓ impl_1 constrs_1 write_bitstream Complete! -0.43	32 -2.	85 0.010 0.000 0.000	2.724 0 2182 312 65.5 0	109 2/9/21, 9:22 PM 00:08:39	Vivado Implementation Defaults* (Vivado Implementa
	V S Out-of-Context Module Runs				20121 0 15 PM 00 00 00	
	Submodule Runs Complete				2/9/21, 9:15 PM 00:06:09	
	N	-				/

Figure 14. Project open in Vivado

3. Open the block diagram (see Figure 15) to observe the design that has been implemented in the project and float the block diagram so that it is in its own window.



Figure 15. Block diagram opened in Vivado

4. Note how there are four hierarchical elements in the block design (see Figure 16). These blocks contain the Zynq MPSoC processing system, the capture pipeline, live video display port and the GPIO needed in the system.



Figure 16. Block diagram of the image processing system

 The clocking architecture (see Figure 17) of the design is critical and a multi-clock design is implemented with the 200MHz and 150MHz being used as references for the MIPI interface and the AXI Stream video processing network. The 48MHz clock is provided externally to the ISP.

Symbol Resource	Component Name	clk_wiz						
Show disabled ports	Clacking Option	c Output Clou	MMCM Satting	6 Summany				
	clocking option		in the section	s Journary				
	The phase is call	ulated relative to	Output Freg (MHz)		Phase (degrees)		Duty Cycle (%)	
	Output Clock	Port Name	Requested	Actual	Requested	Actual	Requested	A
	✓ clk_out1	clk_out1 🛞	200.000 🛞	200.00000	0.000 📀	0.000	50.000 🛞	50
	✓ clk_out2	clk48M 🛞	48 🛞	48 30000	0.000	0.000	50.000 🛞	50
	✓ clk_out3	clk_out3 🛛 🛞	148.5 🛞	150.00000	0.000	0.000	50.000 🛞	50
	Clk_out4	clk_out4	100.000	N/A	0.000	N/A	50.000	
	Clk_out5	clk_out5	100.000	N/A	0.000	N/A	50.000	
	Clk_out6	clk_out6	100.000	N/A	0.000	N/A	50.000	
clk out1	Clk out7	clk_out7	100.000	N/A	0.000	N/A	50.000	
locked		ck Sequence	e Number					
		1						
	clk_out1	+						
	clk_out1 clk_out2	1						
	clk_out1 clk_out2 clk_out3	1						
	clk_out1 clk_out2 clk_out3 clk_out4	1 1 1						
	clk_out1 clk_out2 clk_out3 clk_out4 clk_out5	1 1 1 1 1						
	clk_out1 clk_out2 clk_out3 clk_out4 clk_out5 clk_out6							
	clk_out1 clk_out2 clk_out3 clk_out4 clk_out4 clk_out6 clk_out7	1 1 1 1 1 1 1 1 1						
	ck_out1 ck_out2 ck_out3 ck_out5 ck_out6 ck_out6 ck_out7	1 1 1 1 1 1 1 1 1						

Figure 17. Clocking architecture

6. Double click on the capture pipeline (see Figure 18). This block contains the MIPI input IP, the video processing subsystem and the frame write buffer. This enables the image frames to be stored and accessed by the Zynq PS DDR.



Figure 18. Capture pipeline

7. Examine the configuration of the MIPI IP core and add in 896 Mbps for the line rate (see Figure 19).

umentation 🖆 IP Location							
how disabled ports	Component Name CAPTURE_PIPUINE/mipi_csi2_rx_subsyst_0						
	Configuration Shared Logic Pin Assignment Application Example Design						
	Subsystem Options						
	Pixel Format YUV422 8bit v Serial Data Lanes 4 v						
	✓ Include Video Format Bridge (VFB)						
	□ Support CSI Spec V2_0						
+ mipi_phy_if = + csirxss_s_axi rxbyteckhs -	DPHY Options						
	Line Rate (Mbps) 896 (80 - 1260)						
	✔ D-PHY Register Interface						
	✓ Enable HS and ESC Timeout Counters/Registers						
lite_aclk clkoutphy_out	HS Timeout (Bytes) 65541 (000 - 65541)						
dphy_clk_200M system_rst_out o	Escape Timeout (ns) 25600 (800 - 25600)						
video_aclk csirxss_csi_irq	CSI-2 Options						
Video_areseth	✓ CSI2 Controller Register Interface						
	Embedded non-image Interface						
	☐ Filter User Defined data types						
	Line Buffer Depth 8192 🗸						
	VER Ontions						
	Allowed VC All V Pixels Per Clock 2 V						
	TUSER Width 1 V						
	Resource improvement options						
	Resource improvement options						

Figure 19. MIPI IP configuration

8. Examine the Live Video Display Port (DP) block (see Figure 20). The output video path is through the live video DP output provided by the Zynq ZU3EG. To access this, the frame is read out of the processing system DDR memory and converted from an AXI Stream into a parallel video (pixel, HSync, VSync). This parallel video is timed by the video timing controller.



To demonstrate the capabilities of the image processing in programmable logic, a test pattern generator is also used along with the on-screen display IP block.

Figure 20. Live video DP block

9. Examine the Zynq block (see Figure 21). This element contains the configuration of processing system in the ZU3EG MPSoC.



Figure 21. The processing system block

10. Examine the GPIO block. This block slices a GPIO bus to provide individual reset and GPIO as required by the design.



11. Close Vivado. Open a file browser and examine the project directory. There is a file named ULTRA96V2.xsa and this is the Xilinx Shell Archive that we will be using in the next application note to customize the PetaLinux operating system for the design created in Vivado.

<	> 🔸 🏠 Home	hdl_projects avnet_imaging hdl Projects ultra96v2_dualcam ULTRA96V2_2020_1	Q = ≡ ● ® ⊗
0			
ŵ			
		.cache .hbs .hw .ip_userruns .sim .srcs log .xpr <mark>.xsa</mark> files	
۵			
⇒			
49			
ø			
	Videos		
	Rubbish Bin		
+	Other Locations		
			"ULTRA96V2.xsa" selected (137.5 MB)

Conclusion

This project shows how you can quickly and easily create the hardware design for a complex imaging system using Xilinx IP and Avnet ready-to-go build scripts, which enable you to hit the ground running in your application development.

EBV European Headquarters

EBV Elektronik GmbH & Co. KG | DE-85586 Poing | Im Technologiepark 2-8 | Phone: +49 8121 774 0 EBV Regional Offices | Status April 2021

AUSTRIA 1120 Wien Grünbergstraße 15/1, 4. Stock

Grunbergstraße 15/1, 4. Stock Phone: +43 1 89152 0 Fax: +43 1 89152 30

BELGIUM 1831 Diegem De Kleetlaan 3 Phone: +32 2 716001 0 Fax: +32 2 72081 52

BULGARIA 1505 Sofia 48 Sitnyakovo Blvd., Serdika offices,10th floor, Unit 1006 Phone: +359 2 9264 337 Fax: +359 2 9264 133

CZECH REPUBLIC 18600 Prague Amazon Court, Karolinska 661/4 Phone: +420 2 34091 011 Fax: +420 2 34091 010

DENMARK 8230 Åbyhøj Ved Lunden 10-12, 1. sal Phone: +45 8 6250 466 Fax: +45 8 6250 660

ESTONIA 80042 Pärnu Suur-Jõe 63 Phone: +372 5 8864 446

FINLAND 02180 Espoo Klovinpellontie 1-3, 6th floor Phone: +358 9 2705279 0 Fax: +358 9 27095498

FRANCE 91300 Massy Cedex (Paris) Le Copernic bât B 12 rue Jean Bart Phone: +33 1 644729 29

35510 Cesson Sévigné (Rennes) 35, av. des Peupliers Phone: +33 2 998300 51 Fax: +33 2 998300 60

67400 Illkirch Graffenstaden 35 Rue Gruninger Phone: +33 3 904005 92 Fax: +33 3 886511 25

31500 Toulouse 8 chemin de la terrasse Parc de la plaine Phone: +33 5 610084 61 Fax: +33 5 610084 74

69693 Venissieux (Lyon) Parc Club du Moulin à Vent 33, Av. du Dr. Georges Lévy Phone: +33 4 727802 78 Fax: +33 4 780080 81

GERMANY

85609 Aschheim-Dornach Einsteinring 1 Phone: +49 89 388 882 0 Fax: +49 89 388 882 020

10553 Berlin Kaiserin-Augusta-Allee 14 Phone: +49 30 747005 0 Fax: +49 30 747005 55 30938 Burgwedel Burgdorfer Straße 2 Phone: +49 5139 8087 0 Fax: +49 5139 8087 70

59439 Holzwickede Wilhelmstraße 1 Phone: +49 2301 94390 0 Fax: +49 2301 94390 30

41564 Kaarst An der Gümpgesbrücke 7 Phone: +49 2131 9677 0 Fax: +49 2131 9677 30

71229 Leonberg Neue Ramtelstraße 4 Phone: +49 7152 3009 0 Fax: +49 7152 759 58

90471 Nürnberg Lina-Ammon-Straße 19B Phone: +49 911 817669 0 Fax: +49 911 817669 20

04435 Schkeuditz Frankfurter Straße 2 Phone: +49 34204 4511 0 Fax: +49 34204 4511 99

78048 VS-Villingen Marie-Curie-Straße 14 Phone: +49 7721 99857 0 Fax: +49 7721 99857 70

65205 Wiesbaden Borsigstraße 36 Phone: +49 6122 8088 0 Fax: +49 6122 8088 99

HUNGARY 1117 Budapest Budafoki út 91-93, West Irodahaz Phone: +36 1 43672 29 Fax: +36 1 43672 20

4581500 Bnei Dror Tirosh 1 Phone: +972 9 77802 60 Fax: +972 3 76011 15

ITALY

ISRAEL

20095 Cusano Milanino (MI) Via Alessandro Manzoni, 44 Phone: +39 02 660962 90 Fax: +39 02 660170 20

50019 Sesto Fiorentino (FI) Via Lucchese, 84/B Phone: +39 05 543693 07 Fax: +39 05 542652 40

41126 Modena (MO) Via Scaglia Est, 31 Phone: +39 059 292 4211 Fax: +39 059 292 9486

00139 Roma (RM) Via de Settebagni, 390 Phone: +39 06 4063 665/789 Fax: +39 06 4063 777

35030 Sarmeola di Rubano (PD) Piazza Adelaide Lonigo, 8/11 Phone: +39 049 89747 01 Fax: +39 049 89747 26

10144 Torino (TO) Via Treviso, 16 Phone: +39 011 26256 90 Fax: +39 011 26256 91 IRELAND Fitzwilliam Hall Fitzwilliam Place Dublin 2 D02 T292 Phone: +353 1 4097 802

NETHERLANDS Zonnebaan 9 3542 EA Utrecht Phone: +31 346 5830 10 Fax: +31 346 5830 25

Fax: +35314568 544

NORWAY 1181 Oslo Brannfjellveien 11 Phone: +47 22 67 17 80 Fax: +47 22 67 17 89

POLAND 80-838 Gdansk Targ Rybny 11/12 Phone: +48 58 30781 00

P02-676 Warszawa Postepu 14 Phone: + 48 22 209 88 05

50-062 Wroclaw Pl. Solny 16 Phone: +48 71 34229 44 Fax: +48 71 34229 10

PORTUGAL

4400-676 Vila Nova de Gaia Unipessoal LDA / Edificio Tower Plaza Rotunda Eng. Edgar Cardoso, 23 - 14°G Phone: +351 22 092026 0 Fax: +351 22 092026 1

ROMANIA 020334 Bucharest

4C Gara Herastrau Street Building B, 2nd Floor - 2nd District Phone: +40 21 52816 12 Fax: +40 21 52816 01

RUSSIA

620028 Ekaterinburg Tatischeva Street 49A Phone: +7 343 31140 4 Fax: +7 343 31140 46

127486 Moscow Korovinskoye Shosse 10, Build 2, Off. 28 Phone: +7 495 730317 0 Fax: +7 495 730317 1

197374 St. Petersburg Atlantic City, Savushkina str 126, lit B, premises59-H, office 17-2 Phone: +7 812 635706 3 Fax: +7 812 635706 4

SERBIA 11070 Novi Beograd Milentija Popovica 5B Phone: +381 11 40499 01 Fax: +381 11 40499 00

SLOVAKIA 82109 Bratislava Turcianska 2 Green Point Offices Phone: +421 2 3211114 1 Fax: +421 2 3211114 0

 SLOVENIA

 1000 Ljubljana

 Dunajska cesta 167

 Phone: +386 1 5609 778

 Fax:
 +386 1 5609 877

SOUTH AFRICA

7700 Rondebosch, Cape Town Belmont Office Park, Belmont Road 1st Floor, Unit 0030 Phone: +27 21 402194 0 Fax: +27 21 4196256

3629 Westville Forest Square,11 Derby Place Suite 4, Bauhinia Building Phone: +27 31 27926 00 Fax: +27 31 27926 24

2128 Rivonia, Sandton Johannesburg 33 Riley Road Pinewood Office Park Building 13, Ground Floor Phone: +27 11 23619 00 Fax: +27 11 23619 13

SPAIN

08014 Barcelona c/Tarragona 149 - 157 Planta 19 1º Phone: +34 93 47332 00 Fax: +34 93 47363 89

39005 Santander (Cantabria) Racing n° 5 bajo Phone: +34 94 22367 55 Phone: +34 94 23745 81

28760 Tres Cantos (Madrid) c/Ronda de Poniente 14 - 2ª planta Phone: +34 91 80432 56 Fax: +34 91 80441 03

SWEDEN

16440 Kista Isafjordsgatan 32B, Floor 6 Phone: +46 859 47023 0 Fax: +46 859 47023 1

SWITZERLAND

8953 Dietikon Bernstrasse 394 Phone: +41 44 74561 61 Fax: +41 44 74561 00

TURKEY

06520 Ankara Armada Is Merkezi Eskisehir Yolu No: 6, Kat: 14 Ofis No: 1406, Sogutozu Phone: +90 312 2956 361 Fax: +90 216 5288311

34774 Ümraniye / Istanbul Tatlısu Mahallesi Pakdil Sokak 7 Phone: +90 216 528831 0 Fax: +90 216 528831 1

35580 Izmir Folkart Towers Manas BIv. No 39 B Blok Kat: 31 Ofis: 3121 Phone: +90 232 390 9196 Fax: +90 216 5288311

UKRAINE

03040 Kiev Vasilovskaya str. 14 off. 422-423 Phone: +380 44 496222 6 Fax: +380 44 496222 7

UNITED KINGDOM

Maidenhead (South) Berkshire, SL6 7RJ 2, The Switchback Gardner Road Phone: +44 16 28778556 Fax: +44 16 28783811

Manchester (North) M22 5WB Manchester International Office Centre Suite 3E (MIOC) Styal Road Phone: +44 16 149934 34 Fax: +44 16 149934 74

