PD69204T4 and PD69210

Datasheet

4-Port PSE PoE Manager and PSE PoE Controller

September 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in September 2019. The following is a summary of changes.

- Features (see page 3) section was updated.
- Features Description (see page 13) was updated.
- Main Voltage Monitoring (see page 17) section was updated.
- Typical PoE Application (see page 4) section was updated.
- PD69204T4 Pin Diagram (see page 21) was updated.
- Pin Description (see page 22) was updated.
- PD69204T4 Thermal Specifications (see page 33) were updated.
- Ordering Information (see page 44) was updated.

1.2 Revision 2.0

Revision 2.0 was published in May 2019 with minor editorial corrections.

1.3 Revision 1.0

Revision 1.0 was first published in March 2019. It was the first publication of this document.

2 Product Overview

Microsemi's PD69204T4 Power over Ethernet (PoE) manager IC integrates power, analog, and state-of-the-art logic into a single 56-pin, plastic QFN package. The device is used in Ethernet switches and midspans, to allow network devices to share power and data over the same cable. The PD69204T4 device is a 4-port, mixed-signal, and high-voltage PoE driver. Together with the PD69210 external MCU, it performs as a PSE system. Microsemi's PoE controller, PD69210, is a cost-effective, pre-programmed MCU designed to implement enhanced mode.

PD69204T4/PD69210 chip-set supports PoE Powered Device (PD) detection, power-up, and protection according to IEEE standards, as well as legacy/pre-standard PD detection. It provides PD real-time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit, and enables operation in a standalone mode. It also executes all real-time functions as specified in IEEE802.3at/bt high-power and Power Over HDbaseT (PoH) standards, including PD detection, and classification; using Multiple Classification Attempts (MCA).

Note: The chip-set supports typical power level of 95 W.

PD69204T4 supports supply voltages between 32 V and 57 V, without additional power supply sources. A system that powers over four pairs can be implemented by combining two ports of PD69204T4, enabling an extra feature for a simple and low-cost, high-power PD device. On-going monitoring of system parameters for the host software is available through communication. Internal thermal protection is implemented in the chip. PD69204T4 is a low-power dissipation device, that uses internal MOSFETs and internal 0.1 Ω sense resistors.

PD69210 features an ESPI bus for all PD69204T4 devices. It is developed on the basis of the Microchip SAM D21 family, that is embedded with the 32-bit Cortex-M0+ MCU core. It uses I^2C or UART interface to the host CPU, and is designed to support software field upgradable through the communication interface.

PD69204T4 is available in a 56-pin, 8 mm x 8 mm QFN package. PD69210 is available in 32-pin, 5 mm x 5 mm QFN package.

2.1 Features

- Four independent channels
- Complies with IEEE802.3af-2003, IEEE802.3at-2009 (including two-event classification), and IEEE802.3bt
- Supports Fast PoE
- Supports Perpetual PoE
- Supports three- and six-event Power over HDBaseT (PoH) Classification
- Drives 2-pair power ports or 4-pair ports
- Supports pre-standard PD detection
- Single DC voltage input (32 V to 57 V)
- Built-in 3.3 V and 5 V regulators
- Input voltage out of range protection
- Wide ambient temperature range: –40 °C to 85 °C
- On-chip over-temperature thermal protection and monitoring
- Low-power dissipation (0.1 Ω sense resistor and 0.2 Ω MOSFET Rdson per channel)
- Includes Reset command pin
- 4 x direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable PSE IEEE Type AT/AF/BT and PoH modes
- Power soft start mechanism
- Voltage monitoring/protection
- Internal power on reset
- Emergency power management supporting four configurable power bank I/Os
- Advance System Power Management algorithm supports up to 96 physical ports
- Can be cascaded up to 12 PoE devices (96 ports)
- Easy system implementation of PD69208T4 and PD69204T4 for multiplications of four ports systems. That is, 12-port system consists of 1×PD69208T4 and 1×PD69204T4.
- Supports both UART and I^2C interfaces to host CPU
- LED stream support
- System OK indication
- Disable ports input pin
- Software download through I^2C or UART
- Detailed port status
- Programmable threshold temperature alarm limit
- Interrupt out pin for system and port events
- Forced port power ON function
- Port power limit setting
- Port matrix and priority
- Automatic PoE device type detection
- PD69210: MSL1, RoHS compliant
- PD69208T4: MSL3, RoHS compliant

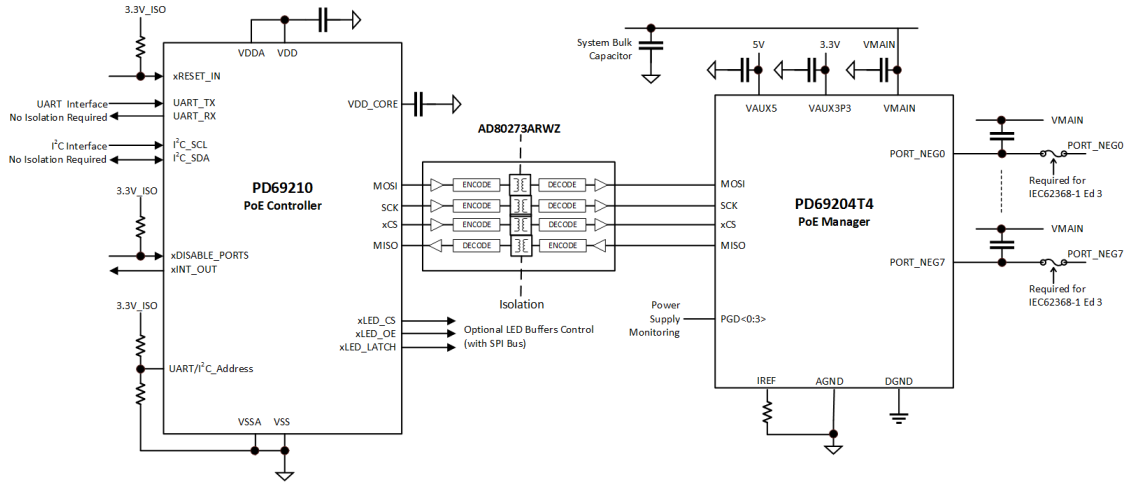
2.2 Applications

- PoE (all IEEE compliant 2-pair modes)
- Supports 4-pair, IEEE802.3bt, and POH
- PSE Switches/Routers/Midspans
- Industrial automation
- PoE for LED lighting

2.3 Typical PoE Application

The following figure shows the typical PoE application of PD69204T4 and PD69210 devices.

Figure 1 • Typical PoE Application



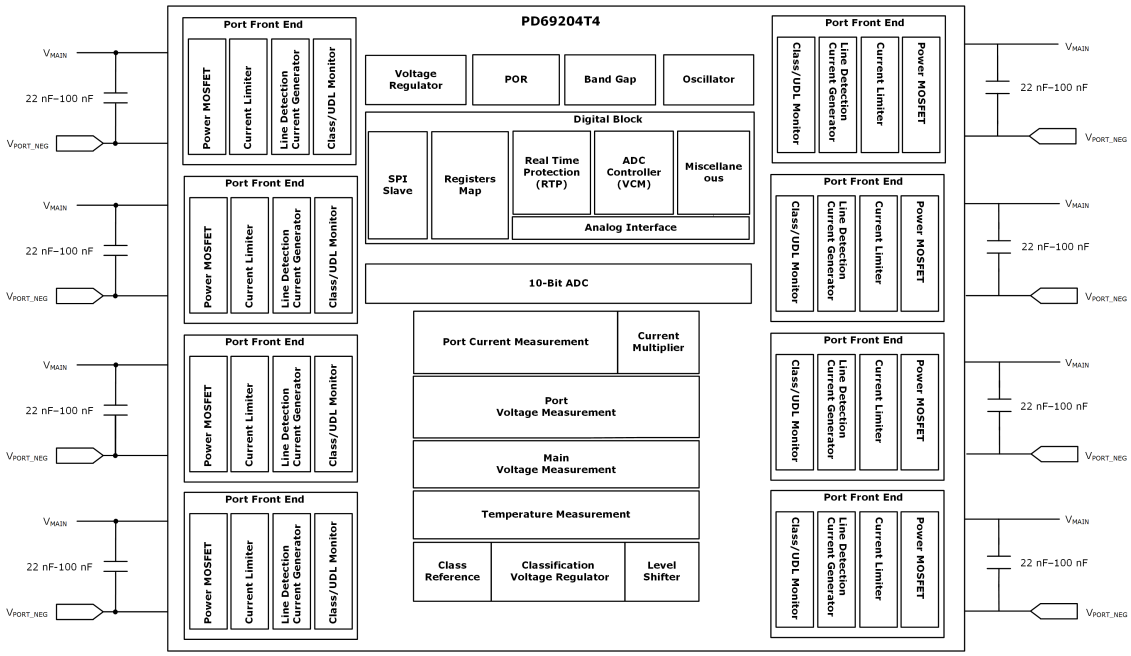
Note: Consult Microsemi AN240 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System (Document Number: PD-000359851) for complete reference design.

Fuses per port are not required for use in circuits with a total power level of up to 3 kW. This isbecause PD69208 is a UL 2367 (category QVRQ2)-recognized component and fulfills limited power source (LPS) requirements of the latest editions of IEC60950-1 and EN60950-1. However, IEC62368-1 which was released in October 2018 and is effective from December 2020, requires per port fuses for asystem power supply greater than 250 W.

3 Functional Descriptions

The following figure shows the functional blocks of the PD69204T4 device.

Figure 2 • PD69204T4 Block Diagram



The following sections describe the functional blocks of the PD69204T4 device.

3.1 Digital Block Module

The logic main control-block includes digital timing mechanisms and state machines that synchronize and activate PoE functions, according to PD69210 control commands, such as the following.

- Real-Time Protection (RTP)
- Start-Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring (VCM)
- ADC interfacing
- Direct digital signals with analog block
- SPI communication block
- Registers

3.2 PD Detection Generator

On request from PD69210 to the main control module, the PD detection generator generates four different voltage levels to ensure a robust AF/AT/BT PD detection functionality.

3.3 Classification Generator

On request from PD69210 to the main control module, state machine applies a regulated class event and mark event voltage to ports, as required by IEEE standards.

3.4 Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a pre-defined value set by AF/AT/BT/PoH. When the current value exceeds this specific value, the system measures the elapsed timing. If this interval is greater than a preset threshold, the port is disconnected.

3.5 Main Power MOSFET

The main power switching FET is used to control PoE current into the load.

3.6 Analog to Digital Converter

A 10-bit analog to digital converter (ADC) is used to convert analog signals into digital registers for the logic control module.

3.7 Power on Reset

Power on Reset (PoR) monitors the internal 3.3 V and 5 V DC levels. If this voltage drops below the specific thresholds, a reset signal is generated, and PD69204T4 is reset.

3.8 Voltage Regulator

The voltage regulator generates 3.3 V and 5 V for internal circuitry. These voltages are derived from V_{MAIN} supply. To use the internal voltage regulator, connect the following.

- V_{AUX5} to DRV_VAUX5
- V_{AUX3P3} to VAUX3P3_INT

The three options to reduce PD69204T4 power dissipation by regulating voltage outside the chip are as follows.

- Use an external NPN transistor to regulate the 5 V. In this setup, the configuration of regulators pins must be as follows.
  - DRV_VAUX5 is connected to NPN BASE
  - V_{AUX5} is connected to NPN EMITTER (connect collector to V_{MAIN})
  - V_{AUX3P3} is connected to VAUX3P3_INT
- Supply PD69204T4 with an external 5 V voltage regulator. In this setup, regulators pins configuration must be as follows.
  - V_{AUX3P3} is connected to VAUX3P3_INT
  - DRV_VAUX5 is not connected (left open)
  - V_{AUX5} is connected to external 5 V
- Supply PD69204T4 with an external 3.3 V voltage regulator. In this setup, regulators pins configuration must be as follows.
  - V_{AUX5} is connected to DRV_VAUX5
  - VAUX3P3_INT is not connected (left open)
  - V_{AUX3P3} is connected to external 3.3 V

These options can be implemented simultaneously to reduce power dissipation.

3.9 Clock

PD69204T4 clock (CLK) is an internal 8 MHz clock oscillator.

3.10 SPI Communication

PD69204T4 uses SPI communication in SPI slave mode to communicate with the PD69210 MCU. Each PD69204T4 has an address determined by ADDR0-ADDR3 pins. The PD69210 can support up to 12 ICs at addresses, 0–11. The actual frequency between PD69210 and PD69204T4 ICs is 1 MHz.

The following table lists the SPI communication packet structure.

Table 1 • SPI Communication—Packet Structure

Control Byte Selects PD69204T4 According to Address	R/W Bit	Internal Register Address	Number of Words (Read Access Only)	Data Written to IC (Write Access Only) Read from IC (Read Access Only)
8 bits	R(0)/W(1)	8 bits	8 bits	16 bits

3.10.1 SPI Addressing

PD69204T4 operates in the 8-bit address and 16-bit data. It responds to SPI transaction, if the first SPI byte (IC address byte bits [7:1]) complies with the following.

Table 2 • SPI Addressing

3 Bits (bit 7:5)	4 Bits (bit 4:1)	1 Bit (bit 0)
000	Address Input Pin	Read/Write

3.10.2 Broadcast

- A broadcast command is used to instruct all connected PD69204T4 ICs to perform a specific operation.
- The broadcast command is a write command with the standard packet structure. In a broadcast read operation, the read data is not valid and the read operation has no impact.

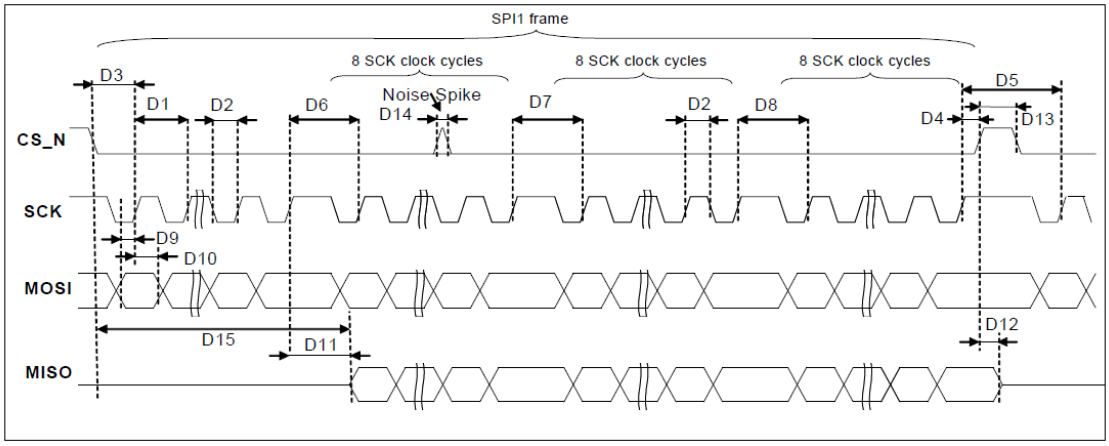
The following table lists the values of PD69204T4 broadcast.

Table 3 • Broadcast

3 Bits (bit 7:5)	4 Bits (bit 4:1)	1 Bit (bit 0)
001	0000	Write

The following figure shows the SPI timing of PD69204T4.

Figure 3 • SPI Timing Diagram



The following table lists the SPI timing diagram description.

Table 4 • SPI Timing Diagram Description

Name	Minimum Delay	Maximum Delay	Description
D1	910 ns		SPI clock period
D2	45 %	55 %	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock positive edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock positive edge (delay before SPI_CS inactive signal)
D5	2 SPI clock cycles		Delay between last SCK in SPI1 frame and first SCK at adjacent SPI1 frame
D6	1 SPI clock cycle		Between byte 0 (IC address) and byte 1 (address)
D7	1 SPI clock cycle		Between byte 1 (address) and byte 2 (data)
D8	1 SPI clock cycle		Between byte 2 (MS data byte) and byte 3 (LS data byte)
D9	340 ns		MOSI setup time
D10	340 ns		MOSI hold time
D11		700 ns	MISO tri-state to valid data from clock positive edge
D12		700 ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycle		SPI_CS width (Delay SPI1 frame to adjacent SPI1 frame)
D14		60 ns	Filtered glitch width
D15		D3 + D11 + 24 SPI clock cycles	MISO tri-state from SPI_CS negative edge to valid data
D16	200 ns		MISO setup to SCK positive edge
D17	200 ns		MISO hold to SCK positive edge

3.10.3 PD69210 I²C Address Selection

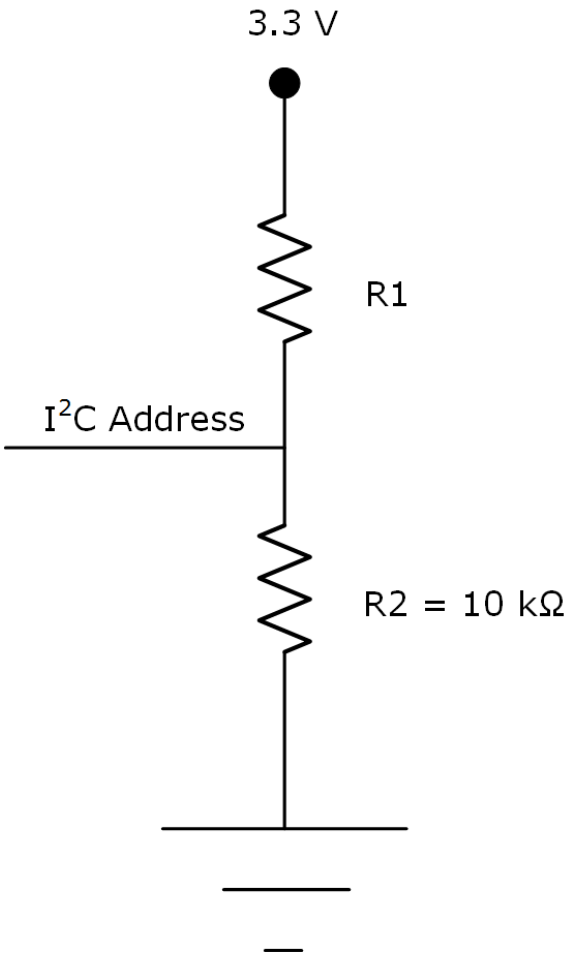
The I²C interface between the host CPU and a specific PD69210 requires setting the PD69210 address. This is done by applying a specific voltage level to pin number 13 (I2C_ADDR_MEAS), as listed in the following table.

Table 5 • I²C Address Selection

I²C_ADDR Voltage Low Level (V)	I²C_ADDR Voltage High Level (V)	I²C Address (Hexadecimal)	R1–KΩ (1 %)
0	0.11875	UART	N.C
0.15625	0.25625	0x4	147
0.29375	0.39375	0x8	86.6
0.43125	0.53125	0xC	57.6
0.56875	0.66875	0x10	43.2
0.70625	0.80625	0x14	34
0.84375	0.94375	0x18	26.7
0.98125	1.08125	0x1C	22.1
1.11875	1.21875	0x20	18.2
1.25625	1.35625	0x24	15.4
1.39375	1.49375	0x28	13
1.53125	1.63125	0x2C	11
1.66875	1.76875	0x30	9.31
1.80625	1.90625	0x34	7.87
1.94375	2.04375	0x38	6.49
2.08125	2.18125	0x3C	5.49

The following figure shows the I²C address selection of the PD69204T4 device.

Figure 4 • I2C Address Selection



UART communications configuration:

- Bits per second: 19,200 bps
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

I^2C communication configuration:

- Address: 7 bits
- Clock stretch: Host must support
- Transaction: 15 bytes or 1 byte

4 Electrical Specifications

This section describes the electrical specifications of the PD69210 and PD69204T4 devices.

4.1 PD69210 Electrical Characteristics

In this application, PD69210 consumption is approximately 20 mA.

- Manufacturer: Microchip
- Manufacturer part number: PD69210
- Maximum pull-ups consumption based on PD69210 application is 2 mA. See the hardware application note document: AN240 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System (Document Number: PD-000359851).

4.2 PD69210 Features Description

The following table lists the main features of the PD69210 device.

Table 6 • Features Description

Features	Description
Supports up to 12 PoE devices–96 physical ports (48 logical)	Up to 12 PoE devices can be cascaded, fitting into a 96-physical-port PoE system that uses one PoE controller (PD69210 can support up to 48 logical ports). A logical port can be built from 2×physical ports or 1×physical port.
Power management	The system supports three power management modes: Class (LLDP), Dynamic, and Static.
Threshold configuration	Over-voltage and under-voltage thresholds can be configured for disconnection purposes.
Fast PoE	Ability of a system to quickly boot and power up ports without loading EEPROM firmware.
Perpetual PoE	Ability of a POE system to maintain PoE power while switch host firmware is being loaded.
High-power Ports (2 pairs or 4 pairs)	PoE devices can be configured (both hardware and software) to enable higher current through ports (up to 948 mA) or double power at the RJ in case of four pairs.
Communication	Supports both I^2C and UART interfaces with the host CPU.
Legacy (reduced capacitance) detection	Enables detection and powering of pre-standard devices (PDs) up to 30 µF.
LED stream	Provides a direct SPI interface to an external LED stream circuitry. Enables designers to implement a simple LED circuit that does not require a software code. LED stream clock frequency is 1 MHz.
System OK indication	System validity indication. Provides a digital output to the host. Digital output is low when the system state is OK.The output behavior is controlled by software mask register settings (Mask 0×28). The mask default setting is 0, which means that this pin indicates valid software, and V_{MAIN} is within the range. This pin is active low. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
System and port measurements	Measurements of the following parameters: Current (mA), Power Consumption (W), V_{MAIN} (V), Port Voltage (V), and PD Class (0–4).
Detailed port status	Port statuses are received from PoE managers. Statuses, such as a port on and port off due to disconnection or overload.
Interrupt pin	Interrupt out from PoE controller, PD69210, indicating events such as port on, port off, port fault, PoE device fault, voltage out of range, and so on. For a full list of interrupt events, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
Port power limit	Configurable port power limit; when a port exceeds the limit, it is automatically disconnected.
Port matrix control	Enables layout designers to connect any physical port to any logical port as required.
'Power Good' interrupt from power supply to PoE drivers	For systems comprising more than a single power supply, when one power supply fails, a fast port disconnection mechanism is executed to maintain operation and prevent the collapse of other power supplies.

4.3 PD69204T4 Electrical Characteristics

Unless otherwise specified under conditions, the minimum and maximum ratings stated in the following table apply to the entire specified operating ratings of the device. Typical (Typ) values stated are either by design or by production testing at 25 °C ambient.

Table 7 • Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
V_{MAIN}	Main Supply Voltage	Supports Full IEEE802.3af/at/bt functionality	32		57	V
V_{PORT}	Port Output	V_{MAIN}–V_{PORT_NEGx}	0		57	V
V_{TH}	POR Threshold	Internal or External 3.3 V supply		8		V
I_{MAIN}		Main Power Supply Current at Operating Mode. V_{MAIN} = 55 V		14		mA
V_{AUX5}	5 V Output Voltage	V_{AUX5}–AGND	4.5	5	5.5	V
V_{AUX3P3}	3.3 V Output Voltage	V_{AUX3P3}–AGND	3	3.3	3.6	V
I_{AUX3P3}	3.3 V Output Current for application use	Without external NPN			5	mA
		With external NPN transistor on V_{AUX5}			30	mA
V_{AUX3P3_IN}	3.3 V Input Voltage	V_{AUX3P3}–AGND	3	3.3	3.6	V
DV_{DD}	Digital 3.3 V Input Voltage	DVDD–DGND	3	3.3	3.6	V
POR_{TP}	Power On Reset DV_{DD} Trip Point	DV_{DD}–DGND	2.575	2.775	2.975	V
POR_{HYS}	Power On Reset DV_{DD} Hysteresis	POR_{TP}–DGND	0.2	0.25	0.3	V
R_{CH_ON}	Total Channel Resistance	R_{ds_on} + R_{sense} + $R_{bonding}$		0.34		Ω

Table 8 • PD69204T4 Detection

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
V_{OC}	Pre-Detection Voltage, Open-Circuit Voltage	V_{MAIN}–V_{PORT_NEGx}, open port			7.8	V
V_{VALID}	Detection Voltage	V_{MAIN}–V_{PORT_NEGx}, for IEEE802.3 compliant signature resistance (R_{SIG} < 33 K)			9.3	V
I_{SC}	Short Circuit Current	V_{MAIN}–V_{PORT_NEGx} = 0 V		388	408	µA
R_{SIG_LOW}	Minimum Valid Detection Resistance		15		19	KΩ
R_{SIG_HIGH}	Maximum Valid Detection Resistance		26.5		33	KΩ

Table 9 • PD69204T4 Classification

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
V_{CLASS}	Class Event Output Voltage	V_{MAIN}–V_{PORT_NEG}x; 0 mA £ I_{PORT} £ 50 mA	15.5	18	20.5	V
V_{MARK}	Mark Event Output Voltage	V_{MAIN}–V_{PORT_NEGx}; 0.1 mA £ I_{PORT} £ 5 mA	7	8.5	10	V
I_{CLASS_LIM}	Class Event Current Limitation	V_{MAIN}–V_{PORT_NEGx} = 0 V	51	70	100	mA
I_{MARK_LIM}	Mark Event Current Limitation	V_{MAIN}–V_{PORT_NEGx} = 0 V	51	70	100	mA
	Classification Current Thresholds	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
		Class Error	51		100	mA

Table 10 • PD69204T4 Port Real-Time Protection

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
T_{RISE}	Turn on rise time	From 10 % to 90 % of the voltage difference at the V_{PORT_NEGx} in POWER_ON state from the beginning of POWER_UP	15			µs
I_{INRUSH}	Output current in POWER_UP state	C_{LOAD} ≤ 180 µF[1]	400	425	450	mA
T_{INRUSH}	Inrush time				65	mS
I_{PORT}	Output operating current	802.3af	10		360	mA
		802.3at	10		620	mA
		802.3bt class 5	10		560	mA
		802.3bt class 6	10		692	mA
		802.3bt class 7	10		794	mA
		802.3bt class 8	10		948	mA
I_{CUT}	Overload current	802.3af		375		mA
		802.3at		645		mA
		802.3bt class 5		589		mA
		802.3bt class 6		709		mA
		802.3bt class 7		825		mA
		802.3bt class 8/PoH[2]		980		mA
T_{CUT}	Overload time limit		62	64	66	mS
I_{LIM}	Port current limit	802.3af	400	425	450	mA
		802.3bt class 1–3	670	720	770	mA
		802.3at, 802.3bt class 4–6	790	850	892	mA
		802.3bt class 7–8/PoH	1020	1150	1300	mA
T_{LIM}	Port current limit time	V_{MAIN}–V_{PORT_NEGx} < 30 V	1	2	3	mS
P_{PWR}	Port power accuracy	> 90 W			2	%
I_{UDL}	DC disconnect under-load current	2 Pairs	6	7.5	9	mA
		4 Pairs (for each pair-set)	2	2.5	3	mA
T_{MPDO}	PD maintain power signature dropout time limit		322	324	326	mS
T_{MPS}	PD maintain power signature time for validity	802.3bt PSE Type 1, 2	46	48	50	mS
		802.3bt PSE Type 3, 4	3	4	5	mS
T_{OFF}	Turn off time	From V_{MAIN} to 2.8 V			500	mS

1. Can be overridden by communication command.

2. The power port is limited to the maximum of 100 W according to UL's LPS requirements (Port Power = $I_{PORT} \times V_{MAIN}$).

Table 11 • Port Current Monitoring

Symbol	Conditions	Typ	Maximum	Units
Resolution	Reported as 14 bits	10		Bits
LSB		122.07		µA
Measurement Period		16		mS
Accuracy	50 mA < I_{PORT} < 150 mA		9	%
	150 mA < I_{PORT} < 350 mA		4.5	%
	350 mA < I_{PORT} < 600 mA		3.5	%
	600 mA < I_{PORT} < 800 mA		3.0	%
	I_{PORT} > 800 mA		1.5	%

Table 12 • Port Voltage Monitoring

Symbol	Typ	Maximum	Units
Resolution	10		Bits
LSB	58.6		mV
Measurement Period	3		mS
Accuracy		3.3	%

Table 13 • Main Voltage Monitoring

Symbol	Conditions	Typ	Maximum	Units
Resolution		10		Bits
LSB		58.6		mV
Measurement Period		3		mS
Accuracy	42 V < V_{MAIN} < 50 V		2.1	%
	50 V < V_{MAIN} < 57 V		1.5	%
	50 V < V_{MAIN} < 57 V[1]		0.6	%

1. 0 °C–70° C

Table 14 • Temperature Monitoring

Symbol	Conditions	Minimum	Typ	Maximum	Units
Resolution			8		Bits
LSB	Temperature = (DATA x 1.9384) – 277		1.9384		°C
Measurement Period			3		mS
Accuracy		–3		3	°C

Table 15 • Digital Interface

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
V_{IH}	Input Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3]	2.2			V
V_{IL}	Input Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3]			0.8	V
Hyst	Input Logic Hysteresis Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3]	0.4	0.6	0.8	V
I_{IH}	Input Logic High Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3]	–10		10	µA
I_{IL}	Input Logic Low Current	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3]	–10		10	µA
V_{OH}	Output Logic High Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3] I_{OH} = –1 mA	2.4			V
V_{OL}	Output Logic Low Voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD [0..3], ADDR[0..3] I_{OH} = 1 mA			0.4	V

Table 16 • Immunity

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
ESD	ESD rating	HBM[1]				
	ESD rating	CDM[2]				
Surge	Lightning surge[3]	EN61000 4–5	–1		1	KV

1. ESD HBM complies with JESD22 Class 2 standard.
2. ESD CDM complies with JESD22 Class 1 standard.
3. System-level common mode 10 µS/700 µS according to IEC61000-4-5.

4.4 Absolute Maximum Ratings

The PoE performance is not guaranteed when it exceeds the recommended rating. Exposure to any stress in the range between the recommended rating, as listed in the following table, and the absolute maximum rating mustbe limited to a short time. If these ratings are exceeded, then it may impact long-term operating reliability.

The following table lists the absolute maximum ratings of the PD69204T4 device.

Table 17 • Absolute Maximum Ratings

Parameters	Minimum	Maximum	Units
Supply Input Voltage (V_{MAIN})[1, 2]	–0.3	72	V
PORT_NEG[0.7] pins	–0.3	V_{MAIN} + 0.5	V
V_{AUX5}	–0.3	6	V
V_{AUX3P3}, DV_{DD}	–0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], PGD[3:0], RESET_N, TRIM	–0.3	DV_{DD} + 0.3 and < 4.0	V
Junction Temperature		150	°C
Lead Soldering Temperature (40 s, reflow)		260	°C
Storage Temperature	–65	150	°C

1. Power Sequence Requirement: V_{MAIN} > V_{AUX5} > V_{AUX3P3} = TRIM, DV_{DD}.
2. PD69204T4 EPAD is connected by copper plane on PCB to AGND. AGND is ground for IC.

Note: DRV_VAUX5 and IREF are output pins and must not apply voltage or current. DRV_VAUX5 can be left open when not used.

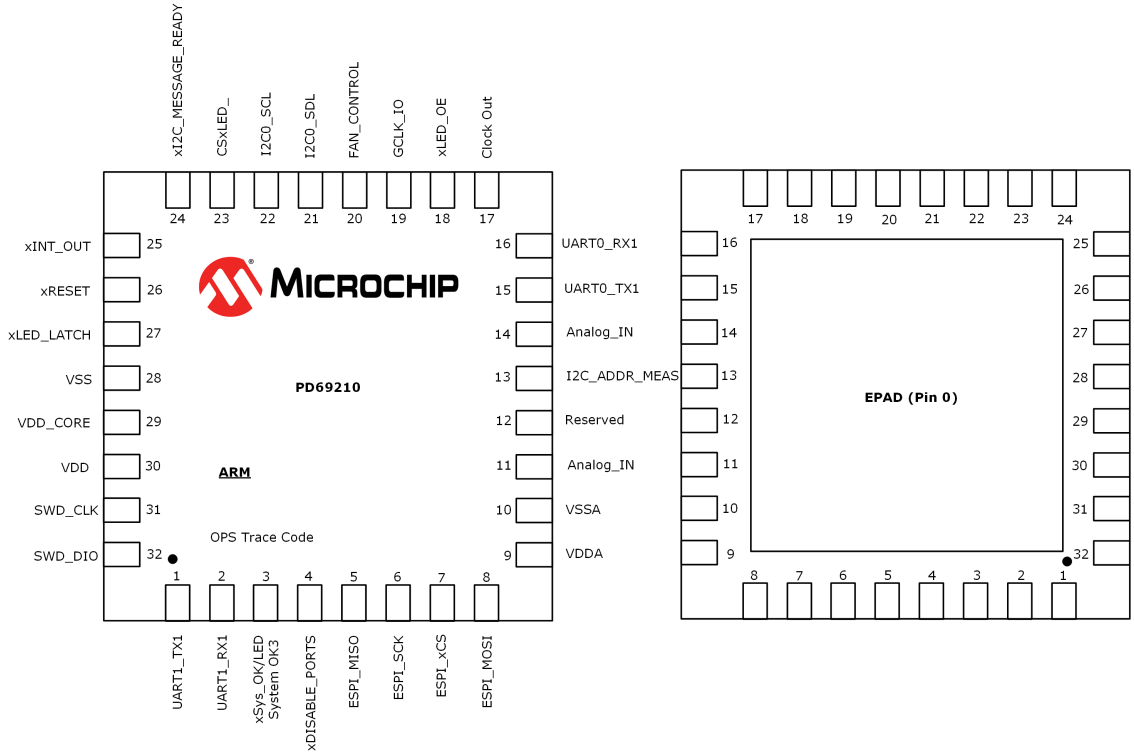
5 Pin Descriptions

This section describes the 32 pins of PD69210 device and 56 pins of PD69204T4 device.

5.1 Pin Configuration and Pinout

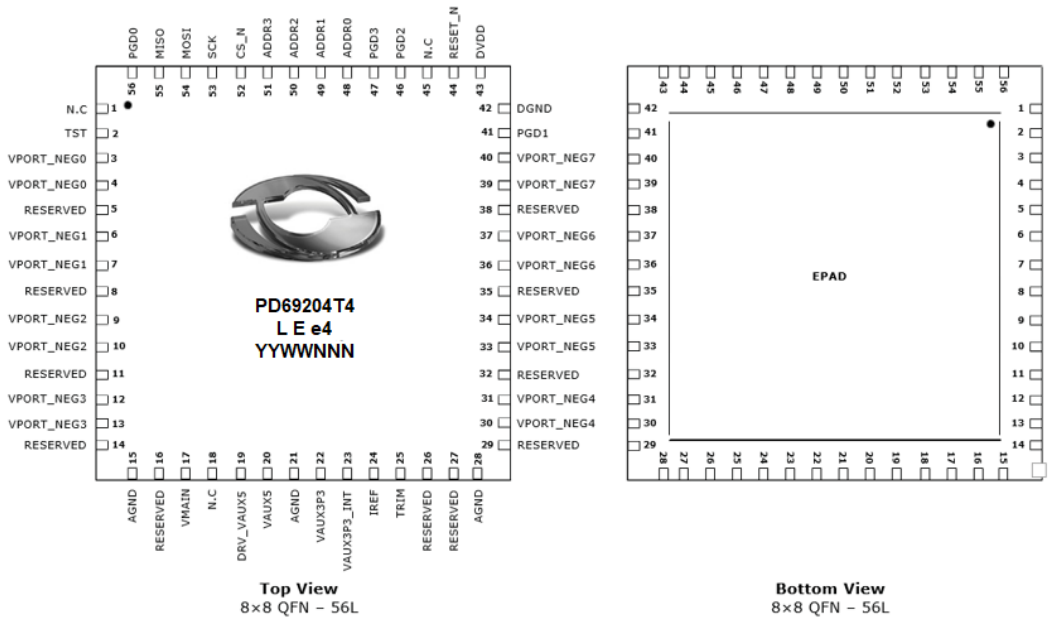
The following figures show the top and bottom view of PD69210 and PD69204T4 devices.

Figure 5 • PD69210 Pin Diagram



Note: For definitions about markings in the PD69210 pinout diagram, see Ordering Information (see page 44).

Figure 6 • PD69204T4 Pin Diagram



Note: For definitions about markings in the PD69204T4 pinout diagram, see Ordering Information (see page 44).

5.2 PD69210 Pin Descriptions

The following table lists the functional pin descriptions of the PD69210 device.

Table 18 • PD69210 Pin Descriptions

Number	Designation	Type	Description
1	UART1_TX[1]	OUT	Reserved UART leave floating.
2	UART1_RX[1]	IN	Reserved UART.
3	xSys_OK/LED System OK[3]	OUT	System validity indication. When the system is in OK state, the pin state is low. The behavior of this output is controlled by software mask register settings. The mask default settings is 0, which means that this pin indicates valid software, and V_{MAIN} is in range. This pin is active low. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
4	xDISABLE_PORTS[2]	IN	Disable all PoE ports. When this input is asserted low, the PD69210 device shuts down all of the PoE ports in the system. This pin contains a software filter of 480 ms to reject noise and false disable scenarios.
5	ESPI_MISO	IN	ESPI Bus to PoE Manager. SPI Master In Slave Out. SPI packets are received on this line.
6	ESPI_SCK	OUT	ESPI Bus to PoE Manager. SPI clock output to PD6920x, and LED stream clock output, set to 1 MHz.
7	ESPI_xCS	OUT	ESPI Bus to PoE Manager. SPI chip select (Active Low). CS is asserted during all SPI frame.
8	ESPI_MOSI	OUT	SPI packets are transmitted on this line.
9	VDDA	Supply	Main Supply 3.3 V.
10	VSSA	GND	Analog Ground.
11	Analog_IN	Analog_IN	Analog input. Should be connected to 3.3 V or GND through 10 k.
12	Reserved	IN	Leave open.
13	I2C_ADDR_MEAS	Analog_IN	I^2C address of PD69210. Analog input to determine I^2C address or UART operation. Consult AN240 Designing an IEEE 802.3af/802.3at /802.3bt- Compliant PD69208 48-Port PoE System (Document Number: PD-000359851) for details on setting I^2C address.
14	Analog_IN	Analog_IN	Reserved analog input. Connect to GND.
15	UART0_TX[1]	OUT	UART transmit to host. 15-byte protocol reply/telemetry is transmitted on this line. The baud rate is set to 19,200 bps. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
16	UART0_RX[1]	IN	UART receive from a host. 15-byte protocol commands are received on this line. The baud rate is set to 19,200 bps. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
17	Clock Out	Oscillator Clock	Clock out—reserved—leave open.

Number	Designation	Type	Description
18	xLED_OE[2]	OUT	The output enable signal for LED stream. This pin is active low.
19	GCLK_IO	DEBUG	Reserved—Leave Open—Debug output signal or debug clock output.
20	FAN_CONTROL	OUT	Optional. Fan control operates a fan when the PD69204T4 device temperature is above the temperature alarm threshold. This pin is active high.
21	I2C0_SDL[3]	IN/OUT	I²C bidirectional data. 15-byte protocol messages are transmitted on this line. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69210_UG_COMM_PROT).
22	I2C0_SCL[3]	IN/OUT	I²C clock from the host master. Speed is limited to 400 KHz and clock stretching functionality must be implemented in the host master. If PD69210 is busy, it holds the clock line.
23	xLED_CS[2]	OUT	Chip select signal for LED stream. This pin is active low.
24	xI2C_MESSAGE_READY[2]	OUT	I²C message ready for reading by the host. PD69210 asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I²C read cycle only when the message is ready. This pin is active low. After the host reads the data from PD69210, this pin is asserted to high.
25	xINT_OUT[2, 3]	OUT	Interrupt output indication. This line is asserted low when a pre-configured event is in progress. The host configures the event that must generate an interrupt through 15-bytes protocol. When this event occurs, the xINT_OUT pin is asserted. This pin is active low.
26	xRESET[2, 3]	IN/OUT	Host Reset input (Active Low). PD69210 can generate self-reset. In this case, the xRESET pin is driven low by the PD69210 for about 100 µS. It is recommended to connect this pin to a host open drain output with a 10 KΩ pull-up. A 47 nF filter capacitor must be connected between this pin to GND, close to the PD69210 device. If this pin is connected to a push/pull driver, a serial resistor of 1.5 KΩ must be connected instead of the pull-up.
27	xLED_LATCH[2]	OUT	Latch signal for LED stream. This pin is active low.
28	VSS	GND	Digital Ground.
29	V_{DD}_CORE	Power	1.2 V Core voltage connects 1 uF capacitor to GND.
30	V_{DD}	Supply	Main 3.3 V Supply.
31	SWD_CLK	DEBUG	Serial debug data bus clock. Use a 1K pull up to 3.3 V.
32	SWD_DIO	DEBUG	Serial debug data bus.
ePAD	ePad	GND	Connect to analog ground.

1. A weak pull-up is recommended. See PD69208_AN_240.
2. The initial x indicates that the pin is active low. Open drain output requires an external pull-up.
3. See the Hardware Application Note: PD69208_AN_240.

5.3 PD69204T4 Pin Descriptions

The following sections describe the functional pin descriptions of PD69204T4 device.

Table 19 • PD69204T4 Pin Descriptions

Number	Designator	Type	Description
	EPAD		Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible. See the PD69208 Layout Design Guidelines in the hardware application note (Catalog Number: PD69208_AN_240).
1	N.C.	N/A	Not connected. Do not connect externally (leave floating).
2	TST	Digital Input	Test pin for production use only. Keep connected to DGND.
3	VPORT_NEG0	Analog I/O	Negative port 0 output.
4	VPORT_NEG0	Analog I/O	Negative port 0 output.
5	RESERVED	N/A	Reserved pin. Do not connect externally.
6	VPORT_NEG1	Analog I/O	Negative port 1 output.
7	VPORT_NEG1	Analog I/O	Negative port 1 output.
8	RESERVED	N/A	Reserved pin. Do not connect externally.
9	VPORT_NEG2	Analog I/O	Negative port 2 output.
10	VPORT_NEG2	Analog I/O	Negative port 2 output.
11	RESERVED	N/A	Reserved pin. Do not connect externally.
12	VPORT_NEG3	Analog I/O	Negative port 3 output.
13	VPORT_NEG3	Analog I/O	Negative port 3 output.
14	RESERVED	N/A	Reserved pin. Do not connect externally.
15	AGND	Power	Analog ground.
16	RESERVED	N/A	Reserved pin. Do not connect externally.
17	V_{MAIN}	Power	Main High Voltage Supply voltage. A low ESR 1µF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
18	N.C	N/A	Not connected. Do not connect externally.
19	DRV_VAUX5	Power	Driven outputs for 5 V external regulation; if internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to Base. If an NPN is used, a 4.7 µF capacitor must be connected between this pin and AGND.
20	V_{AUX5}	Power	Regulated 5 V output voltage source; A 4.7 µF or higher filtering capacitor must be connected between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the emitter. The collector must be connected to V_{MAIN}.
21	AGND	Power	Analog ground.
22	V_{AUX3P3}	Power	Regulated 3.3 V output voltage source. A 4.7 µF or higher filtering capacitor must be connected between this pin and AGND. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.

23	VAUX3P3_INT	Power	Connected to V_{AUX3P3} (pin 22), if internal 3.3 V regulator is used. Leave unconnected (Floating), if external 3.3 V regulator is used.
24	IREF	Analog Input	Reference resistor pin. Connect a 28.7 kΩ 1% resistor to AGND. Use 0.1% resistor in BT/PoH applications.
25	TRIM	Test Input	Test Input pin; Keep connected to VAUX3P3.
26	RESERVED	N/A	Reserved pin. Do not connect externally.
27	RESERVED	N/A	Reserved pin. Do not connect externally.
28	AGND	Power	Analog ground.
29	RESERVED	N/A	Reserved pin. Do not connect externally.
30	RESERVED	N/A	Reserved pin. Do not connect externally.
31	RESERVED	N/A	Reserved pin. Do not connect externally.
32	RESERVED	N/A	Reserved pin. Do not connect externally.
33	RESERVED	N/A	Reserved pin. Do not connect externally.
34	RESERVED	N/A	Reserved pin. Do not connect externally.
35	RESERVED	N/A	Reserved pin. Do not connect externally.
36	RESERVED	N/A	Reserved pin. Do not connect externally.
37	RESERVED	N/A	Reserved pin. Do not connect externally.
38	RESERVED	N/A	Reserved pin. Do not connect externally.
39	RESERVED	N/A	Reserved pin. Do not connect externally.
40	RESERVED	N/A	Reserved pin. Do not connect externally.
41	PGD1	Digital I/O	Power good input from the system power supply.
42	DGND	Power	Digital ground.
43	DV_{DD}	Power In	Regulated 3.3 V for digital circuitry. Connect voltage from pin V_{AUX3P3} or from external power supply source if used. A 1 µF or higher filtering capacitor must be connected between this pin and DGND.
44	RESET_N	Digital Input	Reset input–active low (0 = reset). An external 10 K pull-up resistor should be connected between this pin and DVDD.
45	N.C.	N/A	Not connected. Do not connect externally.
46	PGD2	Digital Input	Power good input from the system power supply.
47	PGD3	Digital Input	Power good input from the system power supply.
48	ADDR0	Digital Input	SPI address bit 0 to set chip address.
49	ADDR1	Digital Input	SPI address bit 1 to set chip address.
50	ADDR2	Digital Input	SPI address bit 2 to set chip address.
51	ADDR3	Digital Input	SPI address bit 3 to set chip address.
52	CS_N	Digital Input	SPI bus, chip select.
53	SCK	Digital Input	SPI bus, serial clock Input.
54	MOSI	Digital Input	SPI bus, Master Data out/slave in.
55	MISO	Digital Output	SPI bus, Master Data in/slave out.
56	PGD0	Digital Input	Power good input from the system power supply.

5.4 Recommended PCB Layouts

This section describes the recommended PCB layouts of the PD69210 and the PD69204T4 devices.

5.4.1 PD69210 Recommended PCB Layout for 32 Pin QFN 5 mm x 5 mm

The following figures show the PCB layout pattern for PD69210. Units are in mm.

Figure 7 • Top-Layer Copper PCB Layout

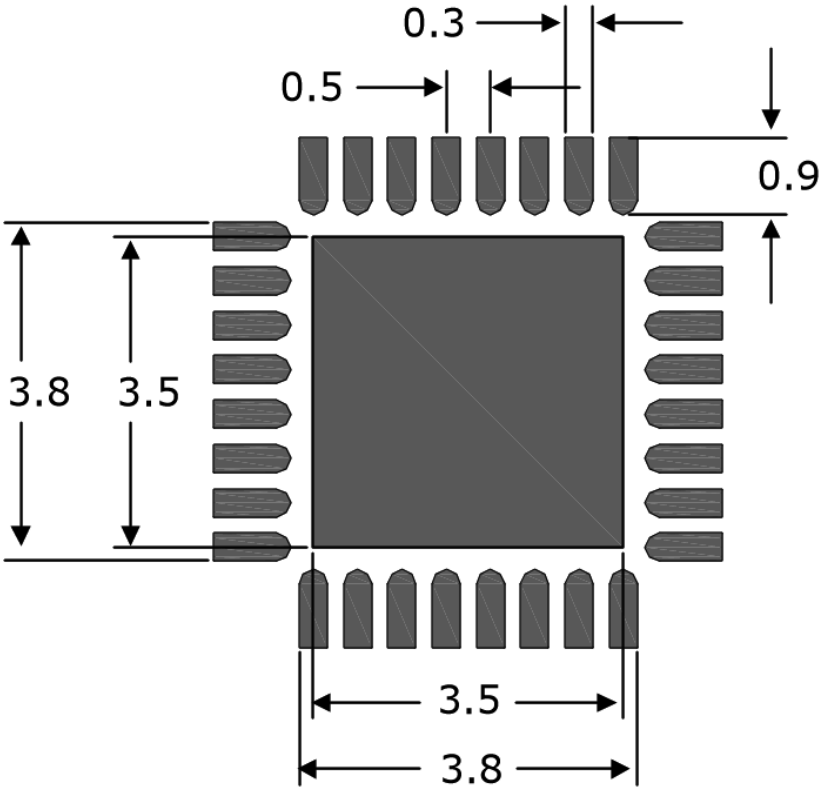
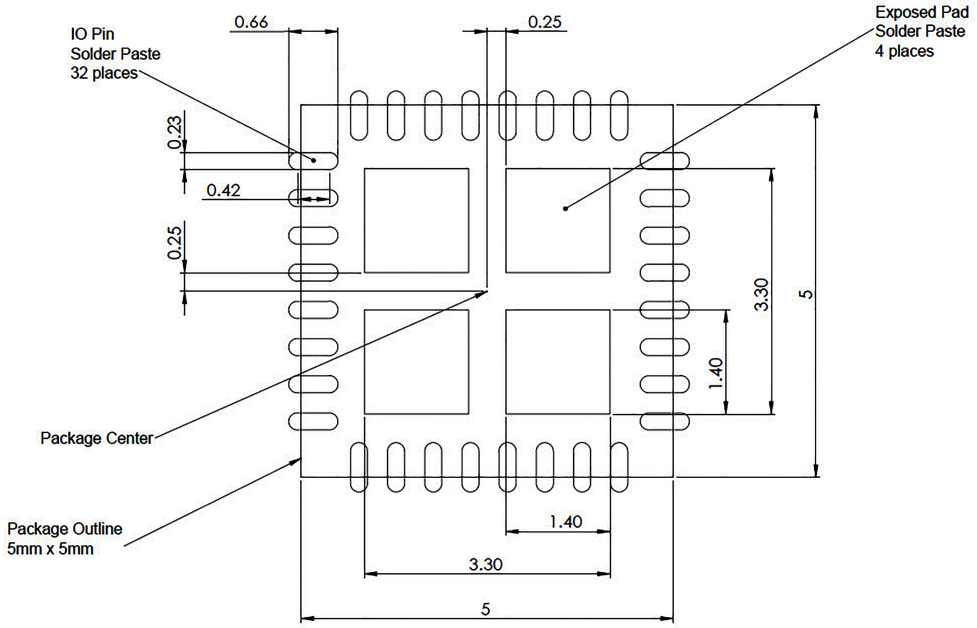


Figure 8 • Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array



5.4.2 PD69204T4 Recommended PCB Layout for 56-Pin QFN 8 mm x 8 mm

The following figures show the PCB layout pattern for PD69204T4. Units are in mm.

Figure 9 • Top-Copper Layer

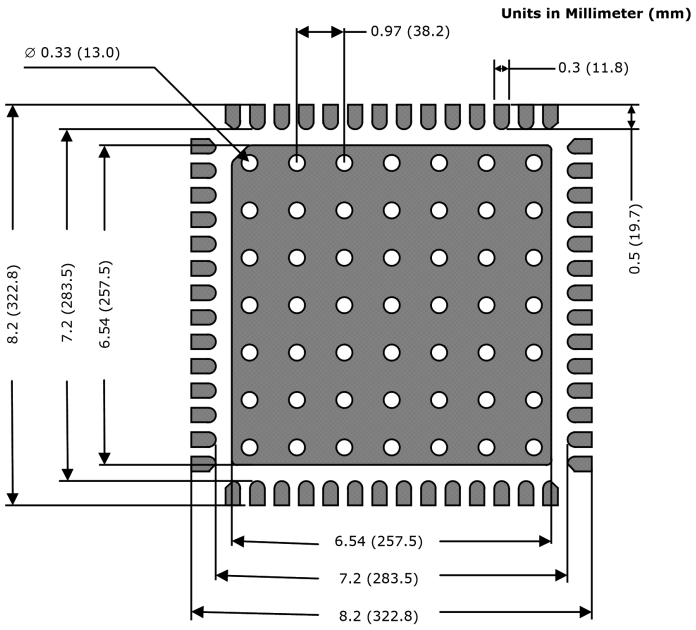


Figure 10 • Top-Solder Paste Layer

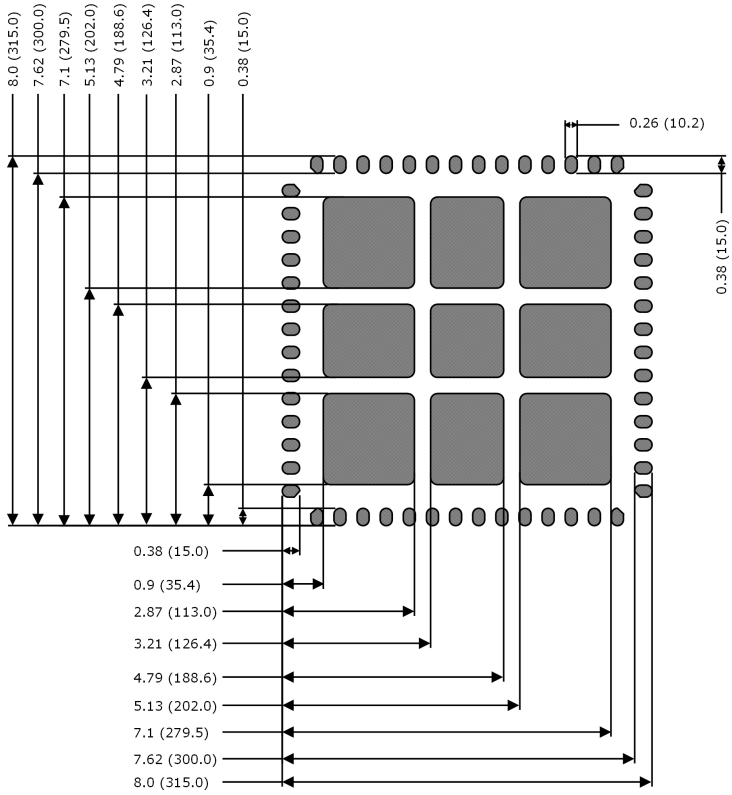


Figure 11 • Top-Layer Mask

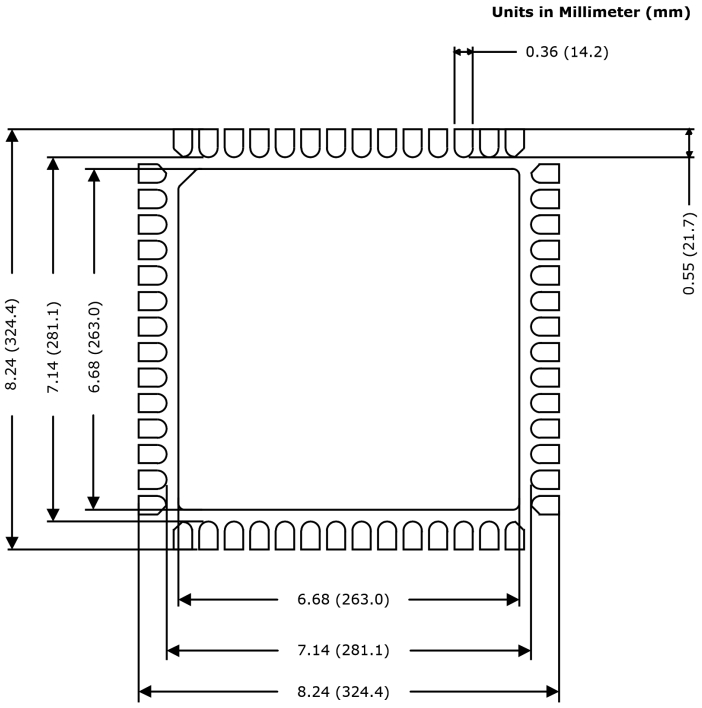


Figure 12 • BOT and Internal Layers Copper Plane

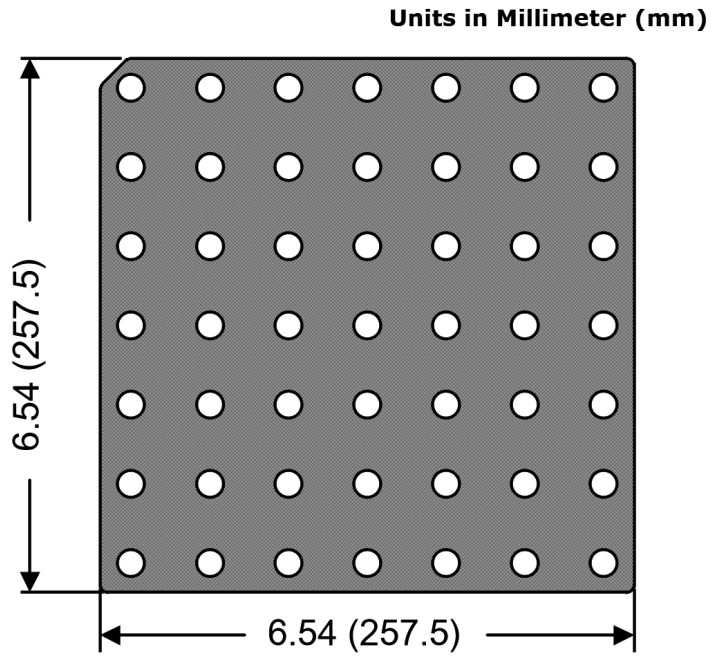
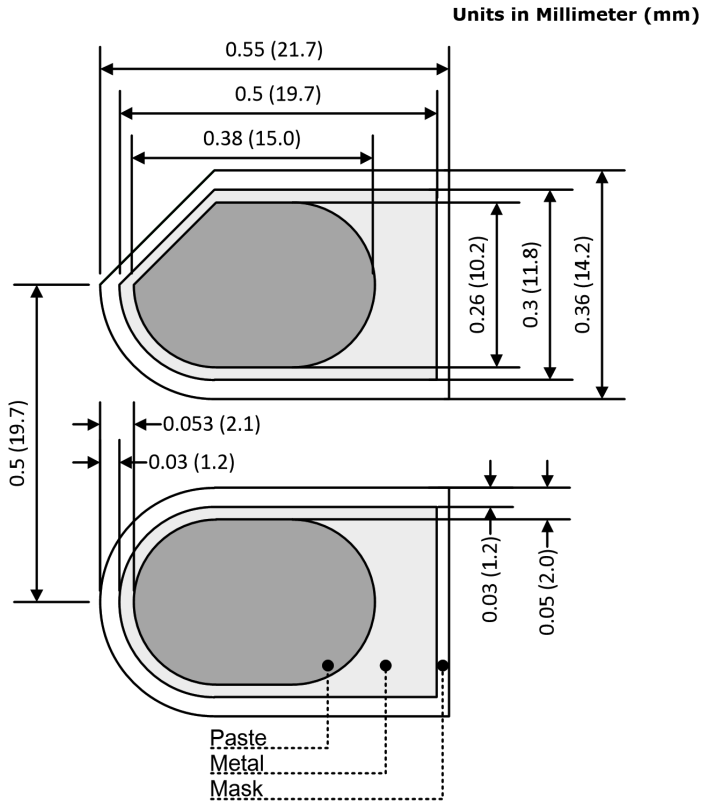


Figure 13 • Top-Layer Pin Geometry



Note: The CM has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad, and must not allow solder to be applied to the thermal vias under the QFN package, using an appropriate method. Any design should be subject to system validation and qualification, prior to commitment to mass production of field deployment. A 5 mm stencil is used.

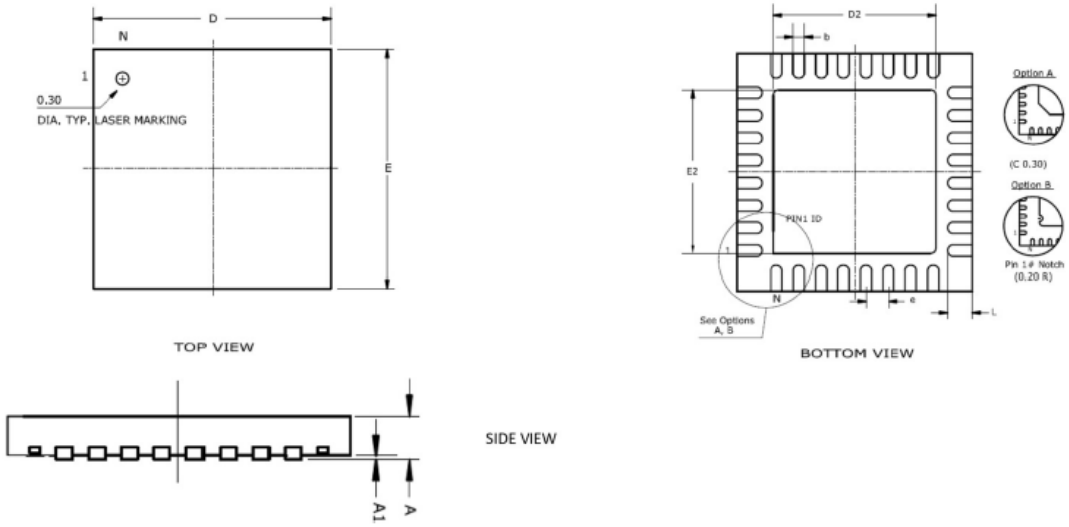
6 Package Information

This section describes package drawings of PD69210 and PD69204T4 devices.

6.1 PD69210 Package Outline Drawing

The following figure shows the package drawing of PD69210 device.

Figure 14 • PD69210 Package Outline Drawing (32 Pin QFN 5 mm x 5 mm)



The following table lists the dimensions and measurements of the PD69210 package.

Table 20 • PD69210 Package Outline Dimensions and Measurements

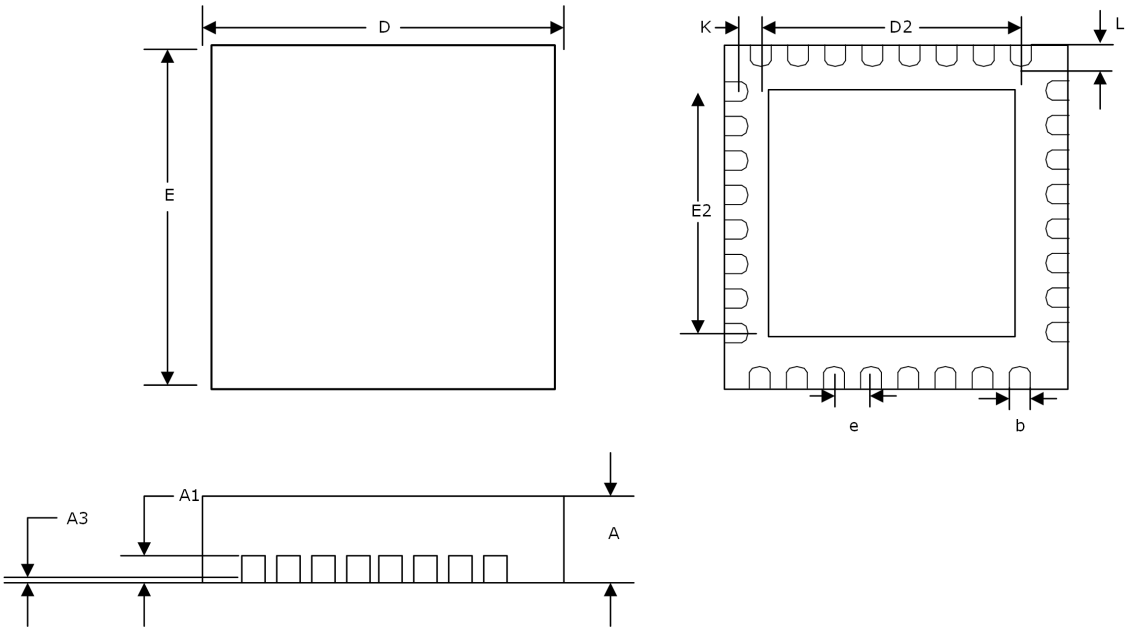
Dimension	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC		0.197 BSC	
E	5.00 BSC		0.197 BSC	

Note: Dimensions do not include protrusions. They must not exceed 0.155 mm (.006 in.) on any side. Lead dimension must not include solder coverage. Dimensions are in millimeters and inches for reference.

6.2 PD69204T4 Package Outline Drawing

The following figure shows the package drawing of the PD69204T4 package.

Figure 15 • Package Drawing (56 Pin QFN 8 mm x 8 mm)



The following table lists the dimensions and measurements of the PD69204T4 package.

Table 21 • PD69204T4 Package Outline Dimensions and Measurements

Dimension	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note: Dimensions do not include protrusions. They must not exceed 0.155 mm (0.006 in.) on any side. Lead dimension must not include solder coverage. Dimensions are in millimeters and inches for reference.

6.3 Thermal Specifications

The following tables list the thermal specifications of PD69204T4 and PD69210 devices.

Table 22 • PD69204T4 Thermal Specifications

Thermal Resistance	Typical	Units	Notes
θ_{JA}	40.9	°C/W	Junction-to-ambient thermal resistance.
θ_{JC}	15.2	°C/W	Junction-to-case thermal resistance with heat flow through package top.

Note: All parameters are as per JEDEC JESD-51.

Table 23 • PD69210 Thermal Specifications

Thermal Resistance	Typical	Units	Notes
θ_{JA}	19	°C/W	Junction-to-ambient thermal resistance.
Ψ_{JT}	0.05	°C/W	Junction-to-top thermal characterization parameter. A thermal metric derived from the difference in junction temperature (TJ) and package top temperature (TT) divided by total heating power (PH).
$\theta_{JC\ (top)}$	4.9	°C/W	Junction-to-case thermal resistance with heat flow through package top.
θ_{JB}	15.2	°C/W	Junction-to-board thermal resistance.

6.4 Recommended Solder Reflow Information

The following lists the recommended solder reflow information.

- RoHS 6/6
- Pb-free 100% matte tin finish
- Package peak temperature for solder reflow (40 seconds maximum exposure)–260 °C
- (0 °C, –5 °C)

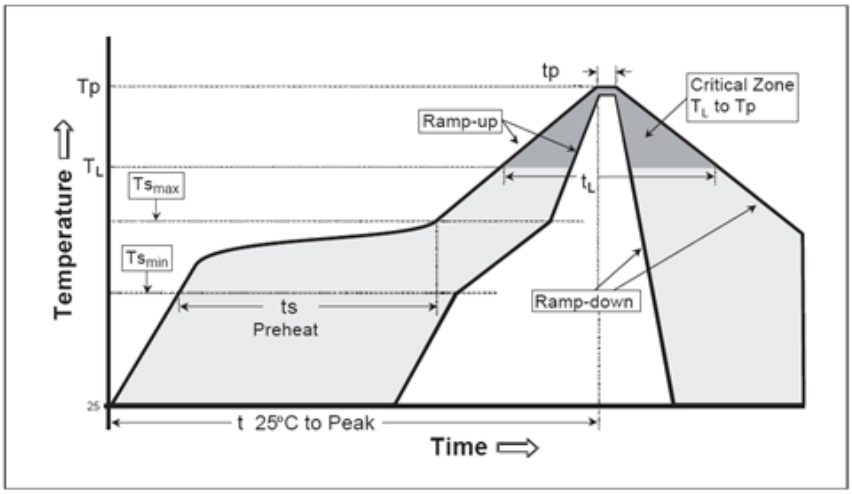
The following table lists the classification reflow profiles information.

Table 24 • Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TSmax to Tp)	3 °C/s maximum	3 °C/s maximum
Preheat		
Temperature min (TSmin)	100 °C	150 °C
Temperature max (TSmax)	150 °C	200 °C
Time (tsmin to tsmax)	60 s–120 s	60 s–180 s
Time Maintained		
Temperature (TL)	183 °C	217 °C
Time (tL)	60 s–150 s	60 s–150 s
Peak classification temperature (TP)	210 °C to 235 °C	240 °C to 255 °C
Time within 5 °C of actual peak temperature (tp)	10 s–30 s	20 s–40 s
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 min maximum	8 minutes maximum

The following figure shows the classification reflow profiles information.

Figure 16 • Classification Reflow Profiles



The following table lists the Pb-free process–package classification reflow temperatures.

Table 25 • Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume mm 3 < 350	Volume mm 3 350 – 2000	Volume mm 3 > 2000
Less than 1.6 mm[1]	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm–2.5 mm[1]	260 + 0 °C	250 + 0 °C	245 + 0 °C
Greater than or equal to 2.5 mm[1]	250 + 0 °C	245 + 0 °C	245 + 0 °C

1. Tolerance: The device manufacturer or supplier must assure process compatibility up to and including the stated classification temperature. This means that the peak reflow temperature is 0 °C. For example, 260 °C to 0 °C, at the rated MSL value.

Note: If the ratings mentioned in the preceding table exceed, then it may cause damage to the device.

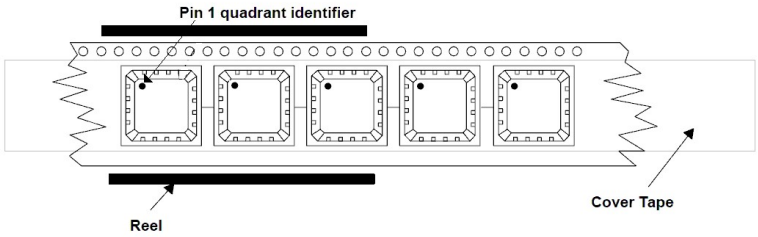
6.5 Tape and Reel Packaging Information

The following sections describe the tape and reel information of the PD69204T4 device.

6.5.1 PD69204T4 Tape and Reel Specification

The following figure shows the PD69204T4 tape and reel pin-1 orientation.

Figure 17 • Tape and Reel Pin-1 Orientation



Pin-1 Orientation of QFN Packages

The following figure shows the PD69204T4 tape specifications.

Figure 18 • Tape Specifications

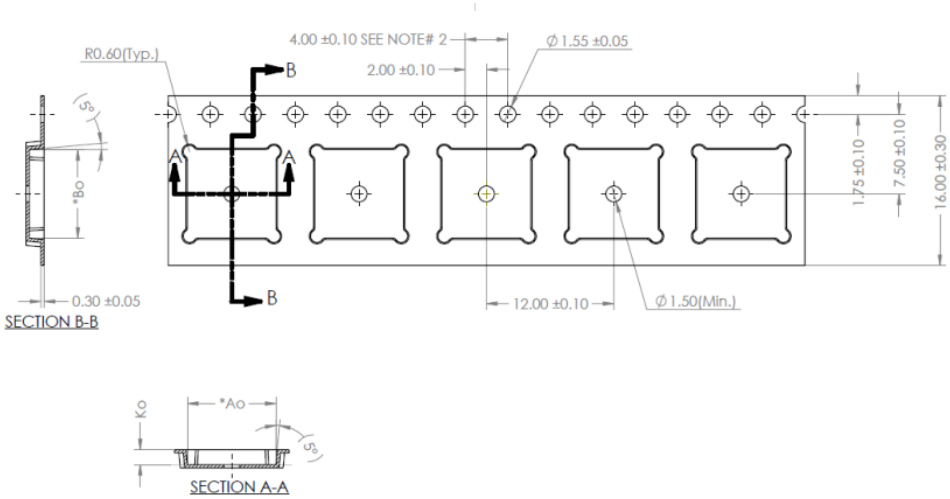
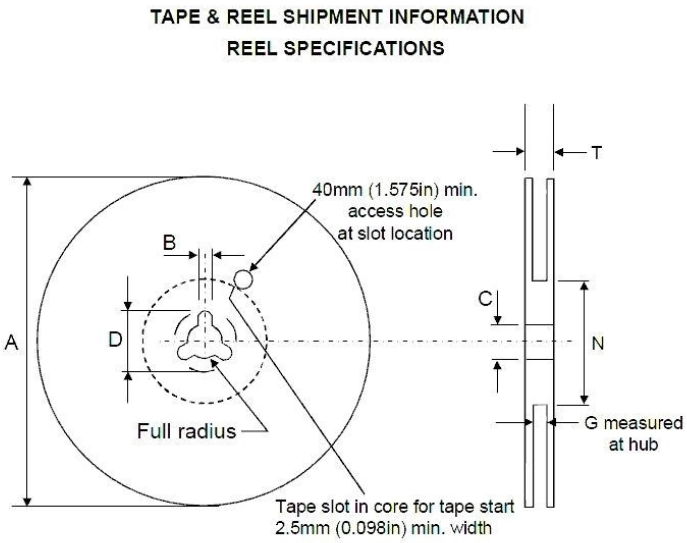


Table 26 • Tape Mechanical Data

Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10
Width	16.00 ±0.30

The following figure shows the PD69204T4 reel specifications.

Figure 19 • Reel Specifications



The following table lists the PD69204T4 reel mechanical data.

Table 27 • Reel Mechanical Data

Dimensions	Value (mm)	Value (inch)
Tape size	16.00 ±0.3	0.630 ±0.012
A maximum	330	13"
B maximum	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D minimum	20.2	0.795
N minimum	50	1.968
G	16.4 + 2.0/–0.0	0.645+ 0.079/–0.0
T maximum	29	1.142

Base Quantity = 2000 pieces

6.6 Reference Documents

- IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet
- PD69210_Serial Communication Protocol User Guide
- Microsemi_AN240 Designing an IEEE 802.3af/802.3at /802.3bt-Compliant PD69208 48-Port PoE System (Document Number: PD-000359851)
- Microsemi_TN218_PoE LED Stream Interface technical note
- Microsemi_Design for surge immunity within PSE systems
- Microsemi_TN230_ PoE_4_Pair_Behavior_PD6920x_PSE_Application_Note
- Microsemi_PD69208T4 and PD69210 datasheet (Document Number: PD000357193)

7 Application Information

The PD69204T4/PD69210 PSE Chipset performs IEEE802.3af (Type 1), IEEE802.3at (Type 2), Power over HDBaseT (POH), and IEEE802.3bt (Type 3 and 4) PSE functionalities in addition to the pre-standard and legacy (capacitor) detection. It includes additional protections such as short circuit and dV/dT protection upon startup.

Note: IEEE802.3bt functionality will be enabled by a firmware upgrade.

7.1 Connection Check

An additional PD construction detection phase, named connection check, is done to detect which PD configuration is connected (single-signature or dual-signature) per the IEEE802.3bt standard.

7.2 PD Detection

The PD detection feature detects a valid IEEE802.3af, IEEE802.3at, or IEEE802.3bt. The PD detection is done on the basis of the four different voltage levels generated over PD (the load), as illustrated in the following 4-pair PoE system diagram.

7.3 Legacy Detection

When legacy detection is enabled, the PD detection mechanism detects and powers up the legacy and pre-standard PDs as well as IEEE802.3af, IEEE802.3at and IEEE802.3bt standard compliant PDs (Classes 0–8).

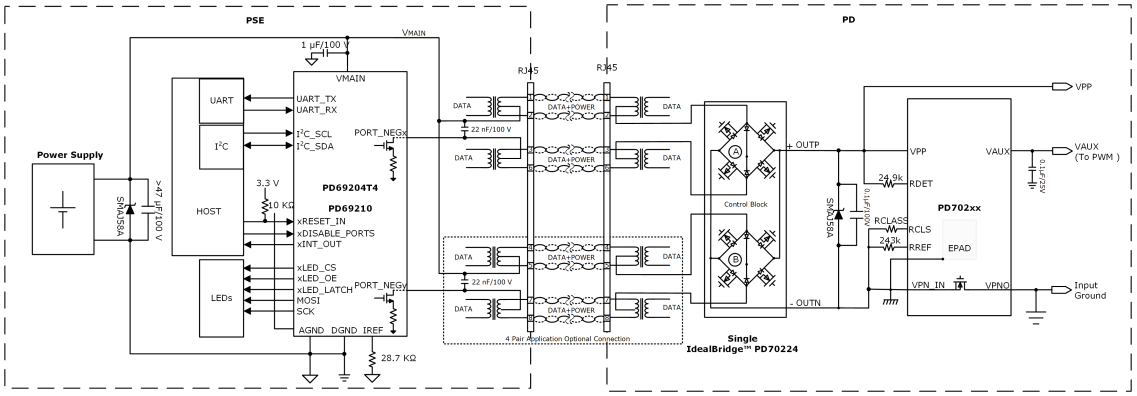
7.4 Classification

The classification process takes place immediately after PD detection is successfully completed. The goal of the classification process is to detect PD class as specified in IEEE802.3 standards.

In IEEE802.3af mode, the classification mechanism is based on a single voltage level (single event). In IEEE802.3at and IEEE802.3bt modes, the classification mechanism is based on two voltage levels (multiple events) as defined in IEEE802.3-2015 Clause 33 and IEEE802.3bt. In PoH mode, the classification mechanism is based on three events classification as defined in HDBaseT standard.

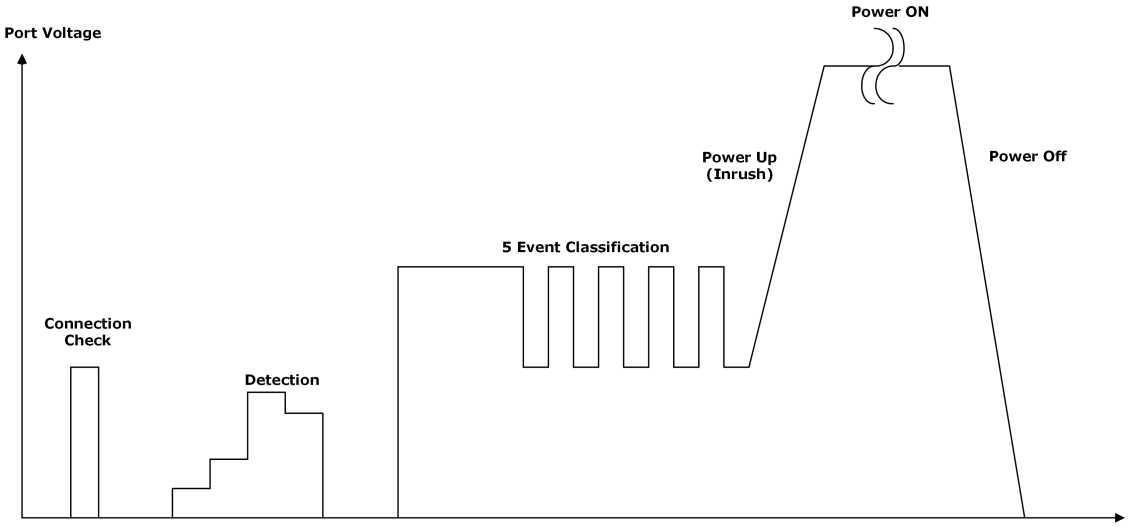
The following figure shows the 4-pair PoE system diagram.

Figure 20 • 4-Pair PoE System Diagram



The following figure shows the typical IEEE802.3bt port PoE voltage.

Figure 21 • Typical IEEE802.3bt Port PoE Voltage Diagram



7.5 Port Start-Up

Upon a successful detection and classification process, power is applied to the load through a controlled start-up mechanism.

During this period, inrush current is limited to 425 mA for a typical duration of 65 ms, which allows the PD load to charge and allows a steady state of power condition.

7.6 Over-Load Detection and Port Shut Down

After power-up, PD69204T4 automatically initializes its internal protection mechanisms. These mechanisms are used to monitor and disconnect power from the PD when extreme conditions occur, as specified in the IEEE802.3 standards. These conditions include over-current or short ports terminals scenarios.

7.7 Disconnect Detection

PD69204T4 supports the DC disconnect function as per IEEE802.3 standards. This mechanism continuously monitors load current and disconnects power according to IUDL, TMPDO, and TMPS parameters, as specified in PD69204T4 Port Real-Time Protection (see page 16).

7.8 IC Thermal Monitoring

PD69204T4 contains a thermal sensor that is sampled by the PD69210 for every 20 ms, so that the PD69204T4 die temperature is monitored at all times. To protect the PD69204T4 device from damage, the system ports are disconnected before damage can occur.

A temperature alarm threshold can be set by PD69210 controller to send interrupt indication by the xINT_OUT pin before ports are disconnected. The temperature can be read and monitored by the host as well if required.

7.9 Over-Temperature Protection

In addition to the die thermal sensor, there are thermal sensors on each MOSFET, that continuously monitors each port main MOSFETs junction temperature, and shut down the port load power when the temperature exceeds 200 °C.

7.10 VMAIN Out of Range Protection

The system automatically disconnects ports power when V_{MAIN} exceeds the pre-configured over-voltage and under-voltage thresholds.

7.11 2-Pair Ports and 4-Pair Ports

Operation modes include the following.

- POE Type 1/2 class 0–4 (up to 30 W)
- POE Type 3 class 0–4 2-pair and class 5–6 4-pair (up to 60 W)
- POE Type 4 class 7/8 4-pair (75 W/90 W)
- POH Mode: 4-pair (up to 95 W)

Note: For more information about 4-pair operation modes and power configuration, see Microsemi_PoE_4_Pair_Behavior_PD6920x_PSE_Application_Note_160159.

7.12 Power Management

The system supports the following three power management modes.

- Class (LLDP and CDP)
- Dynamic
- Static

7.13 Port Power Limit

Port power limit (PPL) is used to configure port power limit. When a port exceeds the power limit, it gets disconnected automatically.

7.14 Reset Pin

The xRESET pin is PD69210 digital host reset input (active low). The shortest pulse that is guaranteed to be recognized is 150 µs. PD69210 can generate self-reset. In this case, the xRESET pin is driven low by PD69210 for about 100 µs. It is recommended to connect this pin to a host open-drain output with a pull-up in a range of 4.7 KΩ to 10 KΩ. If this pin is connected to a push/pull driver, a serial resistor of 4.7 KΩ must be connected instead of a pull-up. Avoid resetting the PD69204T4 IC directly by the RESET_N pin. PD69210 controls the PD69204T4 ICs when the system reset is needed.

For more information about this pin connectivity, see the hardware application note (Catalog Number: PD69208_AN_240).

7.15 System OK Indication

Digital output pin to host is used as a system validity indication. When the system OK pin state is low, the behavior of this output is controlled by software mask register settings (Mask 0×28). The mask default settings is 0, meaning that this pin indicates valid software and Vmain is in range. This pin is active low.

For more information, see the Serial Communication Protocol User Guide document (Catalog Number: PD69210_UG_COMM_PROT).

7.16 Interrupt Pin

Interrupt out from PoE controller, indicating events such as port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events, see the Serial Communication Protocol User Guide document (Catalog Number: PD69210_UG_COMM_PROT). This pin is active low.

7.17 Port Matrix Control

Port matrix control enables layout designers to ascribe each physical port in the system to a logical port if required.

7.18 Power Good Interrupt

Interrupt from power supply directly to PD69204T4 manager. For systems comprising more than a single power supply, if one power supply fails, a port shutdown mechanism is executed to maintain operation and prevent the collapse of other power supplies.

When a function is used, PGD0, PGD1, PGD2, and PGD3 must be connected to the main power supplies status indication pin. Any change of at least 1 µs on these lines triggers a pre-defined disconnection matrix. This matrix is defined by PD69210 system power parameters. The port shutdown function reacts within 2 µs to any power good event.

7.19 LED Stream

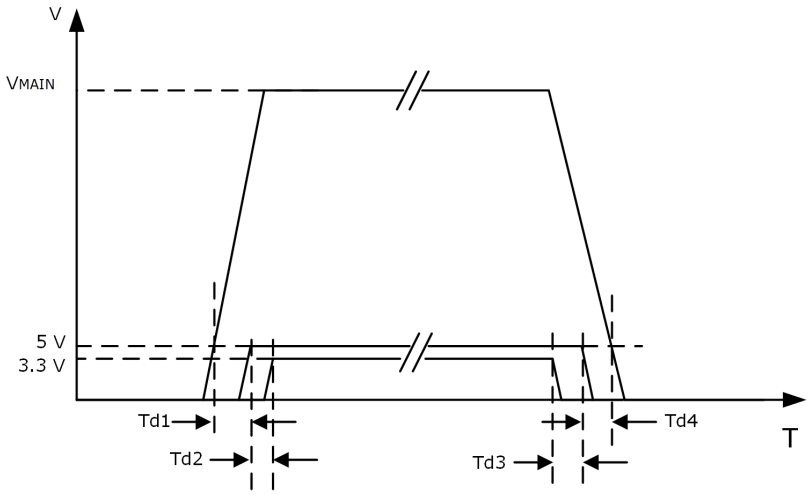
The direct SPI interface to an external LED stream circuitry that can drive LEDs directly without the host intervention. It enables designers to implement a simple LED circuit that does not require a software code. The LED stream clock frequency is 1 MHz.

For more information, see the TN-218.

7.20 Power Sequencing

The following figure shows the power sequencing.

Figure 22 • Power Sequencing



When using external V_{AUX5} or V_{AUX3P3}.

- Td1: V_{MAIN} at 5 V to V_{AUX5} > 0 µs
- Td2: V_{AUX5} to V_{AUX3P3} > 0 µs
- Td3: V_{AUX3P3} to V_{AUX5} > 0 µs
- Td4: V_{AUX5} to V_{MAIN} at 5 V > 0 µs
- $DV_{DD} = V_{AUX3P3}$

Note: See the Application Note AN240 Designing an IEEE 802.3af/802.3at /802.3bt-Compliant PD69208 48-Port PoE System (Document Number: PD-000359851). For proper operations, you need to ensure that

V_{MAIN} is always in the highest voltage connected to the IC. With an external DC-DC converter, the maximum 3.3 V slew rate is 100 ms.

7.21 Ground

The digital ground and the analog ground should be tied together on the board.

8 Ordering Information

The following table lists the part ordering information for PD69210 and PD69204T4 devices.

Table 28 • Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking[10]	Tray Marking[10]
PD69210D[1]-VVVV[2]SS[3]	Plastic QFN 5 mm × 5 mm (32 lead)	Tray	–40 °C to 85 °C	Microchip Logo PD69210 ARM logo YY[4]WW[5]NNN[6]	PD69210D- VVVVSS PD-OOOOG3bb[7] YYWW
PD69204T4ILQ-TR-LE	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	–40 °C to 85 °C	Microsemi Logo PD69204T4 L E e4[8] YYWWNNN[9]	

1. D stands for the detection method set as: C: Detection Method = IEEE802.3 and pre-standard; R: Detection Method = IEEE802.3.
2. VVVV is firmware revision.
3. SS stands for firmware parameters option.
4. Year code (last two digits of calendar year)
5. Week code (week of January; 1 is week 01)
6. Alphanumeric trace code
7. MKTG Product Type (Detection = R: Resistor/D = C: Resistor/Legacy)/Version/SW Parameters /Operation P/N.
8. L = FAB Code, E for V2R4, and e4 = second level interconnect.
9. YY = Year, WW = Week, and NNN = trace code
10. Final marking is subject to change up to product release to production.

The Firmware Release Note has the complete required information about how to specify the choice of VVVV and SS. Find the Firmware Release Notes in the Microchip Software Libraries, and register to My Microchip account to access the release notes.

Notes:

- The package meets RoHS, Pb-free, and MSL3 of the European Council to minimize the environmental impact of electrical equipment.
- Initial burning of controller's firmware is performed in the factory. Firmware upgrades can be performed by users using the communication interface.
  For more information, see TN-140 (Catalog Number:06-0024-081).

The following table lists the manufacturing and ordering part numbers of PD69204T4 devices.

Table 29 • PD69204T4 Manufacturing and Ordering Part Numbers

Ordering Part Number	Die Revision	Product Revision Code	Manufacturing Part Number
PD69204T4ILQ-TR-LE	V2R4	E	PD69204T4ILQ-TR-LE

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PD-000359832