ISL9122A

Ultra-Low I_Q Buck-Boost Regulator With Bypass

The ISL9122A is a highly integrated non-inverting buck-boost switching regulator that accepts input voltages both above or below the regulated output voltage. It features an extremely low quiescent current consumption of 1300nA in Regulation mode, 120nA in Forced Bypass mode, and 8nA in Shutdown mode. It provides 84% efficiency at 10µA load (V_{IN} = 3.6V, V_{OUT} = 3.3V) and has a peak efficiency greater than 97%. It supports input voltages from 1.8V to 5.5V.

The ISL9122A has automatic bypass functionality for situations in which the input voltage is close to the output voltage, and it automatically transitions between Buck and Boost modes without significant output disturbance. In addition to the automatic bypass functionality, the Forced Bypass power-saving mode can be chosen if voltage regulation is not required. Forced Bypass power saving mode is accessible using the I^2C interface bus.

The ISL9122A is capable of delivering up to 500mA of output current (V_{IN} = 3.6V, V_{OUT} = 3.3V) and provides excellent efficiency because of its adaptive frequency hysteretic control architecture.

The ISL9122A is designed for stand-alone applications and supports a default output voltage at Power-On Reset (POR). After POR, the output voltage can be adjusted in the range of 1.8V to 5.375V by using the I^2C interface bus. Specific default output voltages are available upon request.

The ISL9122A requires only a single EIA 0603 size inductor and two external capacitors. Power supply solution size is minimized by a 1.8mmx1.0mm WLCSP and is also available in a 3.0mmx2.0mm 8 Ld plastic DFN.

Features

- 1300nA quiescent current
- 84% efficiency at 10µA load
- 97% peak efficiency
- Input voltage range: 1.8V to 5.5V
- Output voltage range: 1.8V to 5.375V
- Output current: up to 500mA (V_{IN} = 3.6V, V_{OUT} = 3.3V)
- Selectable Forced and Auto Bypass power saving modes
- Seamless PWM/PFM and buck/boost transition
- I^2C Control and voltage adjustability
- Hysteretic controller
- Small 1.8mmx1.0mm WLCSP and 3.0mm x 2.0mm 8 Ld DFN packages

Applications

- Smart watches and wristband devices
- Wireless earphones
- Internet of Things (IoT) devices
- Water, gas, and oil meters
- Portable medical devices
- Hearing aid devices

Related Literature

For a full list of related documents, visit our website:

- ISL9122A product page

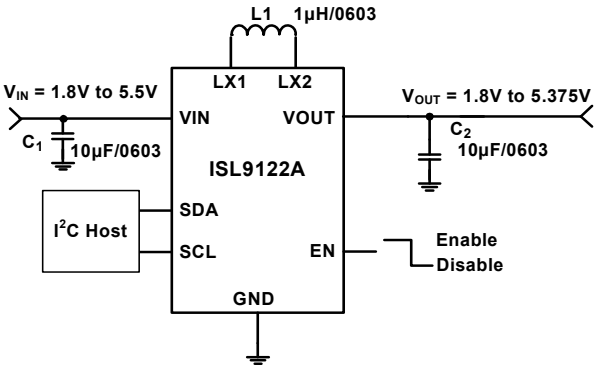


Figure 1. Typical Application

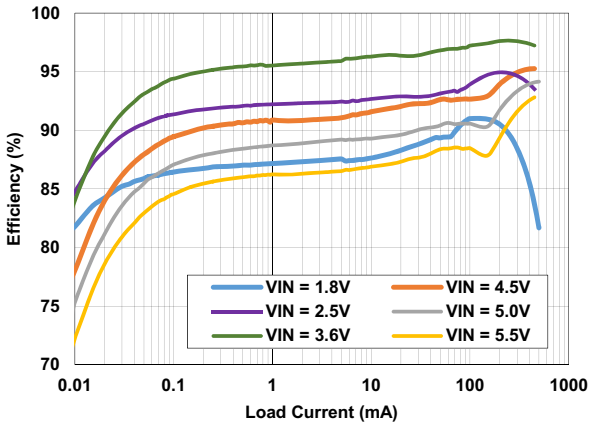


Figure 2. Efficiency: V_{OUT} = 3.3V, T_A = +25°C

Contents

1. Overview

1.1 Block Diagram

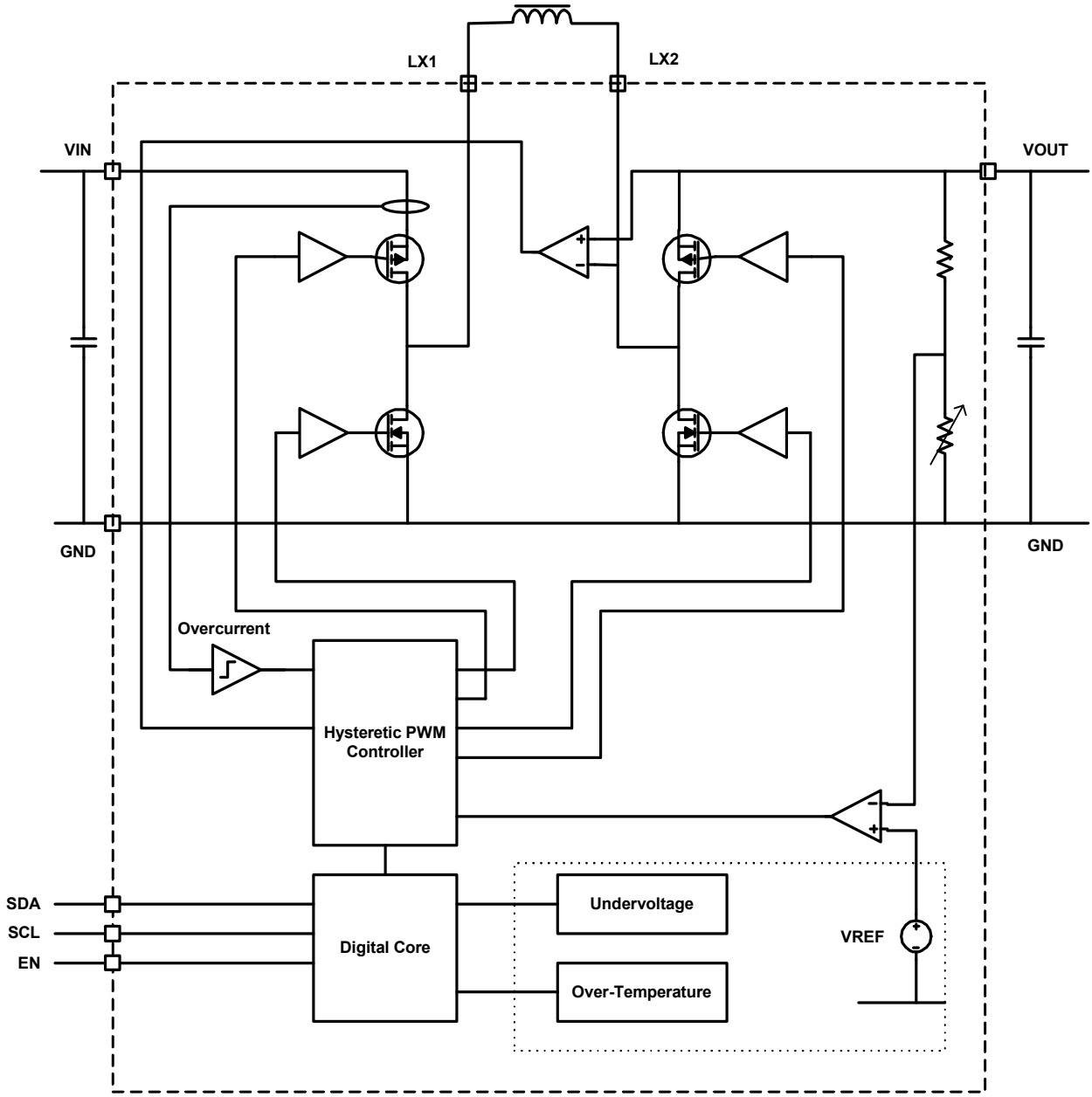


Figure 3. Block Diagram

1.2 Ordering Information

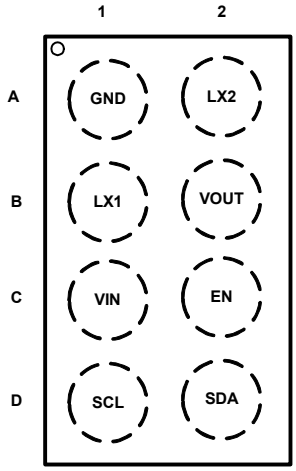
Part Number	Part Marking	Default V_{OUT} (V)	I^2C Address	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL9122AIINZ-T (Note 2)	122A	3.3V	0x18	-40 to +85	3k	8 Bump WLCSP	W2x4.8
ISL9122AIRNZ-T (Note 3)	A22	3.3V	0x18	-40 to +85	6k	8 Ld DFN	L8.2x3
ISL9122AIRNZ-T7A (Note 3)	A22	3.3V	0x18	-40 to +85	250	8 Ld DFN	L8.2x3
ISL9122AIIN-EVZ	Evaluation Board for ISL9122AIINZ						
ISL9122AIRN-EVZ	Evaluation Board for ISL9122AIRNZ						

Notes:

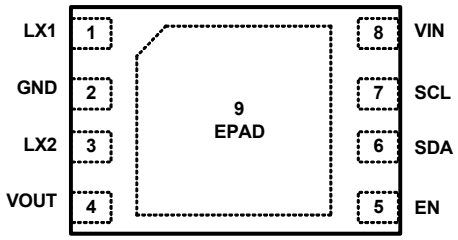
1. See TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL9122A device page. For more information on MSL, see TB363.

1.3 Pin Configurations

8 Bump WLCSP
Top View



8 Ld DFN
Top View



1.4 Pin Descriptions

WLCSP Pin #	DFN Pin #	Pin Names	Description
B2	4	VOUT	Buck-boost output.
A2	3	LX2	Inductor connection, output side.
A1	2	GND	Ground connection.
B1	1	LX1	Inductor connection, input side.
C1	8	VIN	Power supply input.
C2	5	EN	Logic input, drive HIGH to enable device. Do not leave floating.
D2	6	SDA	I^2C data input. Pull up to VIN if not being used. Do not leave floating.
D1	7	SCL	I^2C clock input. Pull up to VIN if not being used. Do not leave floating.
N/A	9	EPAD	Exposed Pad. Must be soldered to PCB GND.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN, VOUT	-0.3	6.5	V
LX1, LX2	-0.3	6.5	V
All Other Pins	-0.3	6.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
8 Bump WLCSP Package (Notes 1, 2)	110	-	28
8 Ld 2x3 DFN Package (Notes 1, 3)	72	21	-

Notes:
1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379
2. For θ_{JB}, the board temperature is taken on the board near the edge of the package, on a copper trace at the center of one side.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside. See TB379.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+125	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature (T_A) Range	-40	+85	°C
Supply Voltage (V_{IN}) Range	1.8	5.5	V
Load Current (I_{OUT}) Range (DC)	0	500	mA

2.4 Analog Specifications

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C.
Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise.

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Power Supply						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} Rising			**1.79**	V
Hysteresis				40		mV
V_{IN} Quiescent Current	I_Q	V_{IN} = 3.6V, I_{OUT} = 0A (Note 5)		1300	**1800**	nA

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C.
Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise. (Continued)

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
V_{IN} Supply Current, Shutdown	I_{SD}	V_{IN} = 3.6V, EN = GND		8	450	nA
V_{IN} Supply Current, Soft Shutdown	I_{SSD}	V_{IN} = 3.6V, shutdown using I^2C register. EN_AND = CONV_CFG[7] = 0		40	450	nA
V_{IN} Supply Current, Forced Bypass Mode	I_{BYP}	V_{IN} = 3.6V, I_{OUT} = 0A, averaged > 1ms		120	850	nA
Output Voltage Regulation						
Output Voltage Range	V_{OUT}	1.8V < V_{IN} < 5.5V, I_{OUT} = 1mA	**1.8**		**5.375**	V
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 0A, forced PWM	-2.5		+2.5	%
		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM	-3.6		+3.6	%
Soft-Start and Soft Discharge						
Time to Read OTP	t_{OTP}	Time from when V_{IN} > V_{UVLO} and EN signal asserts until switching starts		125		µs
V_{OUT} Ramp Rate for Soft-Start and During Dynamic Voltage Scaling (applicable only for V_{OUT} ramp-up, not ramp-down)	DVSRATE	Default at POR		3.125		mV/µs
		Programmable using I^2C after POR		6.25 0.78125 1.5625		mV/µs
V_{OUT} Soft Discharge ON-Resistance	r_{DISCHG}	EN < EN_{IL}		160		Ω
Power MOSFET (WLCSP Package)						
P-Channel MOSFET ON-Resistance (Buck)	r_{DSON_A}	V_{IN} = 3.6V, V_{OUT} = 3.6V		40		mΩ
N-Channel MOSFET ON-Resistance (Buck)	r_{DSON_B}			40		mΩ
P-Channel MOSFET ON-Resistance (Boost)	r_{DSON_D}			40		mΩ
N-Channel MOSFET ON-Resistance (Boost)	r_{DSON_C}			40		mΩ
Power MOSFET (DFN Package)						
P-Channel MOSFET ON-Resistance (Buck)	r_{DSON_A}	V_{IN} = 3.6V, V_{OUT} = 3.6V		50		mΩ
N-Channel MOSFET ON-Resistance (Buck)	r_{DSON_B}			50		mΩ
P-Channel MOSFET ON-Resistance (Boost)	r_{DSON_D}			50		mΩ
N-Channel MOSFET ON-Resistance (Boost)	r_{DSON_C}			50		mΩ
Bypass Mode						
Auto Bypass Thresholds	V_{IN_BYP}	Auto bypass thresholds - input voltage range. I_{OUT} = 10mA		±1% V_{OUT}		V
Inductor Peak Current Limit						
Peak Current Limit	I_{LIM}	2.5V < V_{IN} < 5.5V		2.5		A
		1.8V < V_{IN} < 2.5V		2.5		A
Efficiency						
Efficiency	η	I_{OUT} = 50mA, V_{IN} = 3.7V, V_{OUT} = 3.3V		97		%
		I_{OUT} = 10µA, V_{IN} = 3.7V, V_{OUT} = 3.3V		84		%

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C.
Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise. (Continued)

Parameter	Symbol	Test Conditions	Min (Note 4)	Typ	Max (Note 4)	Unit
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1mA, Forced PWM		2.5		MHz
Hiccup Mode						
Hiccup Time	t_{FLT_WAIT}	Time from shutdown to restart		100		ms
Thermal Protection						
Thermal Shutdown Threshold	T_{SD}	Rising Temperature		130		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			25		°C
Logic Levels						
Input Leakage	I_{LEAK}	EN pin		9	300	nA
		SCL pin		8	300	nA
		SDA pin		8	300	nA
EN Input HIGH Voltage	EN_{IH}	V_{IN} = 3.6V	**1.6**			V
EN Input LOW Voltage	EN_{IL}				**0.36**	V
SCL/SDA Input HIGH Voltage	SCL/SDA_{IH}		**1.45**			V
SCL/SDA Input LOW Voltage	SCL/SDA_{IL}				**0.36**	V

Notes:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Quiescent current measurements are taken when the device is not switching.

2.5 I^2C Interface Timing Specifications

Applicable to SCL and SDA in the Fast mode I^2C operation, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
I^2C Frequency Capability	f_{I2C}		0		400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{SP}	Any pulse narrower than the maximum specification is suppressed			50	ns
Data Valid Time	$t_{VD;DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window			900	ns
Data Valid Acknowledge Time	$t_{VD;ACK}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window, during acknowledgment			900	ns
Bus Free Time Between a STOP and START Condition	t_{BUF}	Time from SDA crossing SDA_{IH} at STOP to SDA crossing SDA_{IH} at the following START	1300			ns
SCL Low Time	t_{LOW}	Measured at the SCL_{IL} crossing	1300			ns
SCL High Time	t_{HIGH}	Measured at the SCL_{IH} crossing	600			ns
START Condition Set-Up Time	$t_{SU;STA}$	Time from SCL rising edge crossing SCL_{IH} to SDA falling edge crossing SDA_{IH}	600			ns
START Condition Hold Time	$t_{HD;STA}$	Time from SDA falling edge crossing SDA_{IL} to SCL falling edge crossing SCL_{IH}	600			ns
Data Set-Up Time	$t_{SU;DAT}$	Time from SDA exiting the SDA_{IL} to SDA_{IH} window to SCL rising edge crossing SCL_{IL}	100			ns
Data Hold Time	$t_{HD;DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA entering the SDA_{IL} to SDA_{IH} window	50			ns
STOP Condition Set-Up Time	$t_{SU;STO}$	Time from SCL rising edge crossing SCL_{IH} to SDA rising edge crossing SDA_{IL}	600			ns
SCL/SDA Capacitive Loading	C_b	Capacitive load for each bus line			400	pF

Note:
6. Limits established by design and are not production tested.

3. Typical Performance Curves

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L1 = 1µH, C1 = 10µF, C_2 = 10µF, T_A = +25°C, unless otherwise stated.

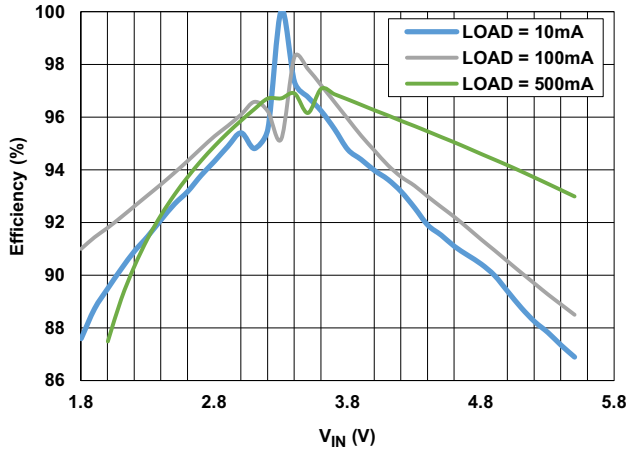


Figure 4. Efficiency vs Input Voltage: V_{OUT} = 3.3V, 1.0µH Coilcraft XEL4020, T_A = +25°C

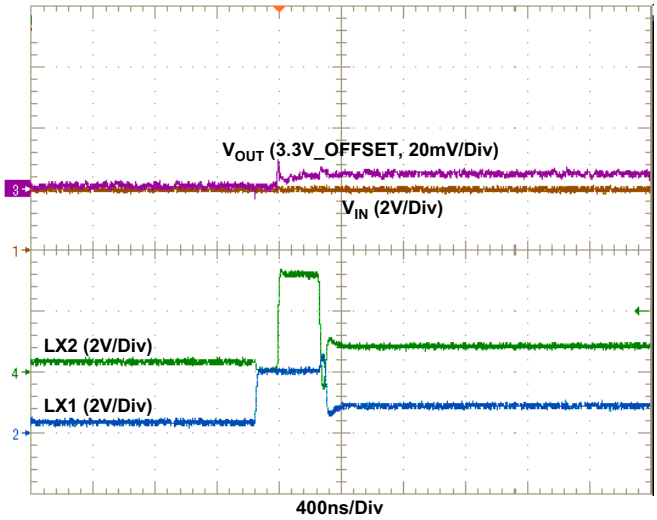


Figure 5. Steady-State Operation in PFM: V_{IN} = 2.0V, V_{OUT} = 3.3V, No Load

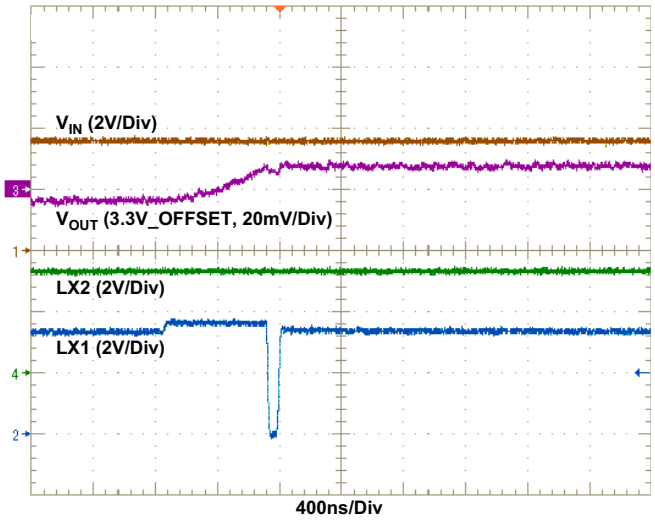


Figure 6. Steady-State Operation in PFM: V_{IN} = 3.6V, V_{OUT} = 3.3V, No Load

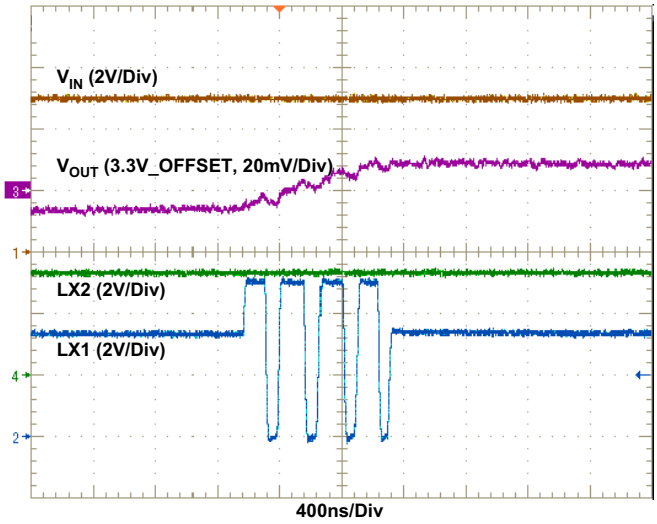


Figure 7. Steady-State Operation in PFM: V_{IN} = 5.0V, V_{OUT} = 3.3V, No Load

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L1 = 1µH, C1 = 10µF, C_2 = 10µF, T_A = +25°C, unless otherwise stated. **(Continued)**

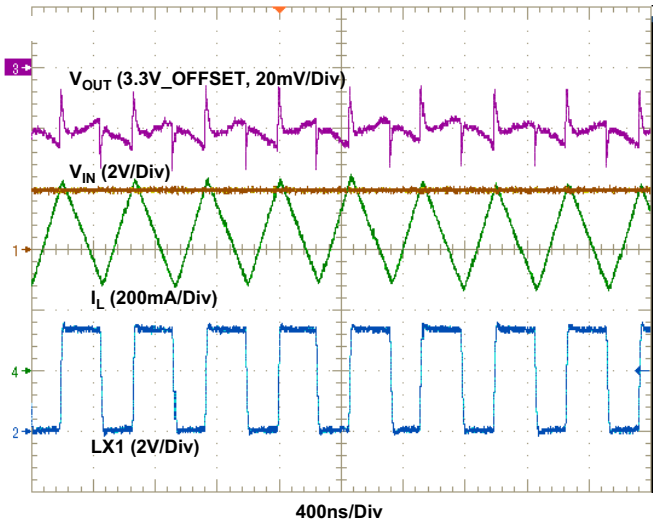


Figure 8. Steady-State Operation in PWM: V_{IN} = 2.0V, V_{OUT} = 3.3V, 200mA

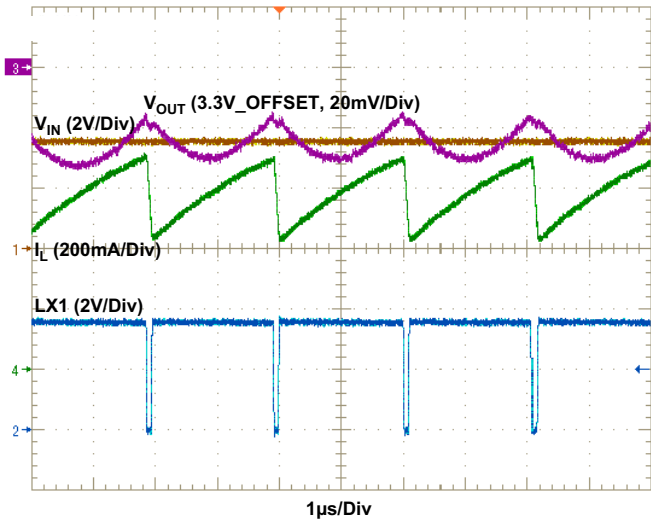


Figure 9. Steady-State Operation in PWM: V_{IN} = 3.6V, V_{OUT} = 3.3V, 500mA

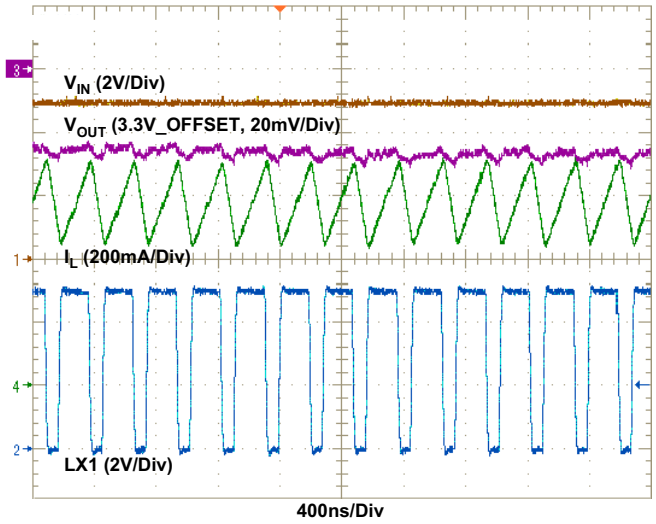


Figure 10. Steady-State Operation in PWM: V_{IN} = 5.0V, V_{OUT} = 3.3V, 500mA

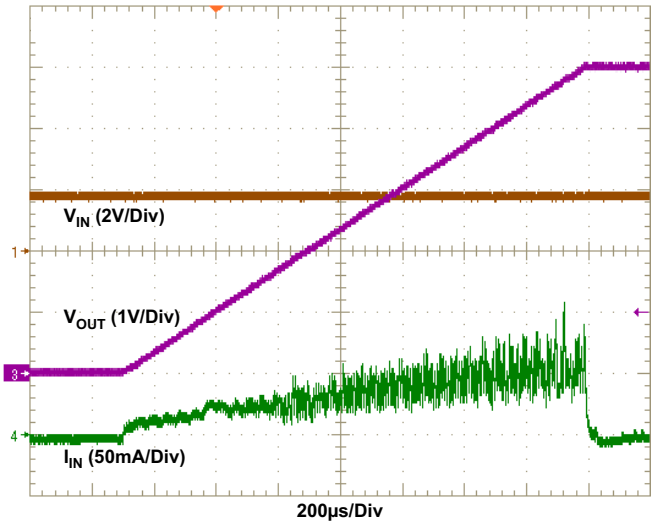


Figure 11. Soft-Start: V_{IN} = 1.8V, V_{SET} = 5.0V, No Load

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, I^2C pull-up voltage = V_{IN}, L1 = 1µH, C1 = 10µF, C_2 = 10µF, T_A = +25°C, unless otherwise stated. **(Continued)**

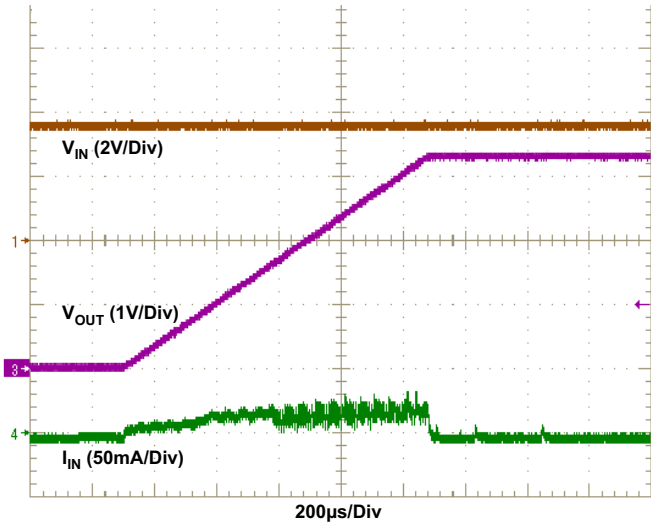


Figure 12. Soft-Start: V_{IN} = 3.6V, V_{SET} = 3.3V, No Load

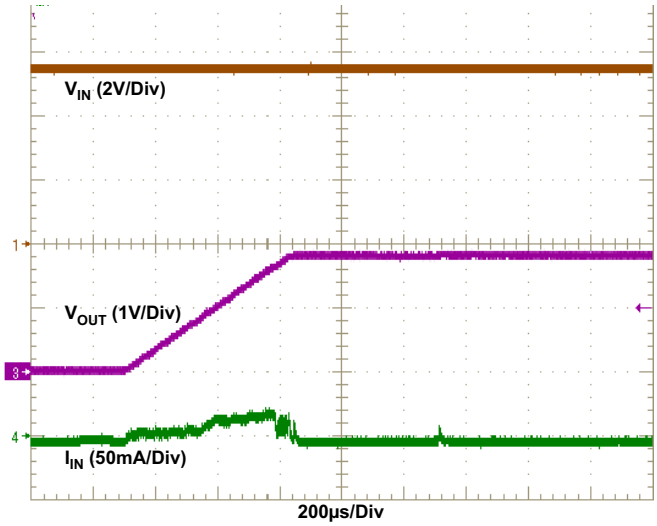


Figure 13. Soft-Start: V_{IN} = 5.5, V_{SET} = 1.8V, No Load

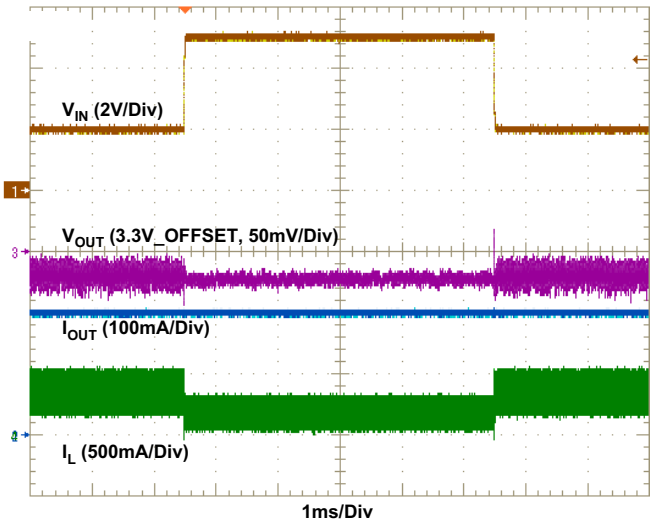


Figure 14. Line Transient: V_{IN} = 2.0V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 3.3V, Load = 200mA, Type II Error Amplifier

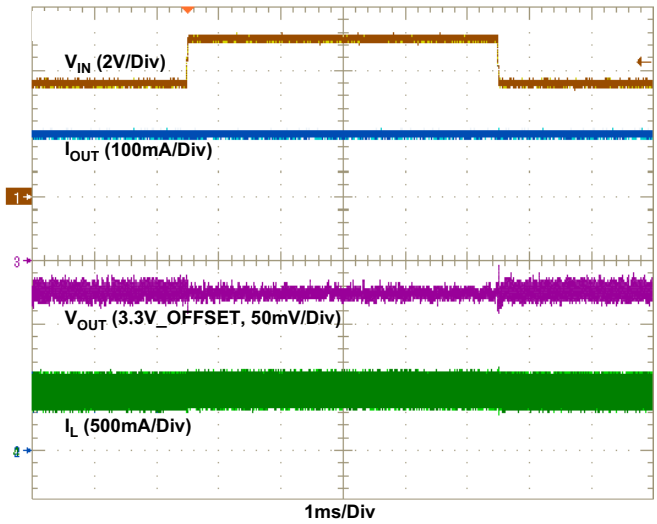


Figure 15. Line Transient: V_{IN} = 3.6V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 3.3V, Load = 500mA, Type II Error Amplifier

4. Functional Description

The ISL9122A implements a complete buck-boost switching regulator, with PWM controller, internal switches, references, protection circuitry, and control inputs. See the Block Diagram.

The PWM controller automatically switches between Buck and Boost modes as necessary, to maintain a steady output voltage with changing input voltages and dynamic external loads.

4.1 Enable Input

The device is enabled by asserting the EN pin HIGH. Driving EN LOW invokes Power-Down mode, in which most internal device functions are disabled. When the device is disabled by driving EN LOW, the output discharges naturally based on the load current.

4.2 Soft Discharge

An internal discharge resistor between VOUT and GND can be activated to slowly discharge the output capacitor. This internal discharge resistor has a typical resistance of 160Ω. The soft discharge function is accessed using I^2C while keeping the EN pin high. Using the CONV_CFG register, set the DISCH bit to 1 and disable the IC by setting the EN_AND bit to 0. (See Table 5 for details).

4.3 Start-Up

When the input voltage rises above the undervoltage lockout threshold and EN is asserted high, the power-on sequence starts. First, the IC is initialized and reads its OTP memory. After the OTP has been read and the controller knows the target output voltage and ramp rate, soft-start begins and the output voltage rises at the programmed ramp rate until it reaches the target output voltage.

4.4 Overcurrent/Short-Circuit Protection

The ISL9122A provides overcurrent protection by monitoring the inductor current. When the peak inductor current hits its current limit, the IC enters Hiccup mode, a Shutdown or Current Limit mode according to the setting of the OC_FAULT_MODE register. During Hiccup mode, the IC shuts down for 100ms and then tries to restart.

4.5 Thermal Shutdown

The ISL9122A features a thermal shutdown that protects the device from damage because of overheating. An integrated temperature sensor circuit monitors the internal IC temperature. When the temperature exceeds T_{SD}, the device stops switching; when the temperature falls by T_{SDHYS}, the controller goes through the soft-start phase before it starts regulating at the target output voltage as defined by the I^2C register value.

4.6 Buck-Boost Conversion Topology

The ISL9122A operates in either Buck or Boost mode. When operating in conditions in which V_{IN} is close to V_{OUT}, the ISL9122A alternates between Buck and Boost mode as necessary to provide a regulated output voltage.

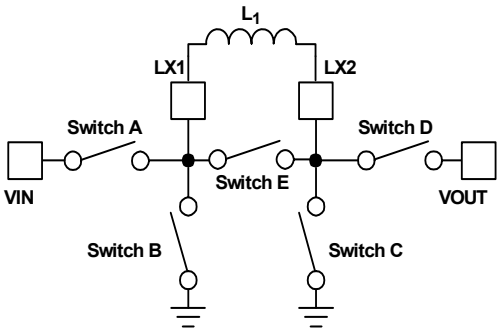


Figure 16. Buck-Boost Topology

Figure 4 shows a simplified diagram of the internal switches and external inductor.

4.7 PWM Operation

In Buck PWM mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

In Boost PWM mode, Switch A remains closed and switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

4.8 PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed, and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in Boost mode, the ISL9122A closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns off Switches A and C and next turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there are multiple PFM pulses to charge up the output capacitor, and the pulses continue until V_{OUT} achieves the upper threshold of the PFM hysteretic controller. Next, switching stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

4.9 Operation With V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL9122A makes smooth, rapid switches between Boost, Bypass, and Buck modes to maintain the regulated output voltage. This behavior provides excellent efficiency with a low output voltage ripple.

Note: For output voltages greater than 5.0V, the input voltage needs to be less than 4.5V to ensure low IQ operation.

4.10 Forced Operating Modes

Forced operating modes include Forced PWM mode and Forced Bypass mode. Forced operating modes are selected using the FMODE bits in the CONV_CFG register. (See Table 5 for details.)

The power-up default mode is normal operation with automatic mode transitions to optimize efficiency. Forced PWM mode can be selected to minimize frequency variation. Forced Bypass mode can be selected to minimize power losses when an output voltage regulation is not required.

When the device enters Bypass mode, both high-side FETs and the inductor bypass FET are turned ON, passing the input voltage to the output through the two high-side FETs and the inductor. In Bypass mode, all other blocks are turned off to minimize quiescent current consumption. When transitioning between Bypass mode and a voltage regulation mode, there should be a time delay of at least 1ms between entry into (or exit out of) Bypass mode. **Note**: There is no overcurrent protection in Bypass mode.

4.11 I^2C Serial Interface

The ISL9122A supports a bidirectional bus-oriented protocol. The protocol defines a transmitter as any device that sends data onto the bus and defines the receiver as the receiving device. The master is the device controlling the transfer, and the slave is the device being controlled. The master always initiates data transfers and provides the clock for both transmit and receive operations; therefore, the ISL9122A operates as a slave device in all applications.

The IC supports the following data transfers rates and modes as defined in the I^2C specification: up to 100kbit/s in Standard mode and up to 400kbit/s in Fast mode. All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

4.12 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 17). At power-up for the ISL9122A, the SDA pin is in input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL9122A continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 17). A START condition is ignored during the power-up sequence and when EN input is low.

All I^{2}C interface operations must be terminated by a STOP condition: a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 17). A STOP condition at the end of a write operation initiates the reconfiguration of the ISL9122A voltage feedback loop as necessary to provide the programmed output voltage.

An acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 18).

The ISL9122A responds with an ACK after recognizing a START condition followed by a valid 7-bit slave address, and the device responds with an ACK after a successful receipt of a register address byte. The ISL9122A again responds with an ACK after receiving a data byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

For the base version, the 7-bit slave address is set in trim to 0x18. The 7-bit address is followed by a Read/$\overline{\text{Write}}$ bit whose value is 1 for a Read operation, and 0 for a Write operation (see Table 1).

Table 1. 7-Bit Address Format

0	0	1	1	0	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

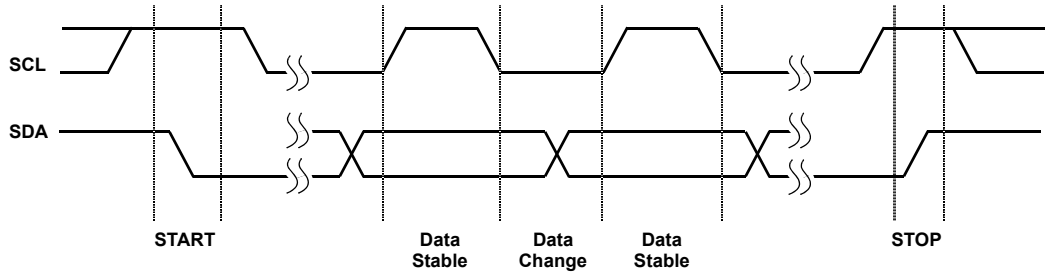


Figure 17. Valid Data Changes, Start, and Stop Conditions

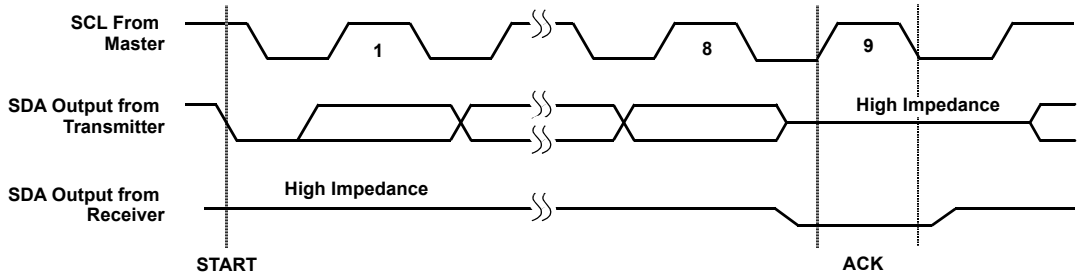


Figure 18. Acknowledge Response from Receiver

4.13 Write Operation

Write operations are shown in Figure 19. A write operation requires a START condition, followed by a valid 7-bit slave address with the R/$\overline{\text{W}}$ bit set to 0, and the write operation requires a valid register address byte, one or more data bytes, and a STOP condition. After each of the bytes, the ISL9122A responds with an ACK. After each data byte is ACK'd, the ISL9122A increments its register address to support block writes. The master sends a STOP to complete the command.

STOP conditions that terminate write operations must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte (or before one full

data byte + ACK is sent), the ISL9122A ignores the command and does not change the output voltage or other settings.

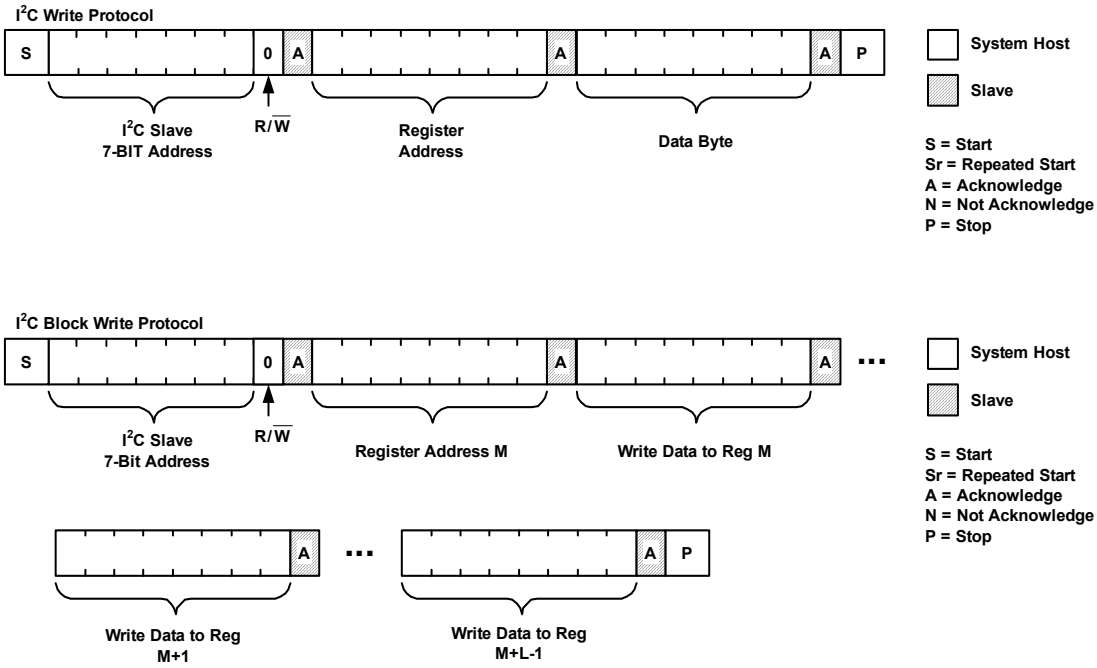


Figure 19. I²C Register Write Protocols

4.14 Read Operation

Read operations are shown in Figure 20. They consist of four or more bytes. The host generates a START condition and transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 0. The ISL9122A responds with an ACK. The host transmits the register address byte, and the ISL9122A responds with another ACK.

Next, the host generates a repeat START condition and transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 1. The ISL9122A responds with an ACK, indicating it is ready to provide the requested data.

The ISL9122A transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin. After each data byte is complete, the host generates an ACK condition, and the ISL9122A increments its register address to support block reads. After the last data byte is complete and ACK'd, the host sends a STOP condition. This completes the I²C Read operation.

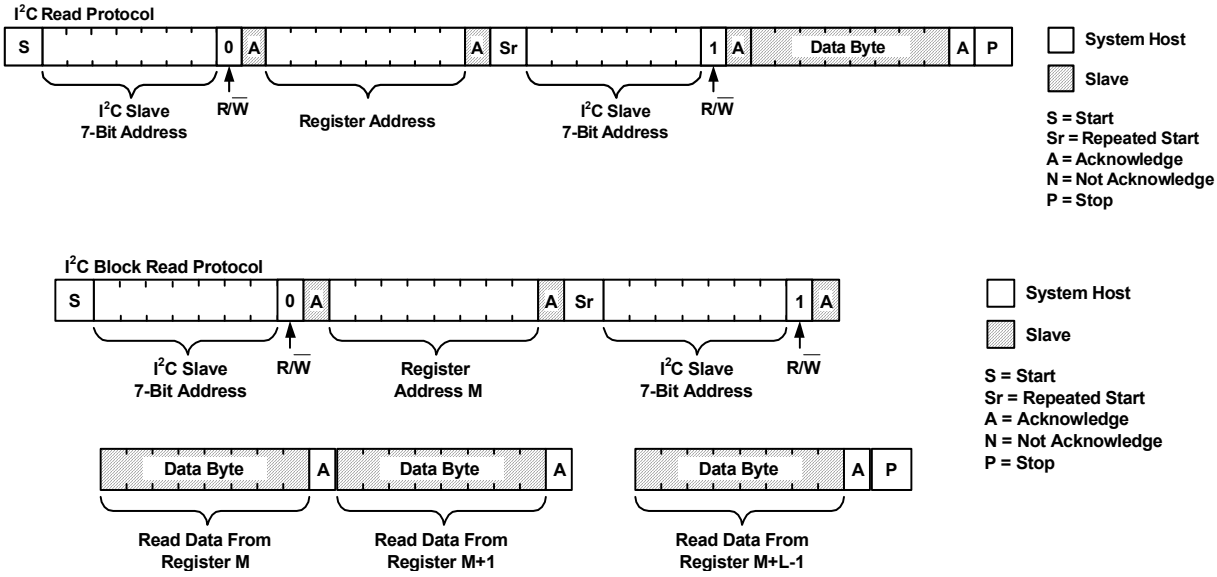


Figure 20. I²C Register Read Protocols

4.15 Register Descriptions

The ISL9122A has five I^2C accessible control registers whose functions are described in Table 2 through Table 6. These registers can be accessed any time the ISL9122A is enabled. When the ISL9122A is disabled (EN = Low), attempts to communicate with the ISL9122A through its I^2C interface are not supported.

4.15.1 RO_REG1

The RO_REG1 register contains the hardware identification bits as described in Table 2.

Table 2. Register Address 0x02: RO_REG1

Bit	Name	Type	Reset	Description
7:6	FAMILY_ID[1:0]	R	0x0	Chip family identifier 0x0 = ISL9122 stand-alone converter family
5:3	HW_REV[2:0]	R	0x3	Chip revision level 0x3 = Hardware revision D
2:0	RAIL_VAR[2:0]	R	0x0	Converter variant identifier 0x0 = High voltage input Buck-Boost (ISL9122A)

4.15.2 INTFLG_REG

The INTFLG_REG register contains fault flags. Each bit represents a different type of fault as described in Table 3. A 0 indicates no fault, and a 1 indicates a fault. Each bit is set by a fault event and is cleared when read.

Table 3. Register Address 0x03: INTFLG_REG

Bit	Name	Type	Reset	Description
3	INT3	R	0x0	Voltage setting under range
2	INT2	R	0x0	Voltage setting over range
1	INT1	R	0x0	Over-temperature
0	INT0	R	0x0	Overcurrent

4.15.3 VSET

The VSET register contains the output voltage setting in 25mV steps as shown in Equation 1. The VSET can be changed after the IC is enabled and operating. When the output voltage is changed, it ramps at the rate set in the DVSRATE bits of CONV_CFG register.

The output voltage range is digitally limited to be between the minimum and maximum values shown in Table 4. Setting values above or below the limits results in the output voltage ramping to the limit and the appropriate overvoltage or undervoltage interrupt flag in INTFLG_REG being set.

(EQ. 1) $$V_{OUT} = VSET \times 0.025V$$

Table 4. Register Address 0x11: VSET

Bit	Name	Type	Reset	Description
7:0	VSET[7:0]	R/W		Output voltage setting Minimum limit = 1.8V Maximum limit = 5.375V

4.15.4 CONV_CFG

The CONV_CFG register settings are described in Table 5.

Table 5. Register Address 0x12: CONV_CFG

Bit	Name	Type	Reset	Description
7	EN_AND	R/W	0x1	Enable bit. ANDed with the enable input 0x0 = EN pin going high wakes up the I^2C, but does not start the converter. The converter is started by writing 1 to this bit using I^2C while the EN pin is high 0x1 = EN pin going high wakes up the I^2C and starts the converter **Note**: EN pin low always disables converter and I^2C
6	DISCH	R/W	0x0	0x0 = No discharge resistor present when converter is disabled over I^2C 0x1 = Discharge resistor present when converter is disabled over I^2C
5:4	DVSRATE[1:0]	R/W	0x0	Dynamic Voltage Scaling slew rate applied when the output voltage setting is changed. 0x0 = 3.125mV/µs 0x1 = 6.25mV/µs 0x2 = 0.78125mV/µs 0x3 = 1.5625mV/µs
3:2	FMODE[1:0]	R/W	0x0	Forced operating modes 0x0 = Normal operation with automatic mode transitions 0x1 = RESERVED. DO NOT USE this combination 0x2 = Forced PWM mode with no PFM operation 0x3 = Forced bypass. Disables switching. If the Forced Bypass mode is selected and the part is disabled over I^2C (CONV_CFG[7] = EN_AND = 0x0), the converter remains in Forced Bypass
1	CONV_RSVD	R/W	0x0	Reserved
0	TYPE1	R/W	0x1	0x0 = Type I error amplifier for best transient response with voltage positioning 0x1 = Type II error amplifier for best steady state voltage accuracy. **DO NOT USE** Type II error amplifier if overcurrent fault handling is disabled (INTFLG_MASK[7] = OC_FAULT_MODE = 0x2 or 0x3)

4.15.5 INTFLG_MASK

The INTFLG_MASK register settings are described in Table 6.

Table 6. Register Address 0x13: INTFLG_MASK

Bit	Name	Type	Reset	Description
7:6	OC_FAULT_MODE[1:0]	R/W	0x0	Overcurrent fault handling modes 0x0 = Hiccup mode with 100ms wait 0x1 = Shutdown mode. Requires restart over I^2C or EN pin 0x2 = Current limit with no fault action taken. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0) 0x3 = Reserved. USE ONLY with Type I error amplifier (CONV_CFG[0] = TYPE1 = 0x0)
5	EN_OR	R/W	0x0	Enable override bit for I^2C control of converter. Implements push-button ON operation; the button pulls EN high and the part starts. If EN_OR is set from OTP or over I^2C, the part remains enabled when the button is released 0x0 = Controlled by the EN pin 0x1 = Held in enable state - EN pin is ignored

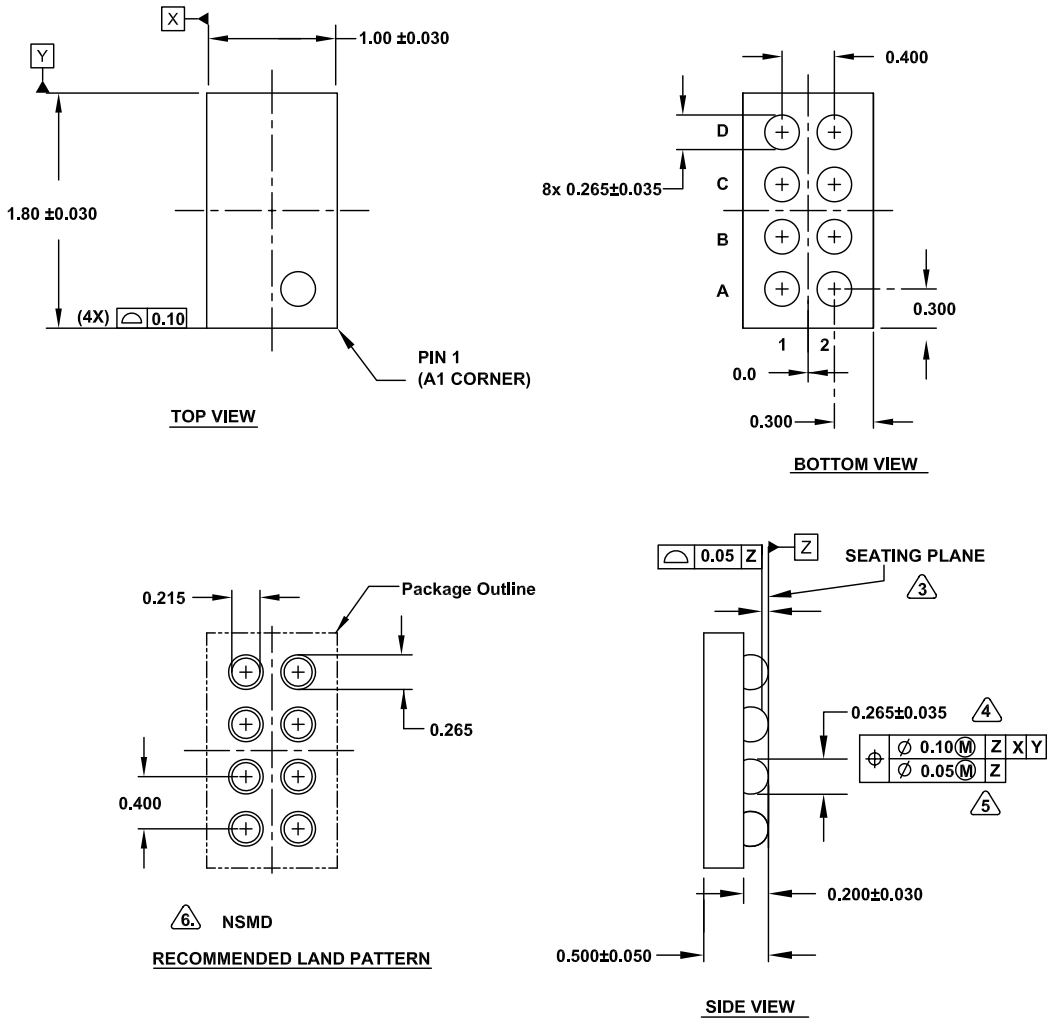
5. Revision History

Rev.	Date	Description
1.00	Sep.14.20	Initial release

6. Package Outline Drawings

For the most recent package outline drawing, see W2x4.8.

W2x4.8
8 Ball Wafer Level Chip Scale Package (WLCSP) 0.4mm Pitch
Rev 0, 6/17

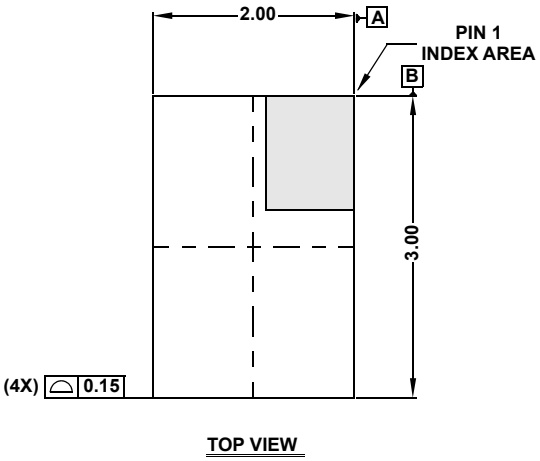


NOTES:

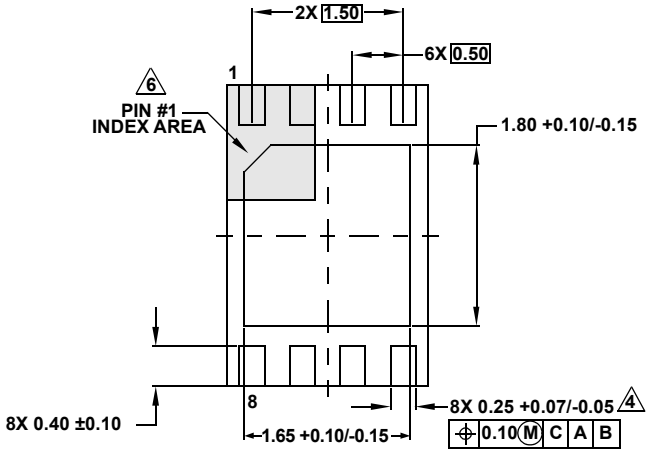
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASMEY 14.5-1994
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per Intersil Techbrief. http://www.intersil.com/data/tb/tb451.pdf

L8.2x3
8 Lead Dual Flat No-Lead Plastic Package
Rev 2, 3/15

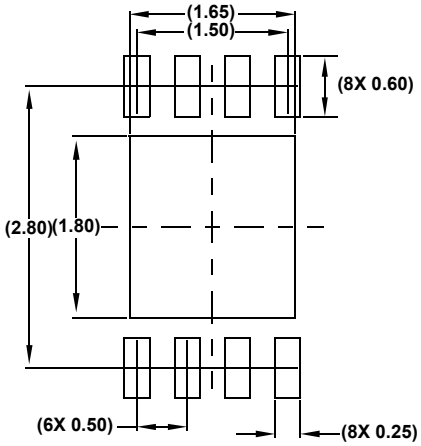
For the most recent package outline drawing, see L8.2x3.



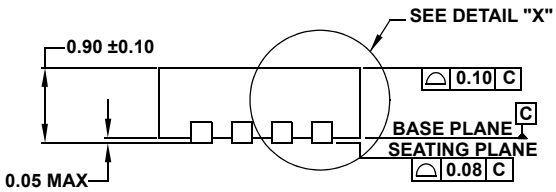
TOP VIEW



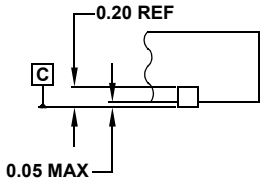
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Complies to JEDEC MO-229 VCED-2.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.