

# **UWB Module Data Sheet**

**NXP SR150 Chipset**


**Design Name: Type2BP**  
**P/N : LBUA0VG2BP-741**

## Revision History

Revision Code	Date	Description	Comments
-	2023.10.10	First Issue	

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 Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

## 1. Scope

This specification is applied to the NXP SR150 UWB module

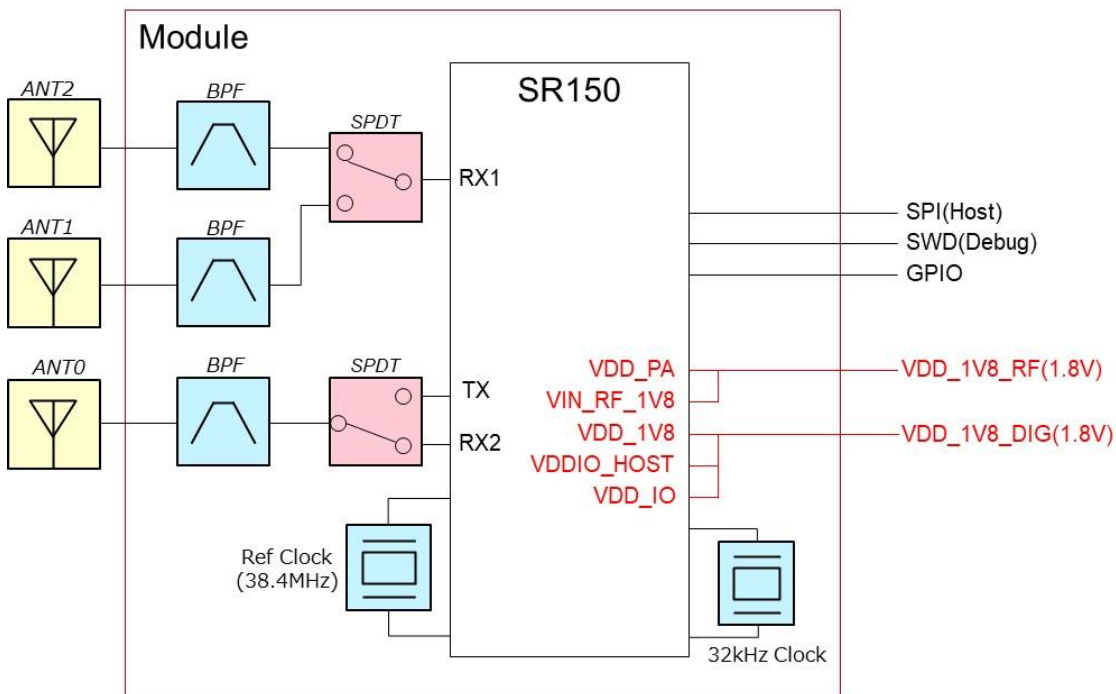
## 2. Key Features

- Main IC : NXP / SR150
- Compliant with IEEE802.15.4z HRP PHY
- Supports SHF UWB bands, Ch5 and 9.
- Supports 62.4MHz, 124.8MHz and 249.6MHz PRF mode.
- Data rates of 6.81Mbps, 7.8Mbps, 27.24Mbps and 31.2Mbps.
- Complies with FCC&ETSI UWB spectral masks
- Supports 2-way ranging (DS-TWR) and one way ranging (TDoA)
- Supports 2D and 3D Angle of Arrival (AoA) measurement
- Surface mount type 6.6 x 5.8 mm(Typical), H = 1.2 mm(Max.)
- Weight : 107 mg
- MSL : 3
- RoHS compliant

## 3. Ordering Information

Ordering Part Number	Description
LBUA0VG2BP-741	MP order
LBUA0VG2BP-SMP	In case of sample order
LBUA0VG2BP-EVK-P	Evaluation Kit

## 4. Block Diagram



## **5. Certification Information**

### **5.1. Radio Certification**

#### **USA**

FCC ID: VPYLB2BP

\* Certified diversion is allowed only if the final product is the Hand-held system (PART 15 Subpart F §15.519) and is an exact copy of the antenna used.

Please see Appendix for the antenna registered by Murata.

#### **Canada**

IC: 772C-LB2BP

\* Certified diversion is allowed only if the final product is the Hand-held system (RSS-220 Section 5.3) and is an exact copy of the antenna used.

Please see Appendix for the antenna registered by Murata.

#### **Europe**

EN302065 conducted test report is prepared.

\*This test report is for reference only and not applicable to the customer's final product.

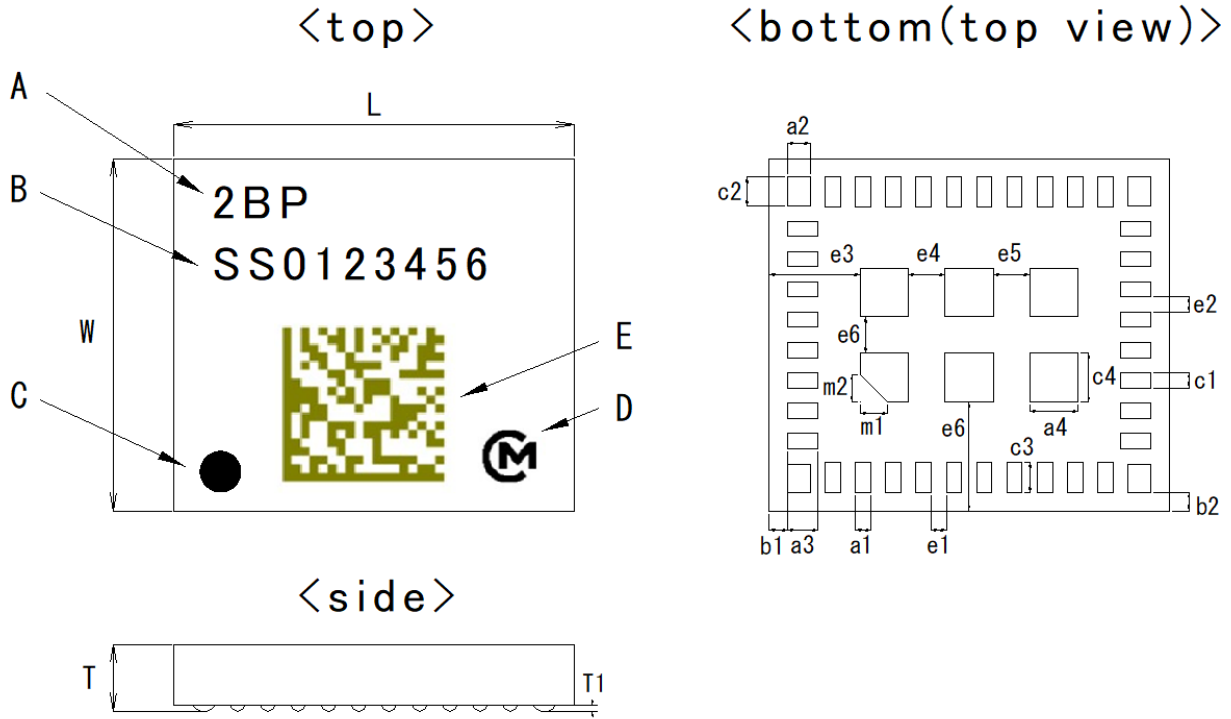
#### **Japan**

Japanese type certification is prepared.

Ⓜ 003-220111

\*Certified diversion is allowed only when the antenna applied for by Murata is used.

**6. Dimensions, Marking and Terminal Configurations**

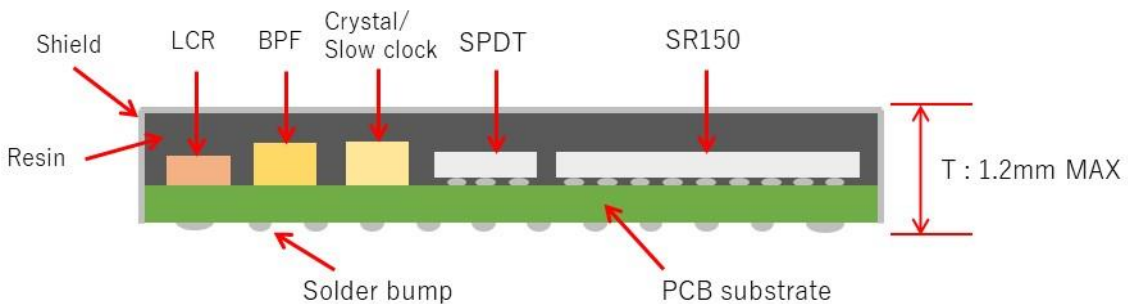


Marking	Meaning
A	Module Type
B	Inspection Number
C	Pin 1 Marking
D	Murata Logo
E	2D Code

(unit:mm)

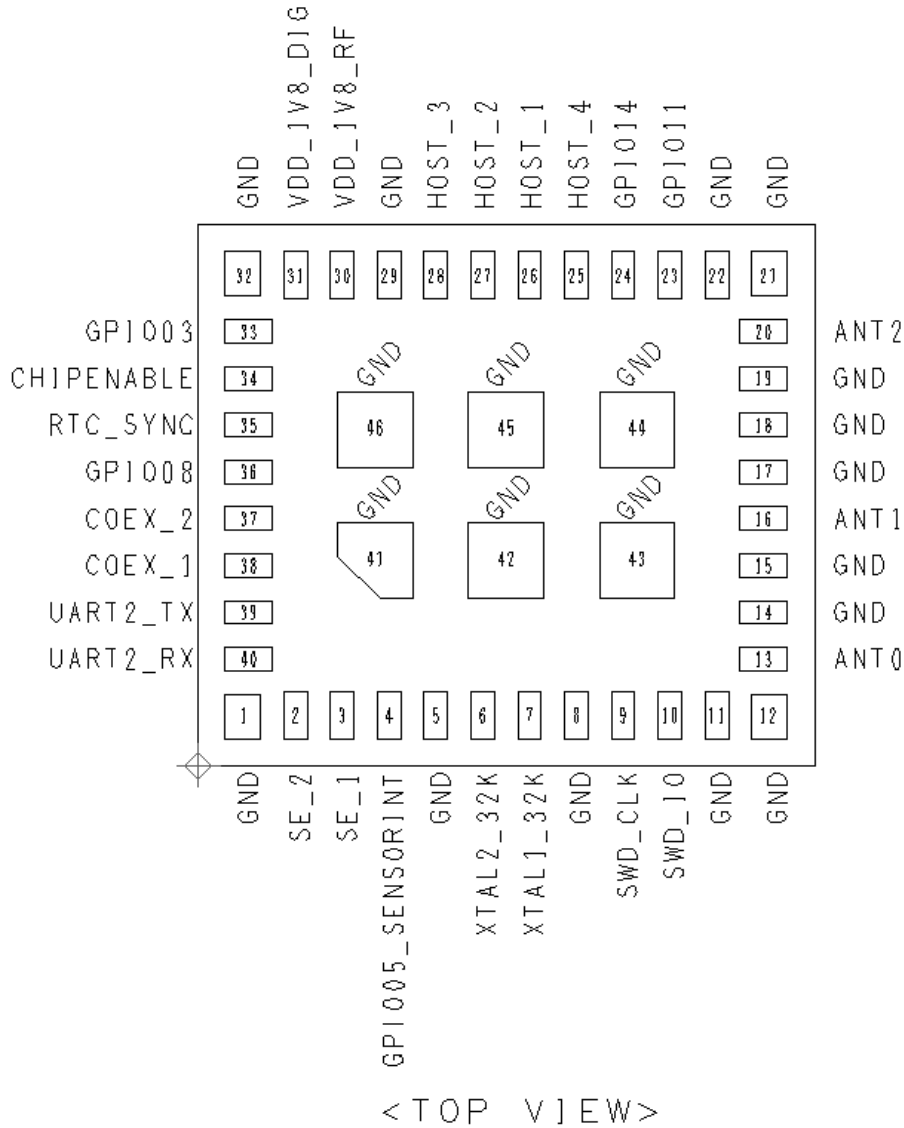
Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	6.6 +/- 0.2	W	5.8 +/- 0.2	—	—
T	1.20 max.	T1	0.045 typ.	—	—
a1	0.25 +/- 0.1	a2	0.375 +/- 0.1	a3	0.5 +/- 0.1
a4	0.8 +/- 0.1	b1	0.3 +/- 0.2	b2	0.3 +/- 0.2
c1	0.25 +/- 0.1	c2	0.475 +/- 0.1	c3	0.5 +/- 0.1
c4	0.8 +/- 0.1	e1	0.25 +/- 0.1	e2	0.25 +/- 0.1
e3	1.5 +/- 0.2	e4	0.6 +/- 0.1	e5	0.6 +/- 0.1
e6	1.8 +/- 0.2	m1	0.45 +/- 0.1	m2	0.45 +/- 0.1

**Structure**



## 7. Module Pin Descriptions

### 7.1. Pin Assignments



No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	13	ANT0	25	HOST_4	37	COEX_2
2	SE_2	14	GND	26	HOST_1	38	COEX_1
3	SE_1	15	GND	27	HOST_2	39	UART2_TX
4	GPIO05_SENSORINT	16	ANT1	28	HOST_3	40	UART2_RX
5	GND	17	GND	29	GND	41	GND
6	XTAL2_32K	18	GND	30	VDD_1V8_RF	42	GND
7	XTAL1_32K	19	GND	31	VDD_1V8_DIG	43	GND
8	GND	20	ANT2	32	GND	44	GND
9	SWD_CLK	21	GND	33	GPIO03_SYNC	45	GND
10	SWD_IO	22	GND	34	CHIPENABLE	46	GND
11	GND	23	GPIO11	35	RTC_SYNC		
12	GND	24	GPIO14	36	GPIO08		

## 7.2. Pin Description

No.	Pin Name	Type	Connection to IC pin name	Supply	Description
1	GND				
2	SE_2	I/O	SE_2	VDD_IO	NA Kept open.
3	SE_1	I/O	SE_1	VDD_IO	NA Kept open.
4	GPIO05_SENSORINT	I/O	GPIO05_HOST_INT	VDD_IO	IRQ to host for indicating data ready, switching time is 125ns
5	GND				
6	XTAL2_32K	I	XTAL2_32K		Reserved pin for external Xtal option, please leave this pin as NC.
7	XTAL1_32K	I	XTAL1_32K		Reserved pin for external Xtal option, please leave this pin as NC.
8	GND				
9	SWD_CLK	I/O	SWD_CLK		Serial Wire Debug interface clock input. Default configuration is secondary SPI bus clock interface connection SPI_SCK, switching time is 125ns.
10	SWD_IO	I/O	SWD_IO		Serial Wire Debug interface input/output. Default configuration is secondary SPI bus MISO connection, switching time is 125ns.
11	GND				
12	GND				
13	ANT0	RF	TX_OUT / RX2_IN		RF Antenna port, Tx / Rx switched by internal SPDT.
14	GND				
15	GND				
16	ANT1	RF	RX1_IN		RF Antenna port. ANT1 / ANT2 switched by internal SPDT.
17	GND				
18	GND				
19	GND				
20	ANT2	RF	RX1_IN		RF Antenna port. ANT1 / ANT2 switched by internal SPDT.
21	GND				
22	GND				
23	GPIO11	I/O	GPIO11_ANT_CTL1	VDD_IO	General purpose IO, switching time is dependent on the end control point, 125ns when controlled by ARM, 33ns when controlled by the DSP.
24	GPIO14	I/O	GPIO14_ANT_CTL2	VDDIO_HOST	General purpose IO, switching time is dependent on the end control point, 125ns when controlled by ARM, 33ns when controlled by the DSP.
25	HOST_4	I/O	HOST_4	VDDIO_HOST	Host Interface line 4, SPI MISO connection, switching time is 125ns.
26	HOST_1	I/O	HOST_1	VDDIO_HOST	Host Interface line 1, SPI clock line, switching time is 125ns.
27	HOST_2	I/O	HOST_2	VDDIO_HOST	Host Interface line 2, SPI slave connection, switching time is 125ns.
28	HOST_3	I/O	HOST_3	VDDIO_HOST	Host Interface line 3, SPI MOSI connection, switching time is 125ns.
29	GND				
30	VDD_1V8_RF	Power	VDD_PA / VIN_RF_1V8		VDD supply for PA and Vin input to 1.8V RF
31	VDD_1V8_DIG	Power	VDD_1V8 / VDD_IO / VDDIO_HOST		VDD for all Digital LDOs, Host interface and IO pins.
32	GND				
33	GPIO03_SYNC	I	GPIO03_SYNC	VDDIO_HOST	SPI Rx handshake from Host Interface, General purpose IO, switching time is 125ns



34	CHIPENABLE	I	CHIPENABLE	VDD_IO	Connection for disabling/enabling the chip
35	RTC_SYNC	I	RTC_SYNC	VDD_IO	Not used. Kept open
36	GPIO08_eSE	I/O	GPIO08_SE_IRQ	VDD_IO	NA Kept open
37	COEX_2	I/O	COEX_2		NA Kept open
38	COEX_1	I/O	COEX_1		NA Kept open
39	UART2_TX		UART2_TX		NA Kept open
40	UART2_RX		UART2_RX		NA Kept open
41	GND				
42	GND				
43	GND				
44	GND				
45	GND				
46	GND				

## 8. Absolute Maximum Ratings

Parameter	Min	Max	Unit	
Storage Temperature	-40	+85	deg.C	
Supply Voltage	VDD_1V8_DIG	-	2.5	V
	VDD_1V8_RF	-	2.5	V

\* Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

## 9. Operating Conditions

### 9.1. Operating conditions

Parameter	Min	Typ	Max	Unit	
Operating Temperature Range	-30	+25	+85	deg.C	
Supply Voltage	VDD_1V8_DIG	1.71	1.8	1.98	V
	VDD_1V8_RF	1.71	1.8	1.98	V

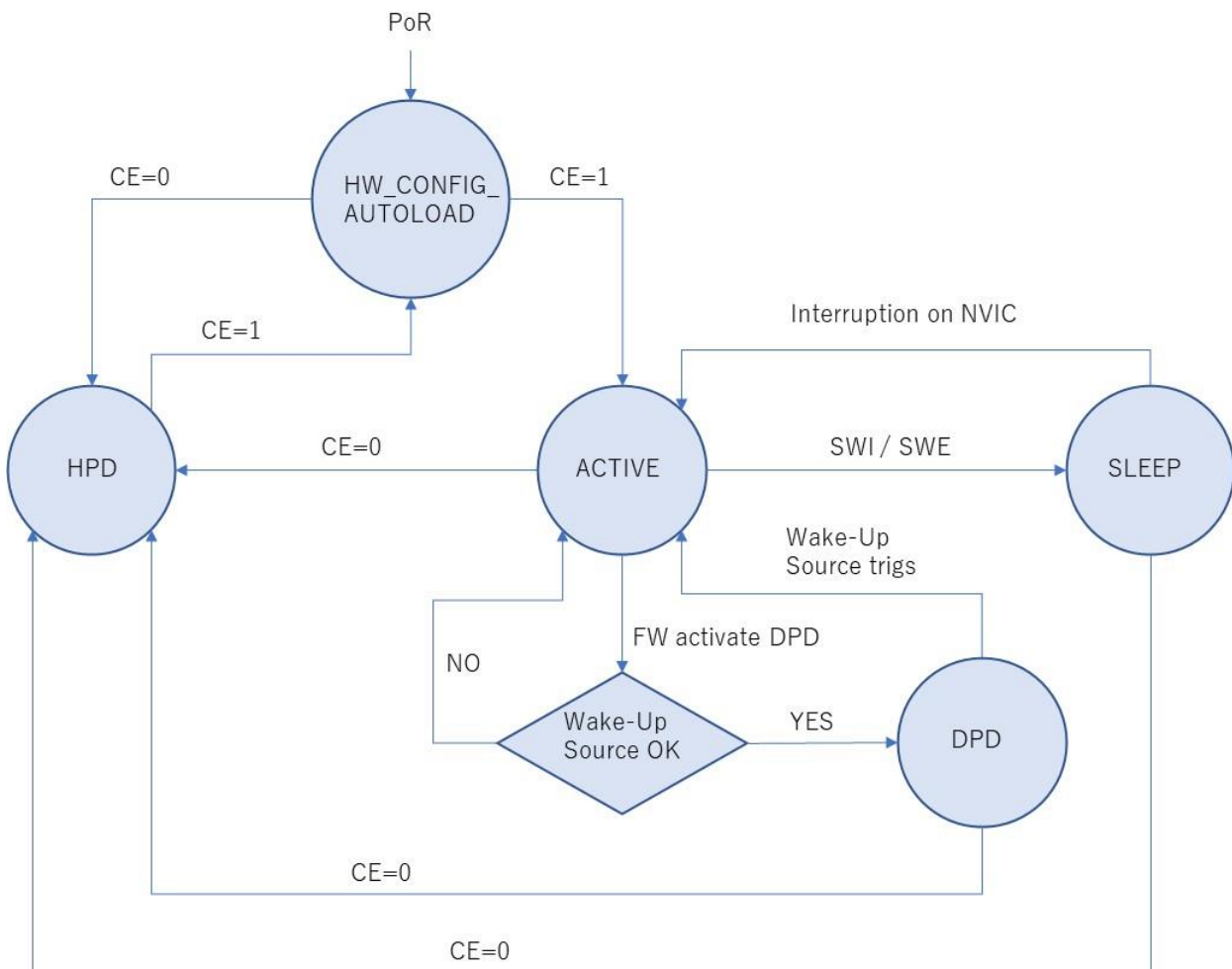
## 10. System power status and power sequence

### 10.1. System Modes

This module has 6 power modes : HPD (Hard Power Down) mode, DPD (Deep Power Down) mode, Deep power down retention mode, Sleep, Active mode and Hardware configuration Autoload. Here is the description of these modes.

System power state	Description
Active mode	The device is running and supplied by Platform PMU, in this mode several active states are available : Idle, TX, RX and Dual RX.
Deep power down(DPD) retention mode	The device is in low power mode and supplied by the Platform PMU, the memory is supplied, a configured wake up can bring the device back to the Active mode, no RF communication is possible.
Sleep	Specific parts can be active or inactive, this sleep mode can be configured by firmware which enables several power states, no RF communication is possible.
Hard power down(HPD) mode	The device is powered down and supplied by the PMU, it can be activated by the CE (CHIPENABLE) signal.
Hardware configuration Autoload	The device is supplied by the platform PMU and is loading the Hardware configuration and firmware into the memory.

### 10.2. State Diagram and Power modes

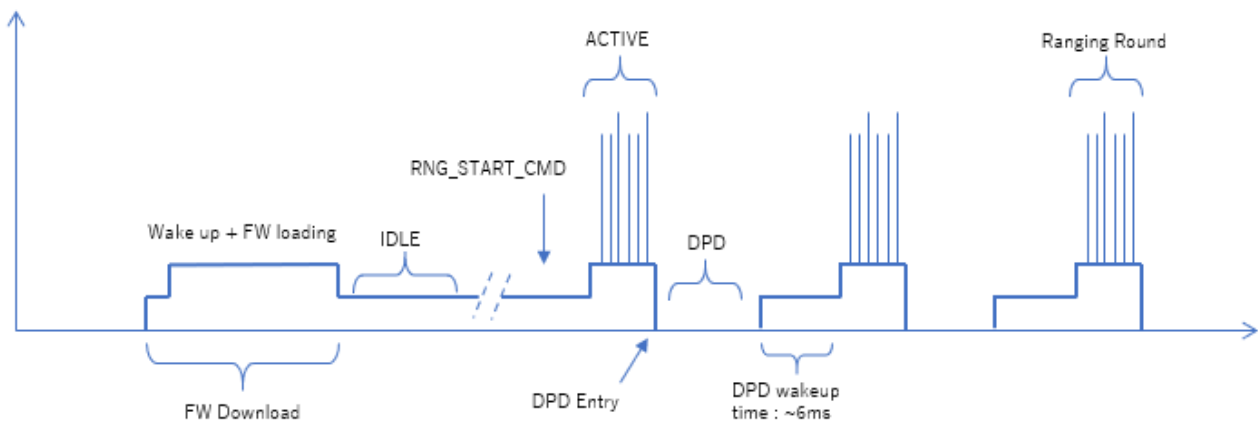


**10.3. Power mode entry and exit conditions**

Power state	Entry Condition	Exit Condition
HPD	Two possible methods <ul style="list-style-type: none"> <li>• Software command</li> <li>• Assert CE low for &gt; 80us</li> </ul>	<ul style="list-style-type: none"> <li>• Assert CE to high</li> </ul>
DPD with memory retention mode	<ul style="list-style-type: none"> <li>• Software command</li> </ul>	Exit to HPD state: <ul style="list-style-type: none"> <li>• Assert CE low for &gt; 80us</li> </ul> Exit to Active state: <ul style="list-style-type: none"> <li>• Wake up timer expired</li> <li>• Temperature sensor event</li> <li>• SPI NSS Negative Edge, GPIO(3,5) event.</li> </ul>
ACTIVE	<ul style="list-style-type: none"> <li>• End of system boot after wake up</li> <li>• Wake up timer expired</li> <li>• Temperature sensor event</li> <li>• SPI NSS Negative Edge, GPIO(3,5) event.</li> </ul>	<ul style="list-style-type: none"> <li>• Software command</li> <li>• Assert CE low for &gt; 80us</li> </ul>

The time required for the module to go into DPD state is < 100us controlled by the firmware. The required time for the module to enter HPD state is less then 100us starting for the instance that CE is de-asserted, in both modes VDD\_1V8\_DIG is turned off. The Wakeup timing from DPD state is around 370us, the wakeup from HPD state is triggered once CE is asserted and takes around 380us.

Here is typical system power cycle image.

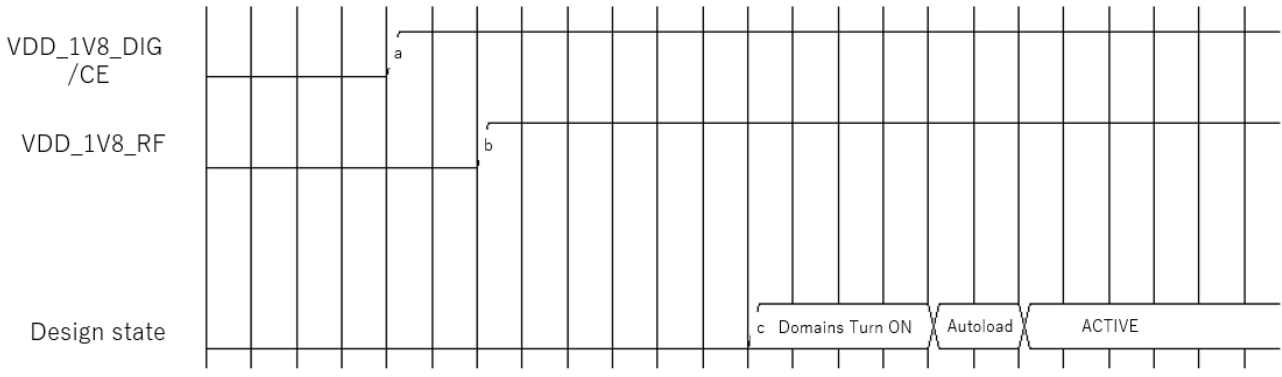


**10.4. Power Timing diagrams**

PMU of SR150 subsystem has a main power up sequence that require VDD\_1V8\_DIG, VDD\_1V8\_RF and CE(CHIPENALBE) to be orderly powered to boot-up.

In all cases, host communication with SR150 will only be possible after one defined amount of time from the different supply sequence setup and CE at rising edge.

High level boot sequence is indicated below, power supply start-up time should be followed. CE pin must be set to high only when VDD\_IO and VDDIO\_HOST are high. Then the CE pin level will be take into account from autoload phase.

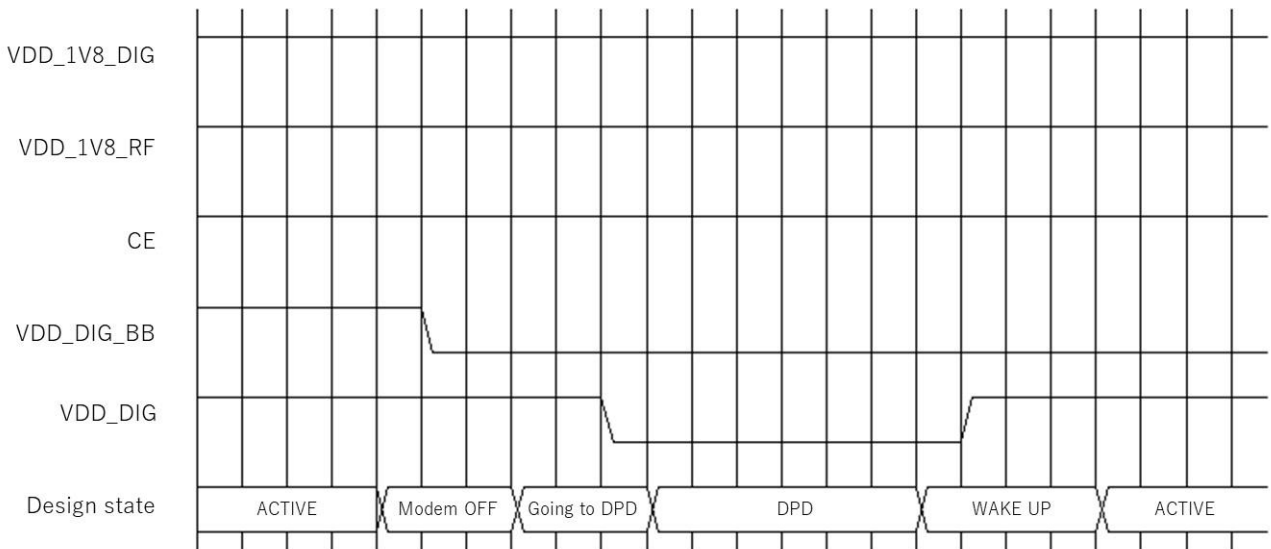


a~b :  $\geq 0\mu s$   
b~c :  $\geq 900\mu s$

CE pin must be set to high only VDD\_1V8\_DIG is high.

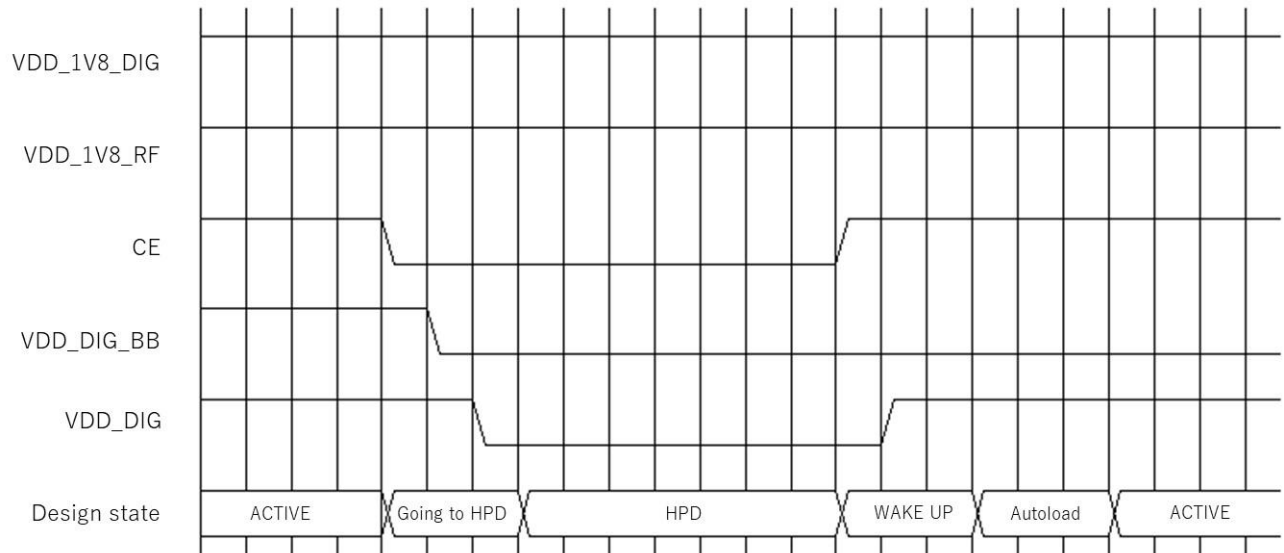
**10.5.1 Deep Power-down (DPD) sequence**

In DPD Low power mode, CE need to be High all the time, Modem domain needs to be turned OFF before decided to go to DPD. All IOs are retained to same state before going to DPD. All high frequency clocks



### 10.5.2 Hard Power-down (HPD) sequence

HPD is lowest Power mode where only SR150 AON domain is ON and rest of the power domains of SR150s are in OFF state. (Note : note the VDD\_1V8\_RF supplies connected to internal RF switch and it also causing leak current. The dominant current consumption factors in HPD mode are current consumption of SR150 HPD state and leakage current of RF switch). HPD state can be entered or exited only by CE pin.



## 11 Host Interface (SPI)

The SR150 supports SPI-bus Master/Slave interface, up to 16.66Mbits/s.

### SPI-bus configuration options

The operation mode of the SPI-bus is shown in below table, CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity. Default setting of CHPA/CPOL settings are CHPA=0, CPOL=0.

Connection
CPHA switch: Clock Phase: defines the sampling edge of MOSI data <ul style="list-style-type: none"> <li>• CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low</li> <li>• CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low</li> </ul>
CPOL switch : Clock Polarity <ul style="list-style-type: none"> <li>• CPOL = 0: the clock is idle low and the first valid edge of SCK will be a rising one</li> <li>• CPOL = 1: the clock is idle high and the first valid edge of SCK will be a falling one</li> </ul>

The SPI-bus interface shares the pins with the other host interfaces that are supported by SR150. When SPI-bus is configured the functionality of the interface pins is as described in below table.

Pin name	Functionality
Host_1	SCK (Serial input Clock)
Host_2	NSS (Not Slave Select)
Host_3	MOSI (Master Out Slave In)
Host_4	MISO (Master In Slave Out)

### SPI-bus functional description

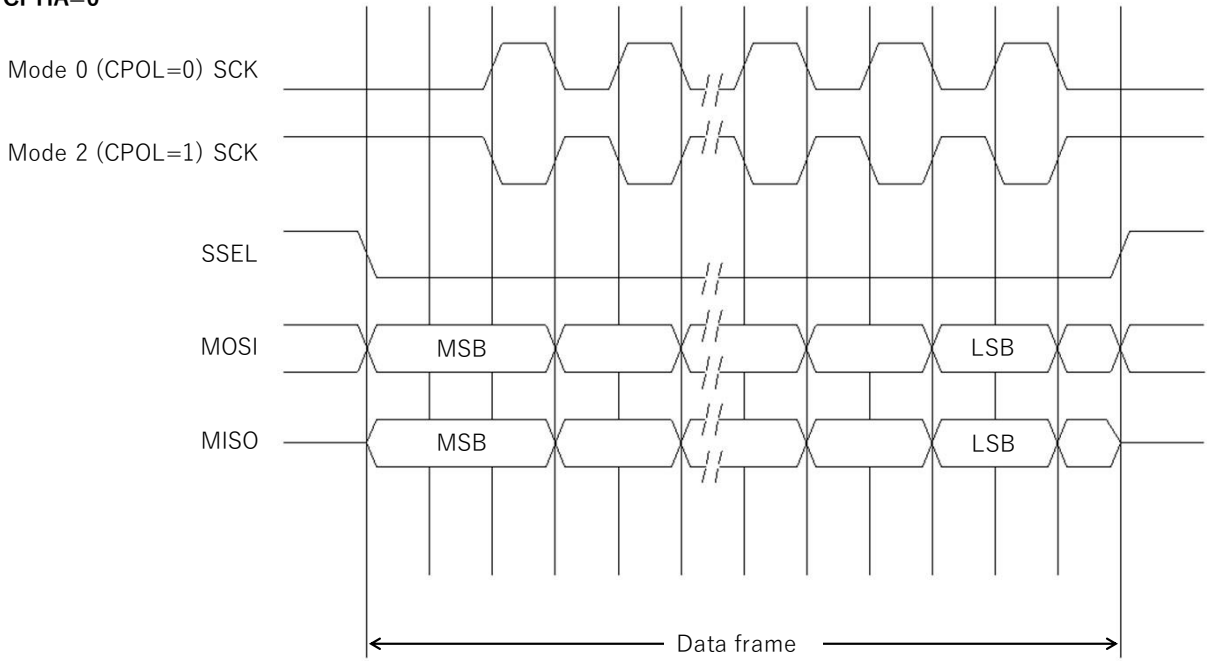
When a master device transmits data to the SR150 via the MOSI line, the SR150 responds by sending data to the master device via the MISO line. This implies full-duplex transmission with both, data out and data in synchronized with the same clock signal.

SR150 starts sampling when receiving a logic low at pins NSS Host\_2 pin and the clock at input pin SHOST\_1. Thus, SR150 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loaded in the 8-bit shift register. After the 8bit shift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then the SR150 waits for a clock train from the master to shift the data out on the MISO line.

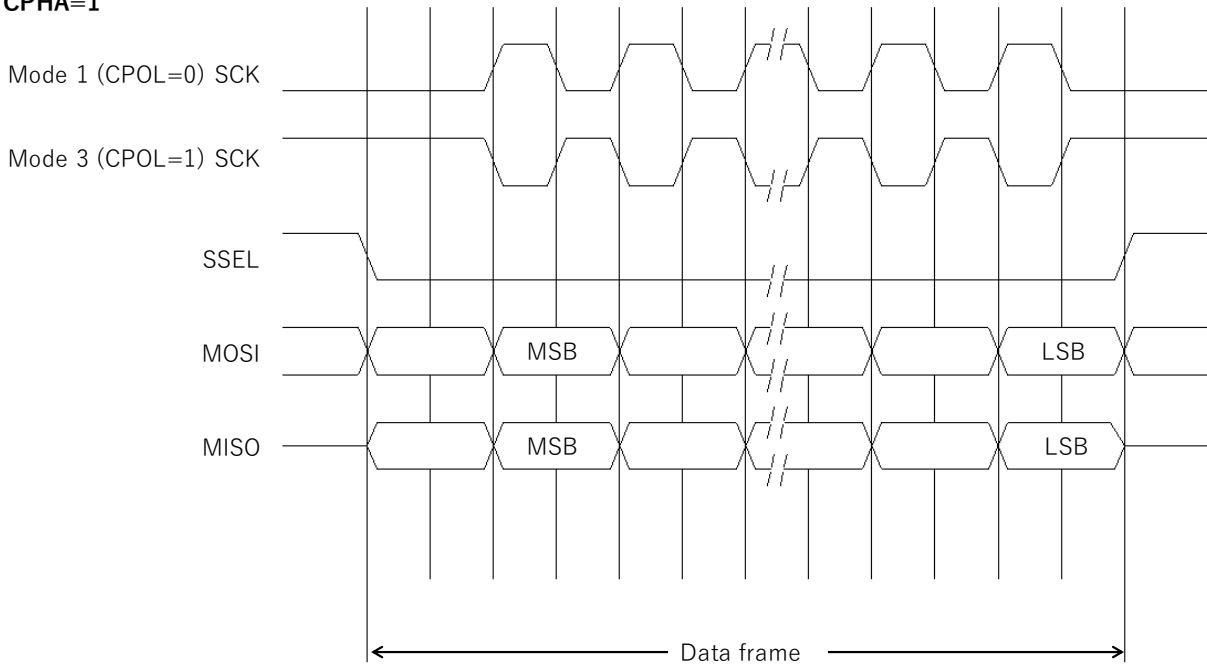
Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, for the slave device to latch the data.

SR150 SPI data frame

**CPHA=0**

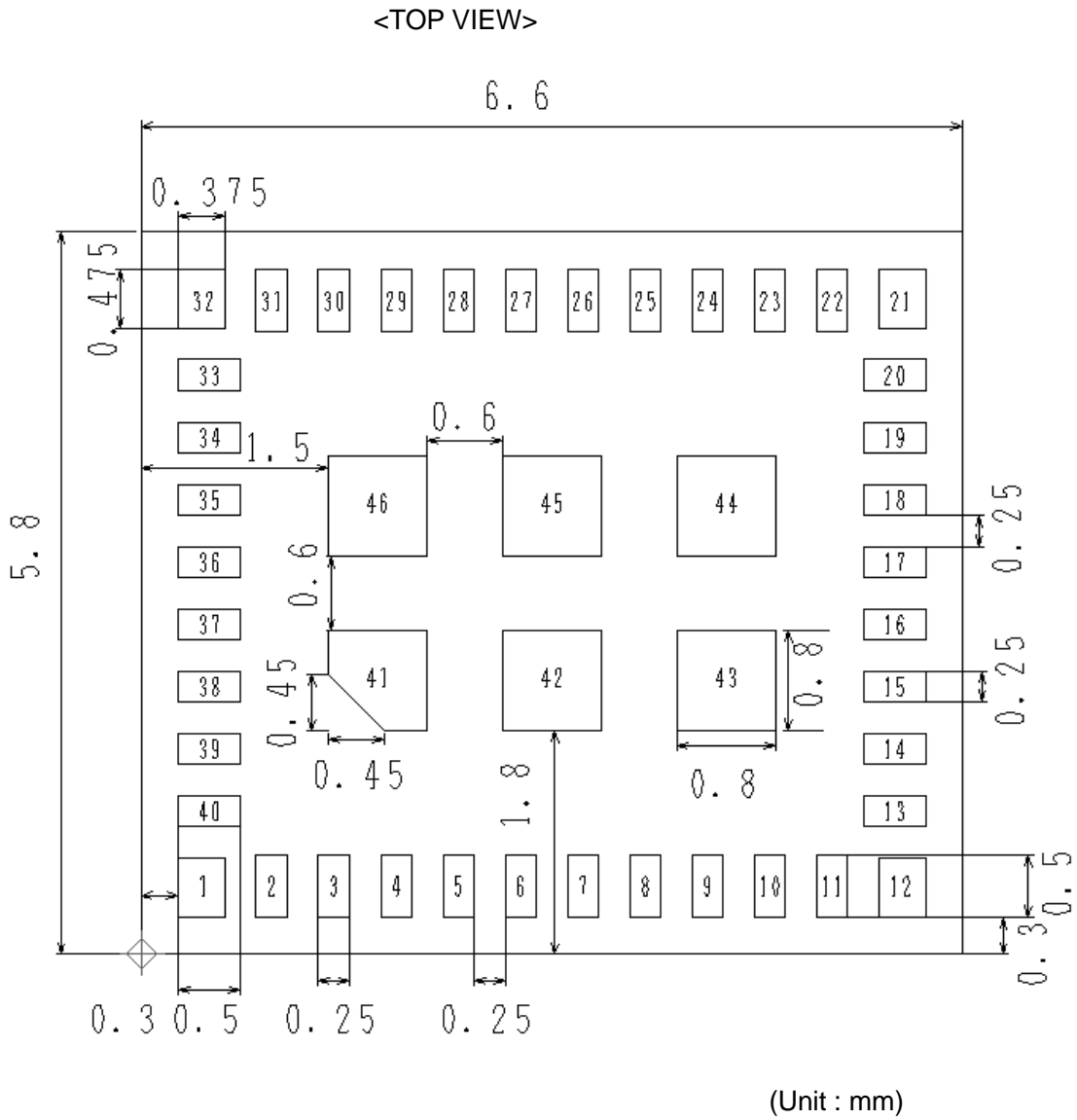


**CPHA=1**



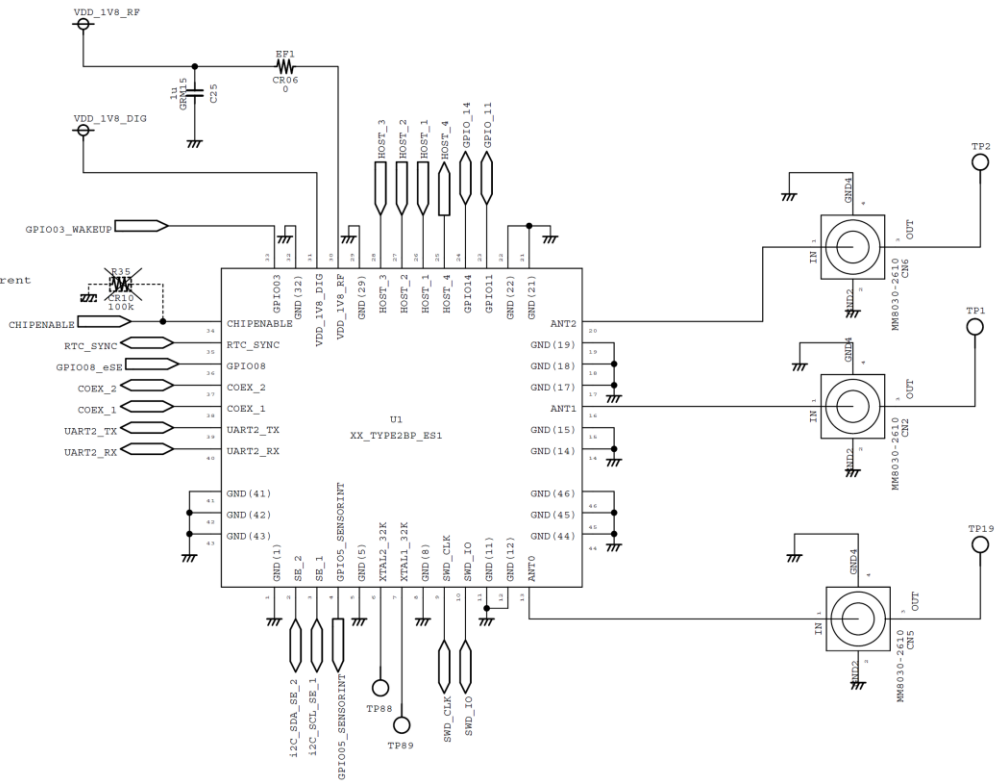


**12 Recommended land pattern**



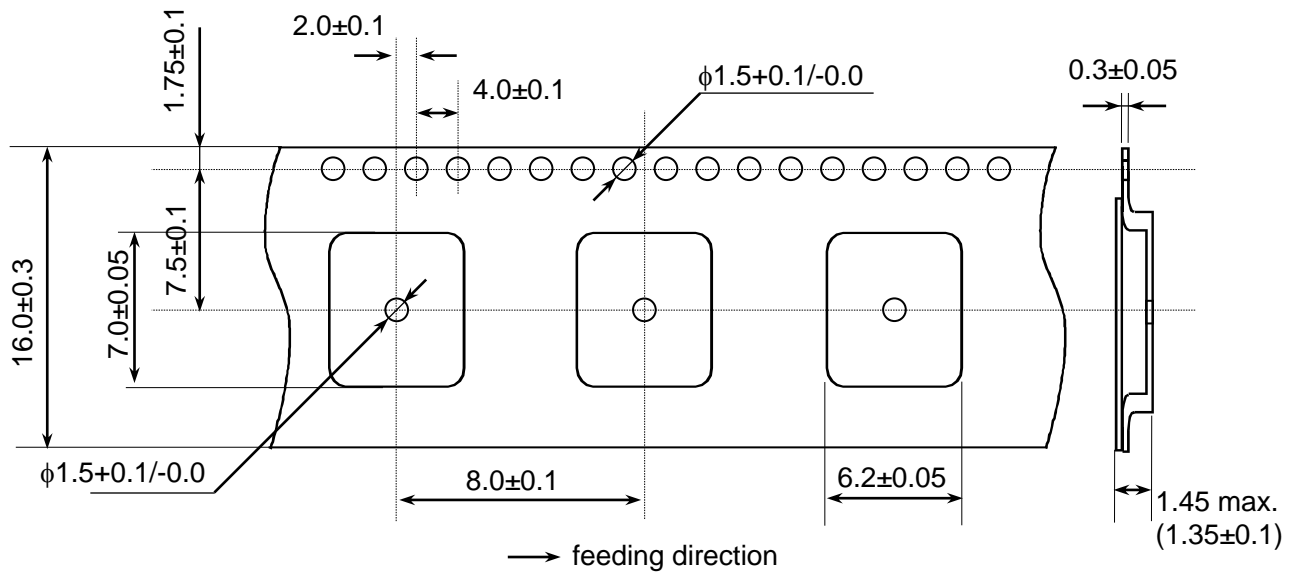
**13 Reference Circuit**

R35: "no mount" for Smaller current consumption in DPD mode.



## 14 Tape and Reel Packing

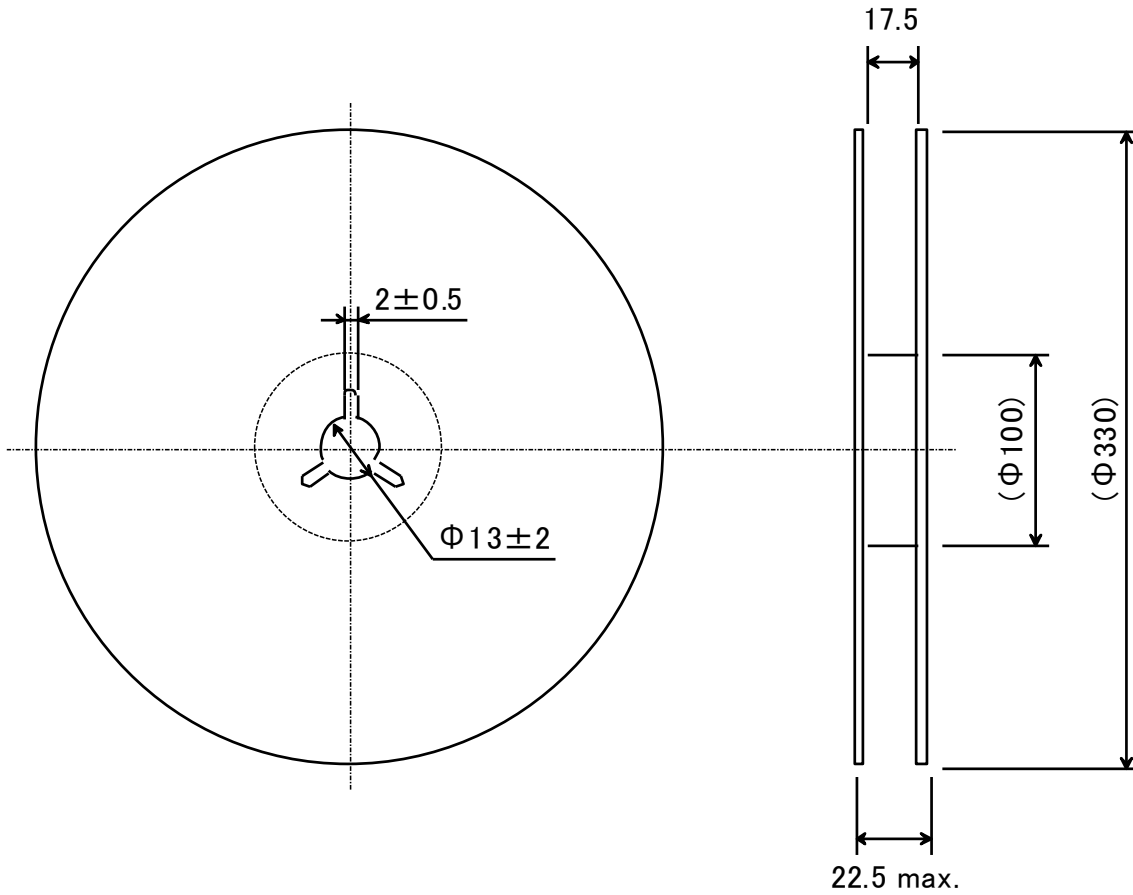
### (1) Dimensions of Tape (Plastic tape)



- 1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
- 2) Cumulative tolerance of 10 pitches of the sprocket hole is  $\pm 0.15$ mm
- 3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

(Unit : mm)

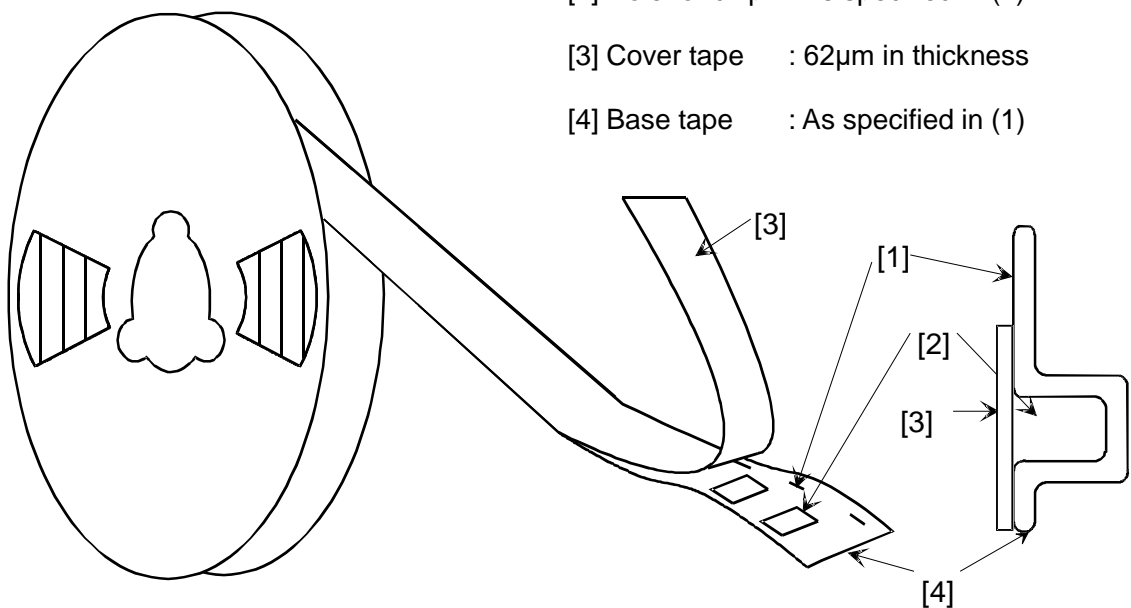
(2) Dimensions of Reel

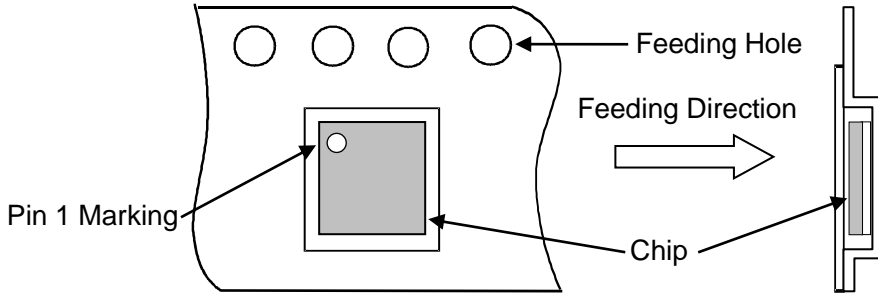


(unit : mm)

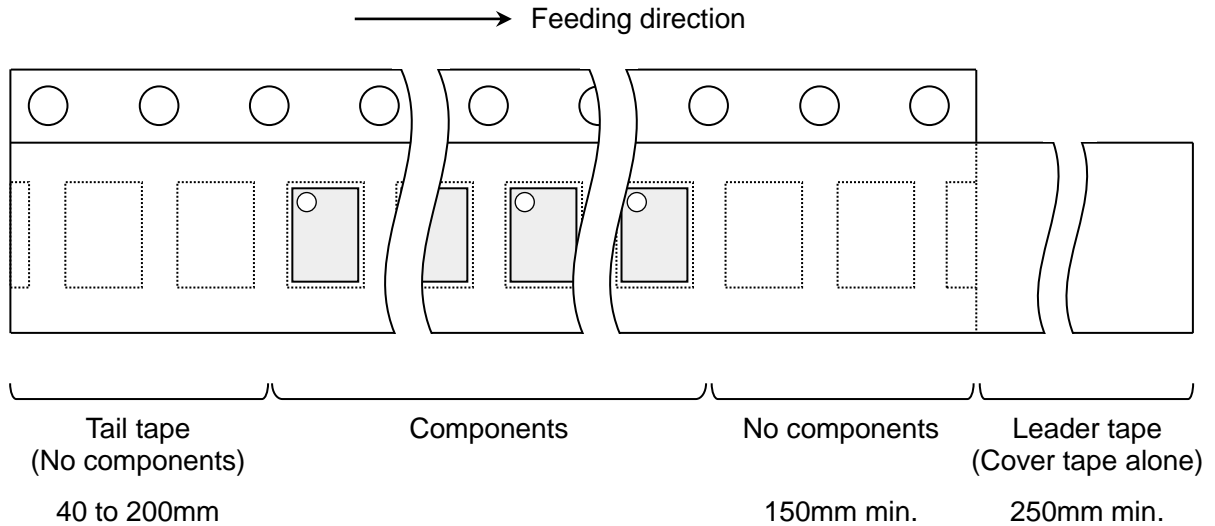
(3) Taping Diagrams

- [1] Feeding Hole : As specified in (1)
- [2] Hole for chip : As specified in (1)
- [3] Cover tape : 62 $\mu$ m in thickness
- [4] Base tape : As specified in (1)





(4) Leader and Tail tape



(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

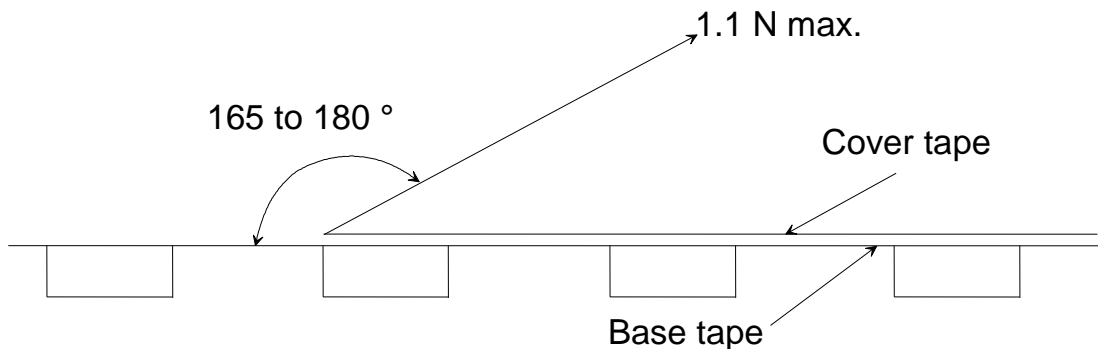
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

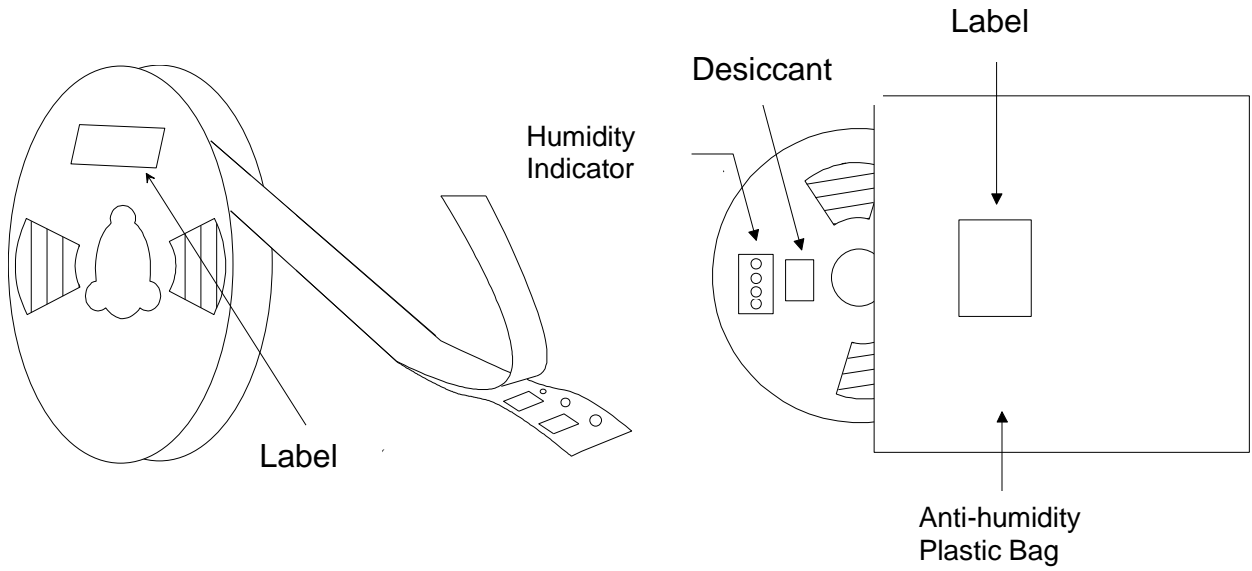
(8) Packaging unit : 1000pcs./ reel

(9) material : Base tape : Plastic  
Real : Plastic  
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : 1.1N max. in the direction of peeling as shown below.



(11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

## 15 **NOTICE**

### 15.1 **Storage Conditions:**

Please use this product within 6month after receipt.

- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.  
(Packing materials, in particular, may be deformed at the temperature over 40 °C)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>2</sub>, Nox, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)

- After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition : 125 +5/-0 °C, 24 hours, 1 time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

### 15.2 **Handling Conditions:**

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

### 15.3 **Standard PCB Design (Land Pattern and Dimensions):**

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

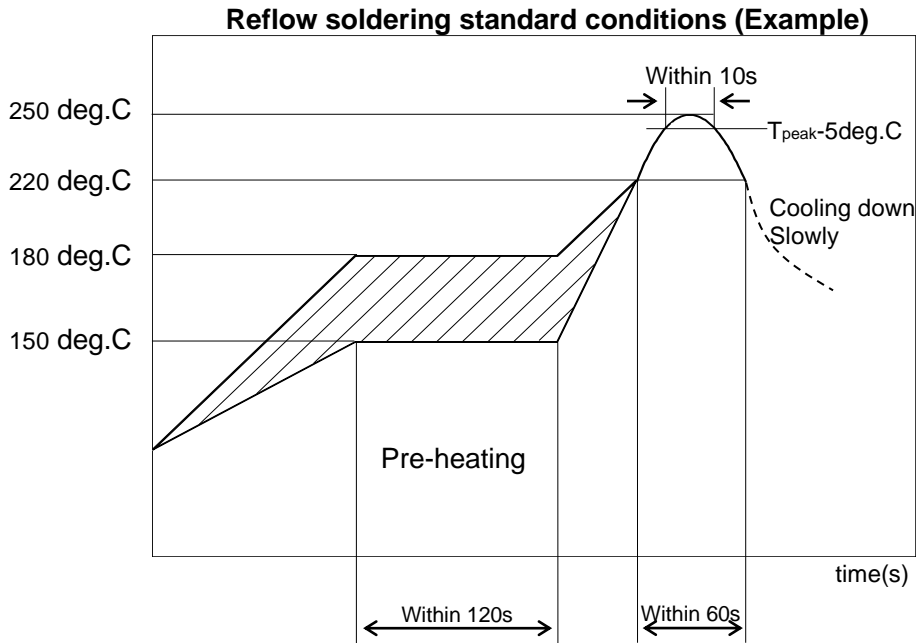
The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

### 15.4 **Notice for Chip Placer:**

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

### 15.5 Soldering Conditions:

The recommendation conditions of soldering are as in the following figure. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.



Please use the reflow within 2 times.  
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

### 15.6 Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

### 15.7 Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas ( Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>x</sub>, NO<sub>x</sub> etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.



## **16 PRECONDITION TO USE OUR PRODUCTS**

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

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- Power plant control equipment
- Burning / explosion control equipment
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.
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