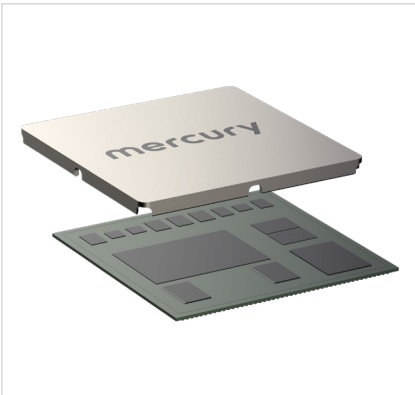**mercury**

RFS1140 RFSiP
RF System-in-Package: 64GSPS and Versal® ACAP Enabled Processing

Direct-to-digital processing at chip scale

- Onshore design and manufacturing at a DMEA-accredited facility
- High-speed data conversion with four channels

- 64 GSPS per channel
- Versal FPGA processing
- On-chip power and memory

The advanced System-in-Package RFS1140 consists of an AMD Versal® FPGA, Jariet high-speed data converters and integrated power and memory. This technology, combined with Mercury's onshore design and manufacturing, brings commercial technology to mission-critical applications creating a trusted and secure solution for modern sensor processing at the edge.

The RFS1140 offers direct digitization and massive processing while maintaining SWaP-C optimization through the reduction of multiple boards and reducing overall system cost. The on-chip memory and power management simplify system design and integration and contribute to overall system longevity.

Included in the SiP is the AMD Versal ACAP for the heterogeneous integration of best-in-class technology for increased performance per unit area. With direct digitization up to 32 GHz and 4 channels each of ADC and DAC data conversion operating at 64 GSPS per channel, the RFS1140 offers the most advanced processing capability for applications where ultra-low data latency is critical for success.

Highlights

- First advanced Versal RFSiP developed and manufactured onshore with ultra-fast data conversion rates up to 64 GSPS
- On-chip memory and power management for ease of system design and integration
- Development platform available — ask your sales representative for details

64 GSPS
direct digitization

4
channels each of ADC/DAC
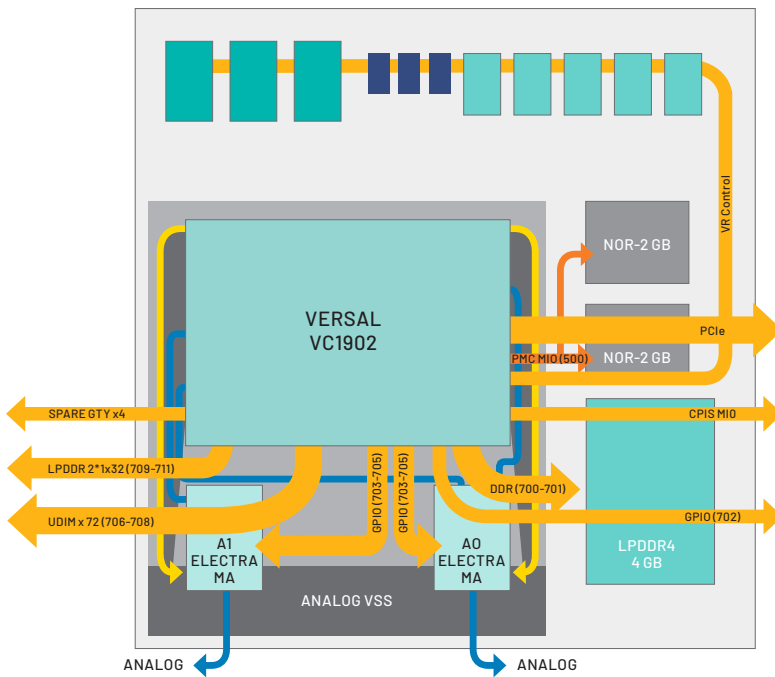
AMD Versal®
technology

4 GB
LPDDR4 memory

APPLICATIONS

- Military and aerospace: Radar, EW, EA, ISR, ELINT
- Comm commercial: 5G base station, PtP, test and measurement equipment, autonomous vehicles Radiometry
- Test and measurement
- Phased array and data aggregation end uses

RFS1140 with integrated PoL

AMD VERSAL ACAP

AMD Versal® devices are the industry's first adaptive compute acceleration platform (ACAP), combining adaptable processing and acceleration engines with programmable logic and configurable connectivity to enable customized, heterogeneous hardware solutions for a wide variety of applications in the data center, automotive, 5G wireless, wired and defense industries. Versal ACAPs feature transformational technologies like an integrated silicon host interconnect shell and Intelligent Engines (AI and DSP), Adaptable Engines and Scalar Engines, providing superior performance per watt over conventional FPGAs, CPUs and GPUs. The VC1902 is part of the AI Core high-compute series with medium-density programmable logic and connectivity capability coupled with AI and DSP acceleration engines.

VERSAL ACAP FEATURES

FEATURE	VC1902
AI Engines	400
AIE/AIR-ML Data Memory (Mb)	100
DSP Engines	1,968
System Logic Cells	1,968,400
CLB Flip-Flops	1,799,680
LUTs	899,840
Distributed RAM (Mb)	27.5
Block RAM Blocks	967
Block RAM (Mb)	34
UltraRAM Blocks	463
UltraRAM (Mb)	130.2
Accelerator RAM (Mb)	0
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 cache w/ parity and ECC; 1 MB L2 cache w/ ECC
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 cache, and TCM w/ECC
Memory	256 KB on-chip memory w/ECC
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)
NoC Master/Slave Ports	28
DDR Bus Width	256
DDR Memory Controllers	4
PCIe w/DMA & CCIX (CPM4)	1 x Gen 4x16, CCIX
PCIe (PLPCIE4)	4 x Gen 4x8
100G Multirate Ethernet MAC	4
XPIO	648
HDIO	44
GTY Transceiver (32.75Gb/s)	44

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HIGH-SPEED JARIET DATA CONVERSION

The Jariet Electra-MA transceiver enables the end user to eliminate substantial portions of the RF and microwave block diagram based on the ability to directly digitize waveforms from 40 to 64 GSPS per channel with analog frequencies as high as 36 GHz and instantaneous bandwidths in excess of 4 GHz. At the same time, the 10-bit converters are extremely DC power efficient based on state-of-the-art 14nm CMOS technology, and are designed and fabricated in the United States at Global Foundries.

Each channel is based on interleaved ADCs and DACs followed by programmable digital up and down conversion, linear and non-linear equalization, decimation and interpolation and a 16-bit SerDes baseband data interface. A 12-bit interface is also available for x8 and x16 decimation and interpolation rates. A single Fs/16 or Fs/32 reference clock is distributed to all channels, simplifying PCB and package routing. For single-ended applications that would not benefit from array-based phase noise improvements, the clock multiplier unit can be bypassed and a half-rate low-noise reference clock injected. Additionally, an optional synchronization clock input allows precise alignment of all channels within the ASIC and between multiple ASICs when used in an array.
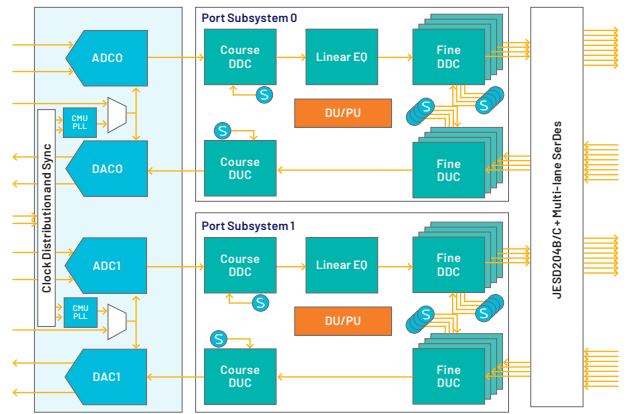
TECHNICAL SPECIFICATIONS

ADC/DAC Performance

4-channels each, ADC and DAC at 64 GSPS

Operation in 1st Nyquist zone up to 32 GHz

ADC & DAC directly digitized through 36 GHz

Broad instantaneous bandwidth > 4 GHz

Memory

4 GB LPDDR4

- 4266 Mbps max data rate
- 1600 MHZ max clock speed
- 256 M x 32

2 Gb NOR Flash

Power Supply

Integrated power regulation

Power with POL

- Max power 145 W, Typical 125 W

Mechanicals

Dimensions:

- 50 x 50 x 5 mm with integrated power
- 50 x 40 x 5 mm without integrated power

Operating temperature range –40° C to +85° C

Storage temperature –55° C to +105° C

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