Attracting Tomorrow

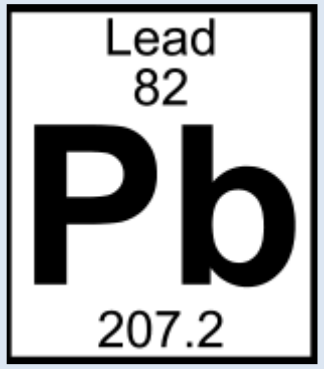
Ceramic Capacitor Technology

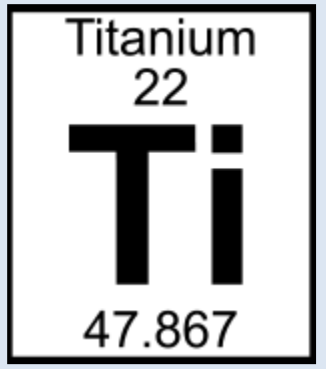
CeraLink® Opens New Dimensions in Power Electronics

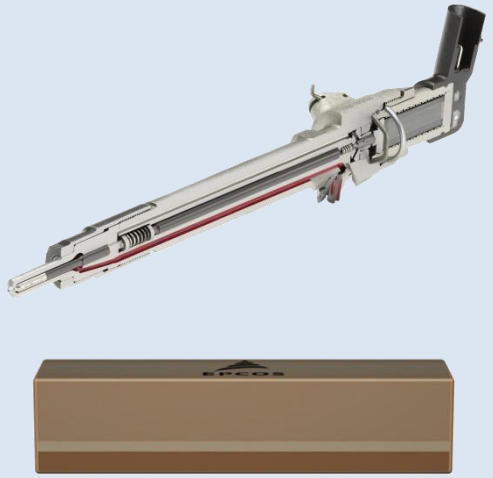
TDK Electronics AG
Piezo and Protection Devices Business Group
Product Marketing PI AE/IE Munich, Germany
June 2020

Ceramic Capacitor Technology

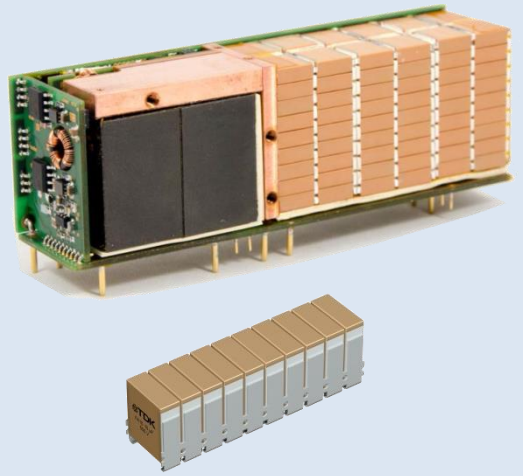
PZT – a highly flexible ceramic material class





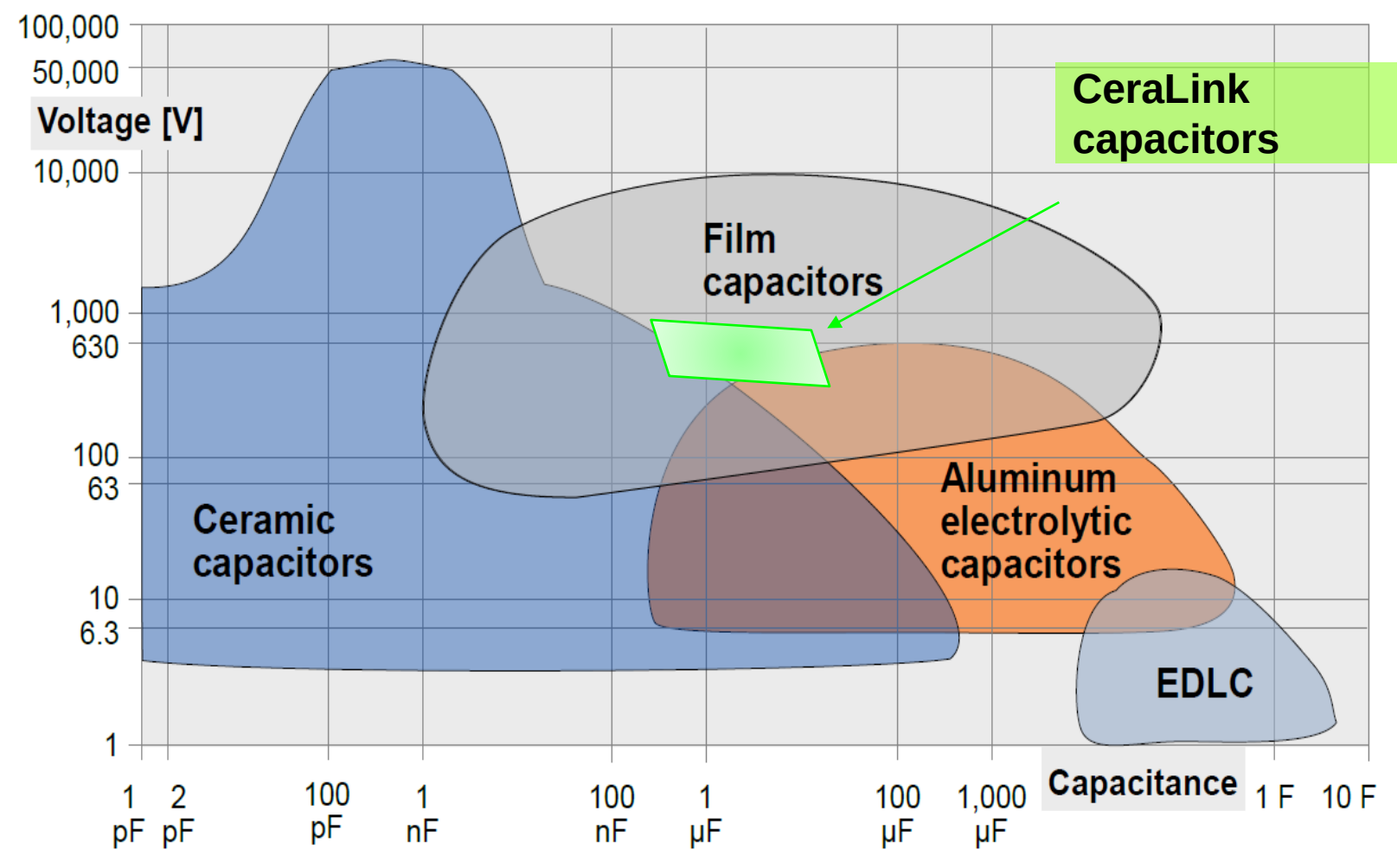


Piezo actuators



Capacitors

CeraLink® at a first glance



Applications
SiC & GaN

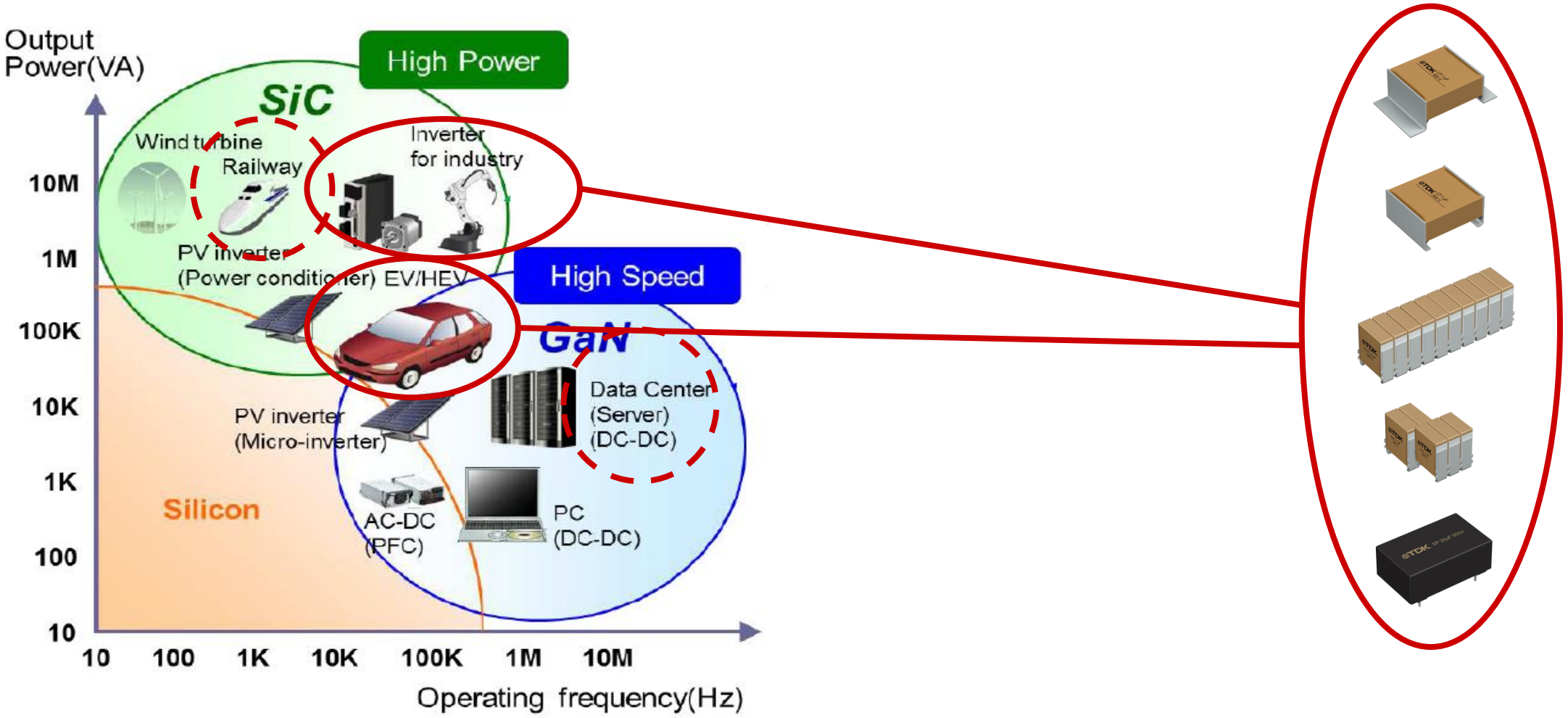
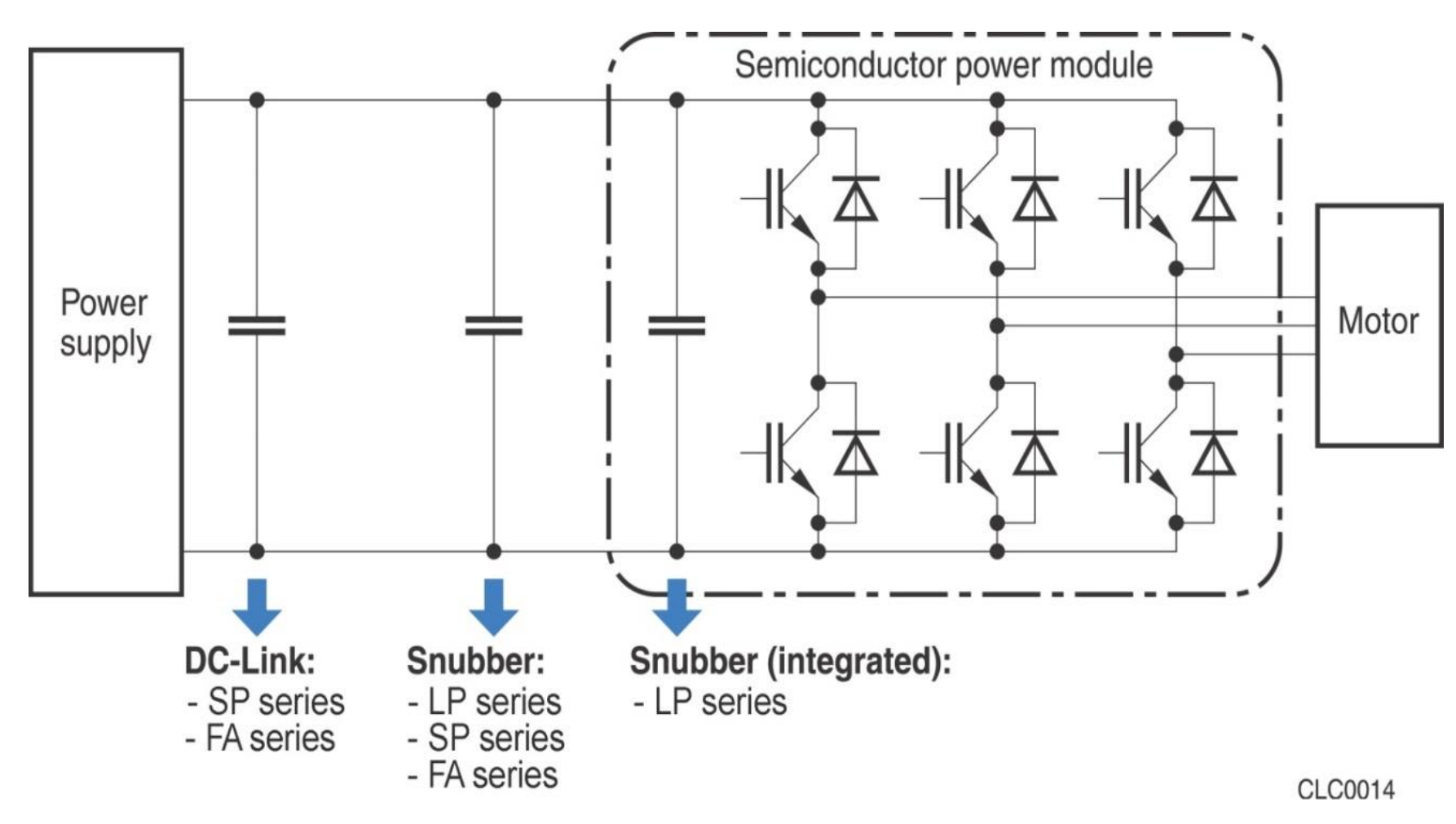


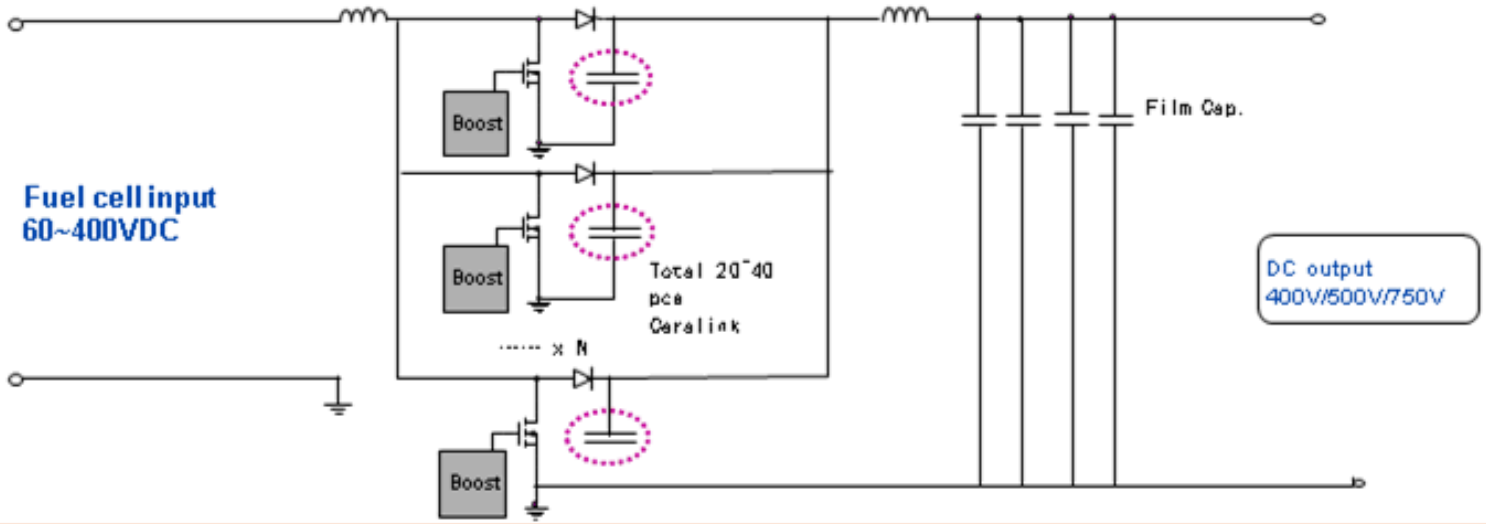
Image: Panasonic

CeraLink at a first glance



CeraLink in output filter

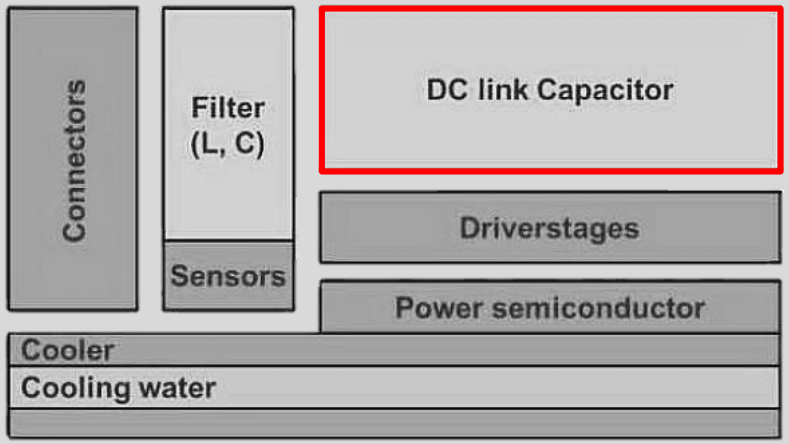
HV Output filtering in Fuel cell vehicle



Highlight:	CeraLink for HV filtering
Application	80KW~150KW DC/DC with SIC MOS technology
Application field	DC/DC for Fuel cell vehicle
Function of CeraLink™	High Ripple current capability ~100A SMD **mounting on AL base board & close to SIC MOS** **Meet <7mm low profile requirement**
Benefits on system level	**Withstand the high temperature (180° C, 4S) in production** **High working temperature ~110° C** **High frequency ~80KHz**

New demands for DC link capacitors

Improvements in power density and efficiency were mainly driven by semiconductor technology in the last decade.



Example: principle block picture and size comparison of a motor inverter

"Today the package of a motor inverter is mainly driven by the size of the capacitor, the bus bars, the terminal box and the filter components."

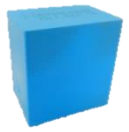
Source: Plikat, Mertens, Koch, Volkswagen AG, Corporate Research, 2013

Requirements for a DC link capacitor

- High capacitance density
- High current density
- Low parasitic values (ESR/ESL) for fast switching
- Low losses in operation
- High operating and peak temperatures
- High cooling efficiency due to high thermal conductivity
- Support of distributed DC link capacitor topologies with low inductance components (modular design)

Technology guideline

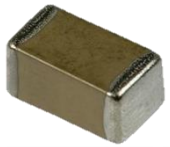
Film Capacitor



- more compact
- higher operating temperature
- lower ESL
- higher frequency
- SMD
- higher ripple current ratings

Standard semiconductor technology

Large MLCC Chips



- more compact / less footprint
- lower ESL
- more robust

Standard semiconductor technology

Stacked MLCC

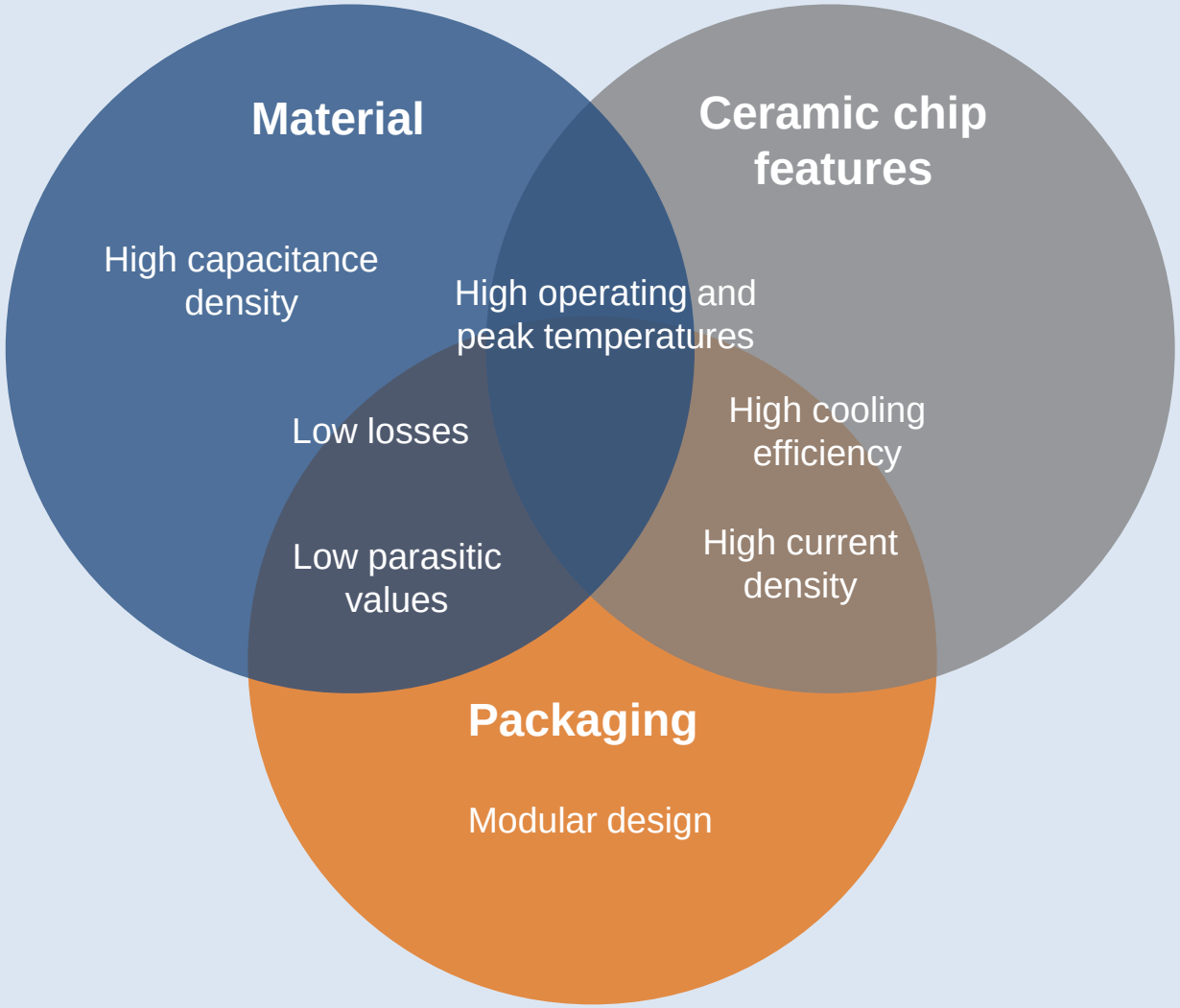
- higher cap-density at V_{op}
- higher operating temperature
- lower ESL
- higher ripple current ratings

Enhanced technologies / modular ceramic designs possible / automotive

CeraLink

High-end and high-temperature applications / fast switching (SiC) / full ceramic DC-link solutions

How does CeraLink meet these requirements?



Material
PLZT – an antiferroelectric material

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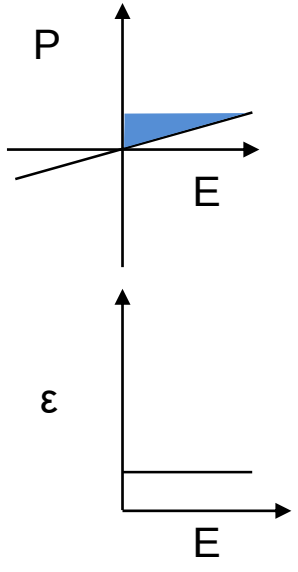
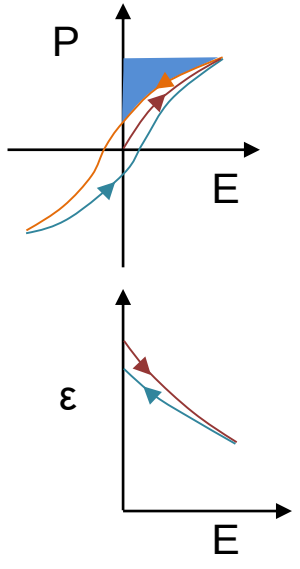
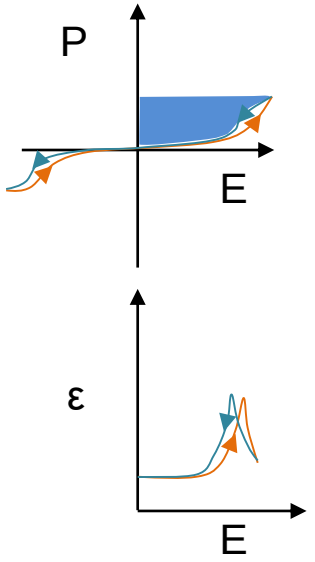
Linear	Ferroelectric	Antiferroelectric
		

Nature of electrical polarization	Electronic, ionic	Permanent dipoles form ferroelectric domains	Permanent dipoles form antiparallel zones
Material class	(Ba,Nd)TiO, typ. NP0, C0G	$BaTiO_3$ (BTO), typ. X7R	$(Pb,La)(Zr,Ti)O_3$ (PLZT)
Advantages	ε constant over electric field and temperature	ε up to 10,000 is possible	ε increases with field
Disadvantages	ε < 100	ε decreases strongly with electrical field	ε low at zero bias

P Dielectric polarization

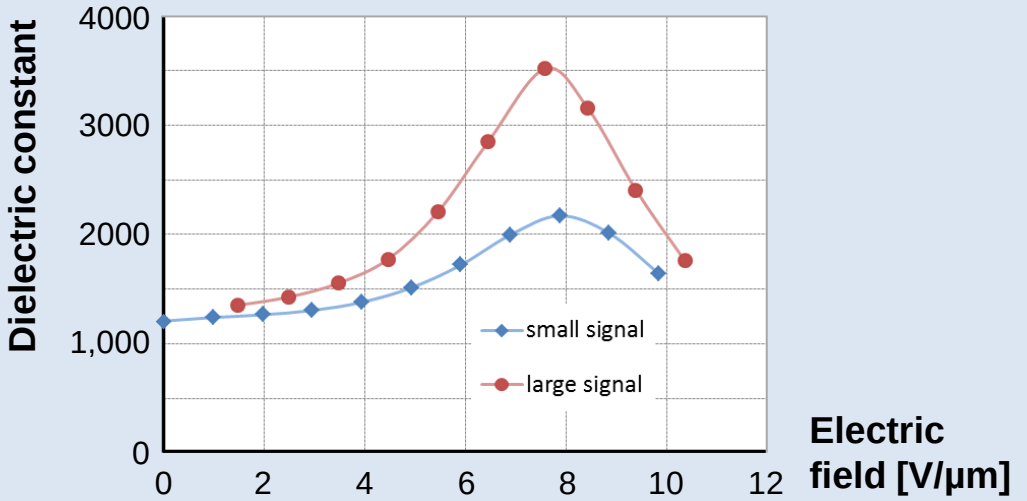
E Electrical field strength

ε Permittivity

High capacitance density at operating condition

- Due to antiferroelectric behavior, the characteristics of CeraLink are strongly non-linear and optimized for conditions under operation in power electronics
- Film capacitors and class 1 ceramics have a dielectric constant (nearly) independent on the electrical field (ε < 100)
- The permittivity of ferroelectric (e.g. X7R) MLCC capacitors is decreasing with electrical field
- CeraLink features an increasing dielectric constant up to the operating voltage
- At higher AC voltage (peaks), the material is able to provide even higher permittivities

DC bias characteristics at room temperature

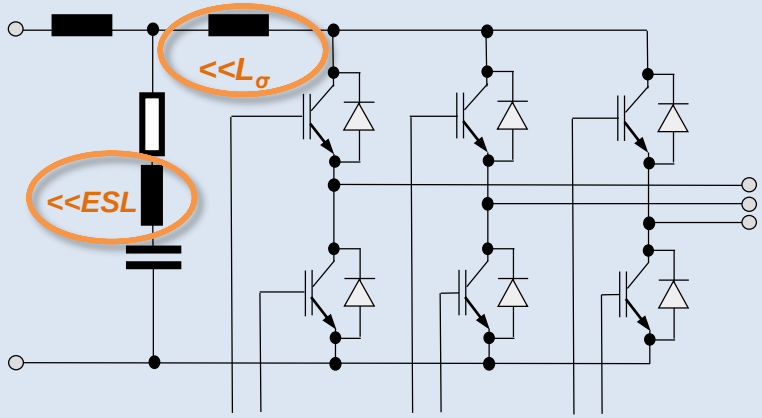


	Film capacitor	Class 2 MLCC	CeraLink	
Nominal / rated capacitance	100 %	100 %	**100 %**	
No bias voltage 0.5 V_{RMS}	100%	100 %	**35 %**	
DC link voltage 0.5 V_{RMS}	100 %	35 %	**60 %**	**DC link (energy)**
DC link voltage 20 V_{RMS}	100 %	35 %	**100 %**	**Snubber**

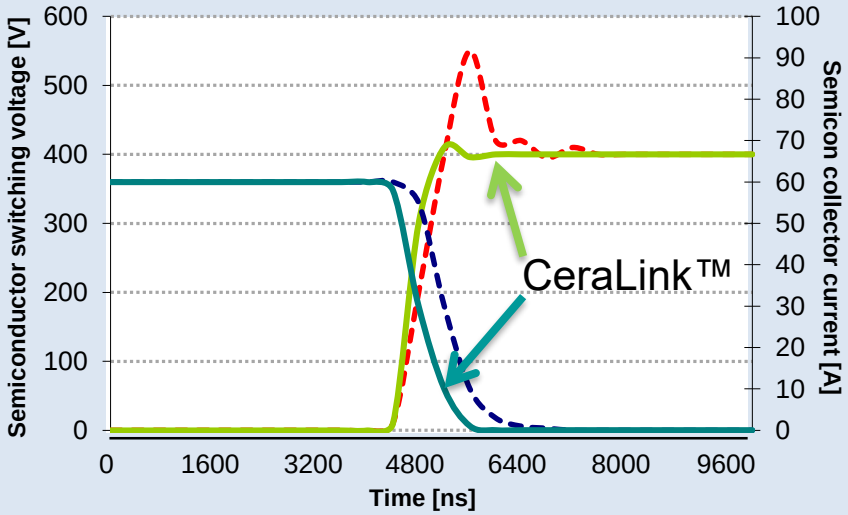
CeraLink is ideal for fast switching

Device characteristics lead to a low inductive commutation loop

- High capacitance density of 2 to 5 µF/cm³
- **Low self-inductance (ESL) of 2.5 to 4 nH**
- High thermal robustness allows CeraLink to be placed very close to the semi-conductor with operation up to 150 °C permissible
- **No limitation of dV/dt**



Semiconductor overshoot principle



Ceramic Chip Features
Design for robustness against ceramic cracks

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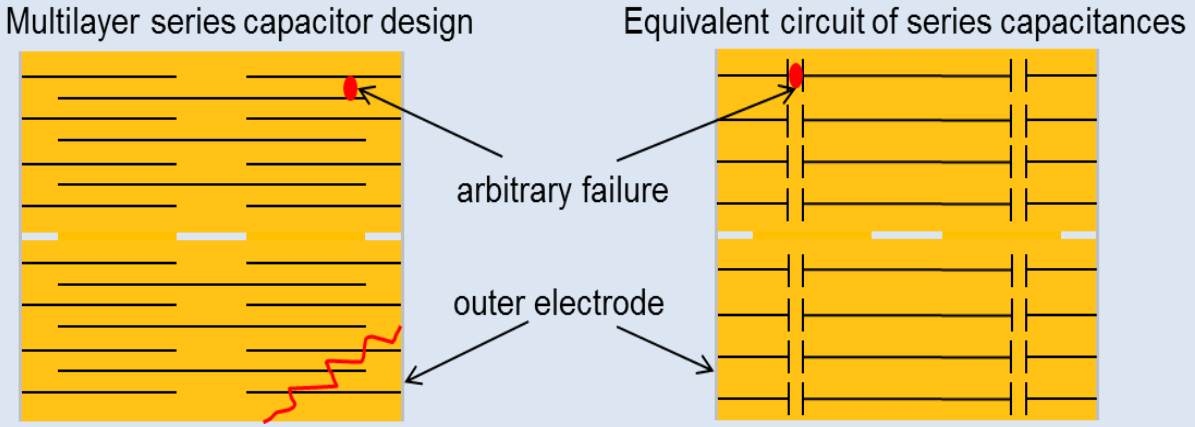
MLSC design

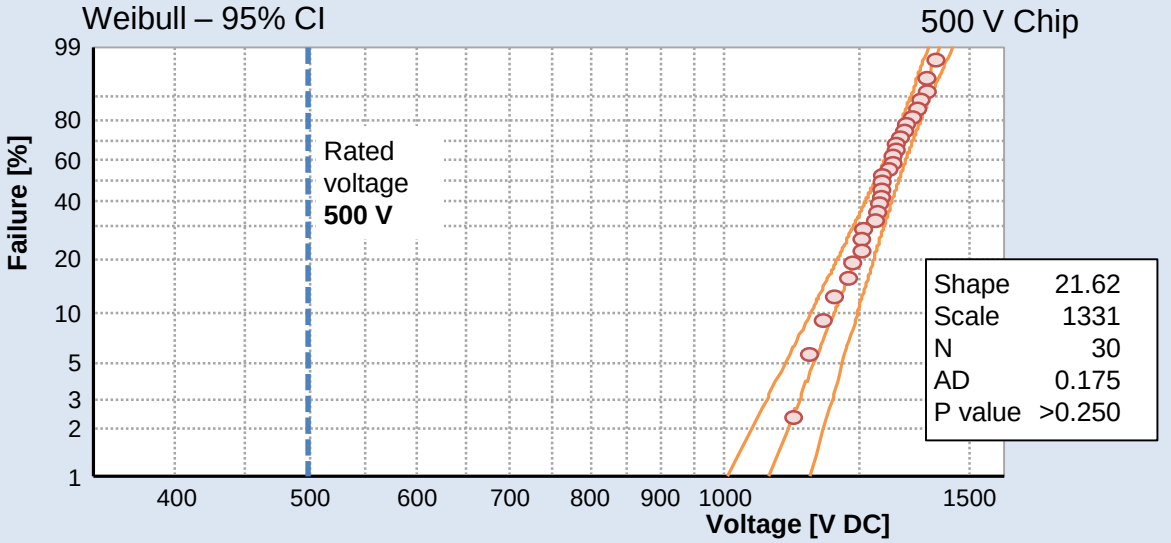
- Series connection of two MLCC geometries in one component.
- **MLSC** design prevents short circuits caused by cracks from mechanical overstress



MFD design

- Chip is segmented in height to reduce piezoelectric stress between active and inactive area

Breakdown voltage measurement



Ceramic chip design for high current capability and high thermal conductivity

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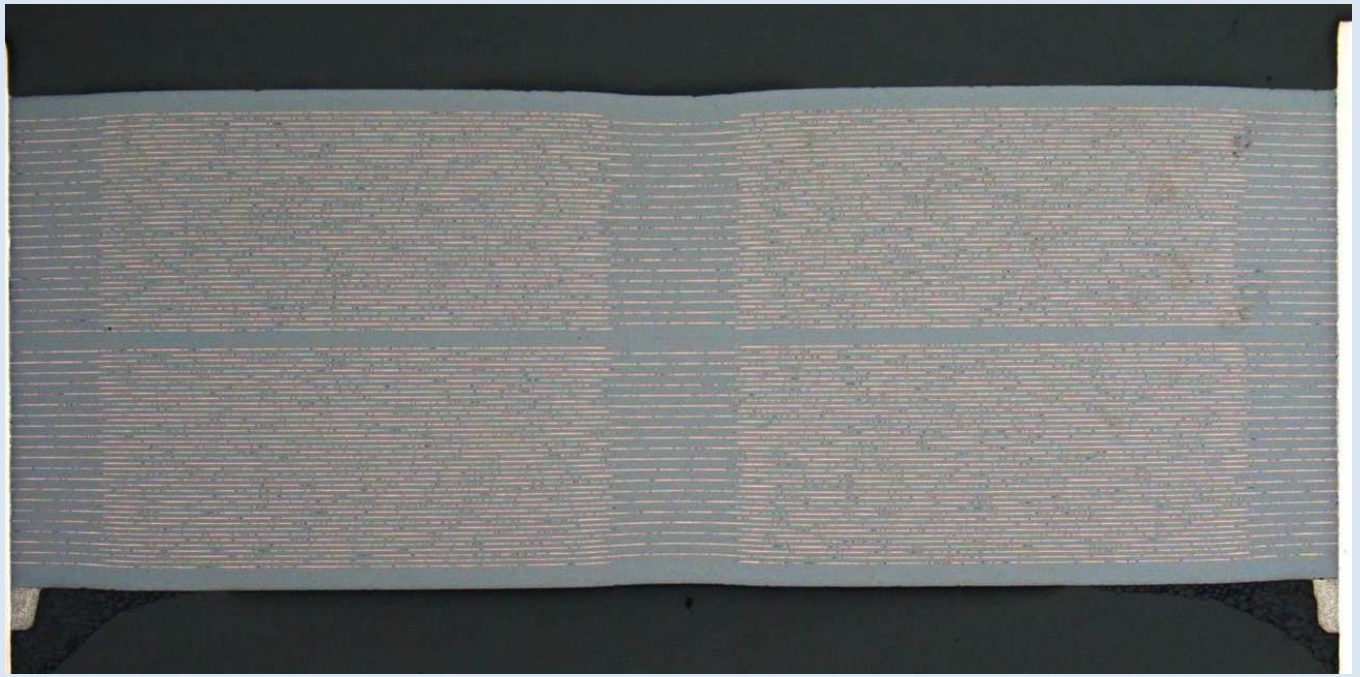
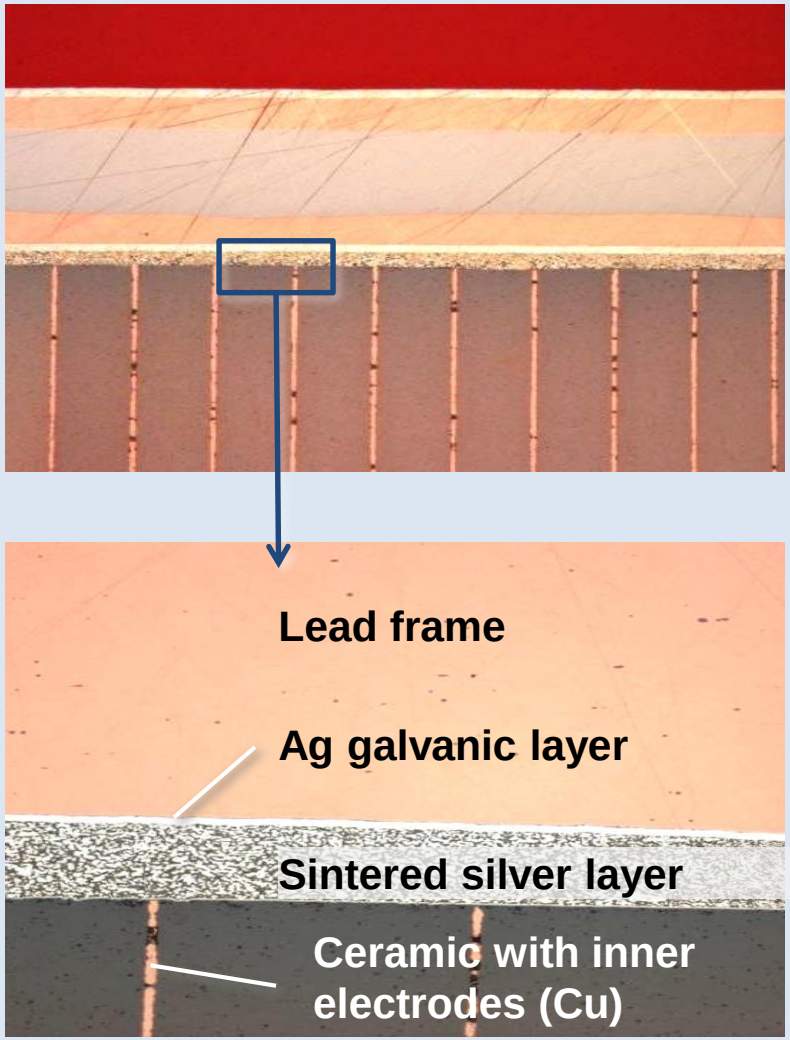
Copper inner electrodes

- Co-firing of PLZT ceramic material together with Cu is difficult, but possible
- Cu – process is one core competence of the piezo mother factory in Deutschlandsberg, Austria

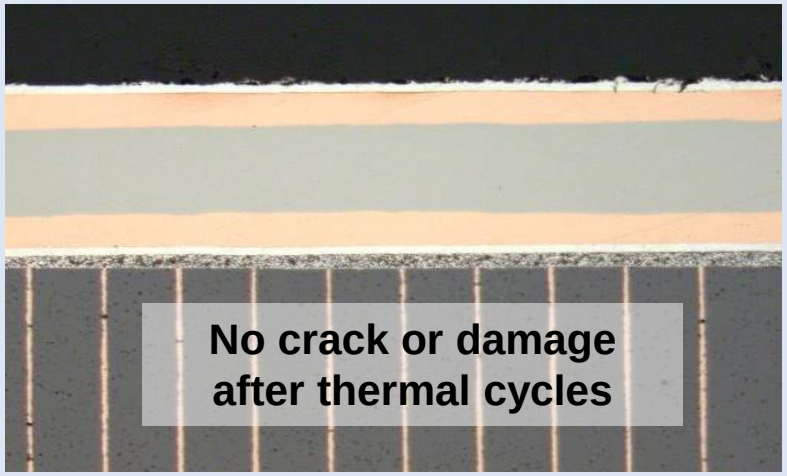


Cross section of the CeraLink multilayer chip consisting of appr. 80 dielectric ceramic layers

Packaging
Robust interconnection of metallic contacts



10,000 cycles thermal shock test
(-55 °C to +150 °C)

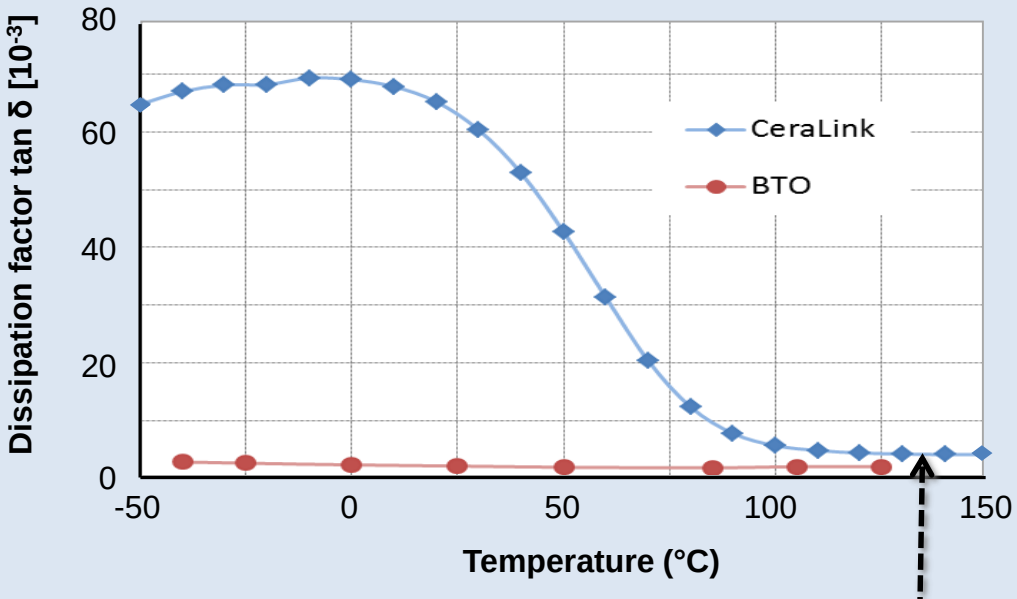


- Silver sinter connection between ceramic body and lead frame
- Outer contacts made of CIC (copper invar* copper), to combine high electrical and thermal conductivity with low coefficient of thermal expansion
- All materials are excellent thermal and electrical conductors (lowest thermal and electrical resistance)
- Silver layer prevents cracking of the ceramic in case of mechanical overstress or solder shock → open mode!

*Invar: 36Ni-Fe

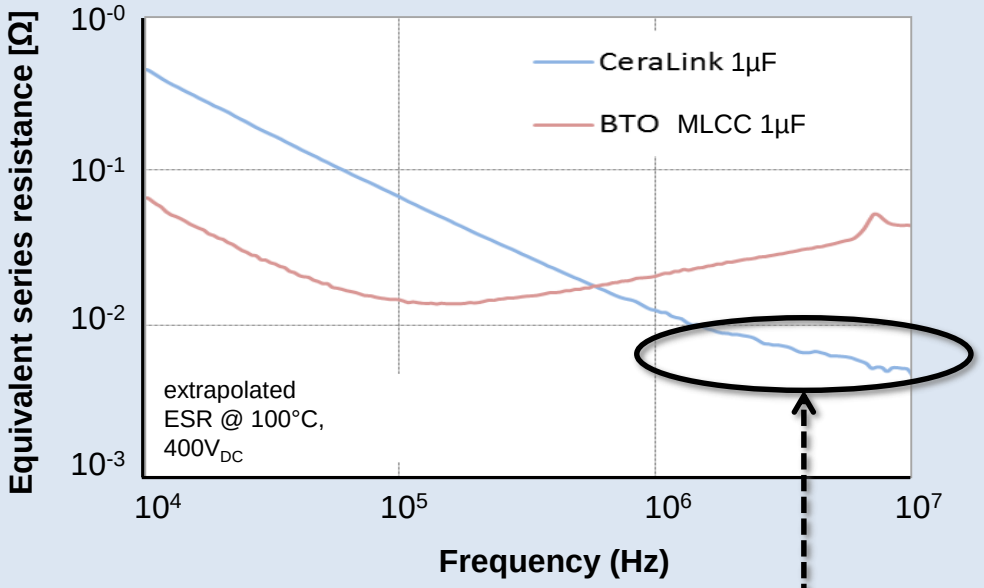
Low losses at high temperatures and frequencies

Comparison @ 1 V_{AC}, 1 kHz, 400 V_{DC}, 25 °C



Low dielectric loss at high temperatures

Comparison @ 0.1 V_{AC}, 0 V_{DC}, 25 °C



Minimal ESR due to low-loss copper electrodes and HF-suited backend

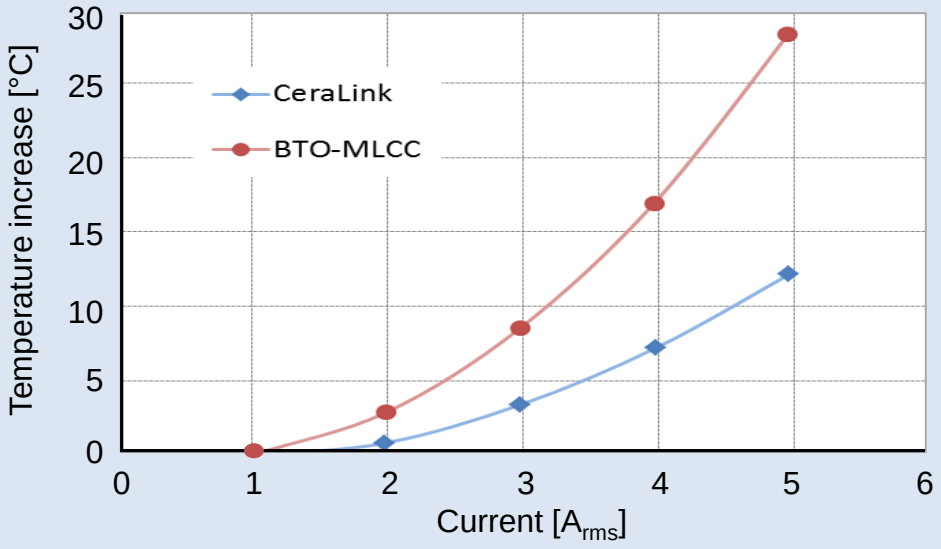
BTO = barium titanate oxide = standard MLCC material

Low self-heating and high current capability

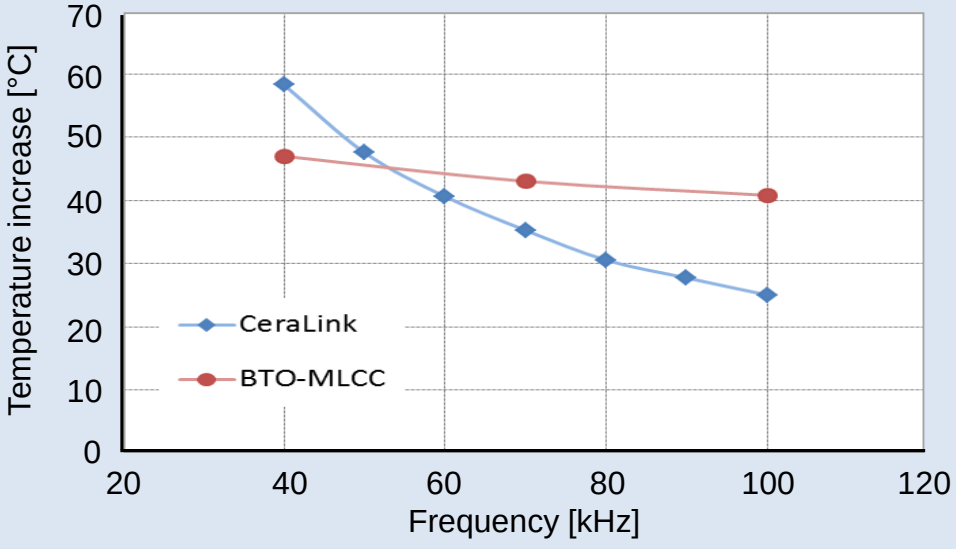
Due to low losses at high temperature and high frequency, CeraLink can carry more current under these conditions

Measurement condition	MKP film capacitor	BTO Class 2 MLCC	CeraLink
Typical capacitance density @ DC link voltage, 20 V_{RMS}, 25 °C	0.7 µF/cm³	2.5 µF/cm³	**4.9 µF/cm³**
Typical current rating per capacitance @ 100 kHz, 105 °C	< 1 A/µF	< 4.5 A/µF	**12 A/µF**

Comparison @ 400 V_{DC}, 105 °C, 200 kHz

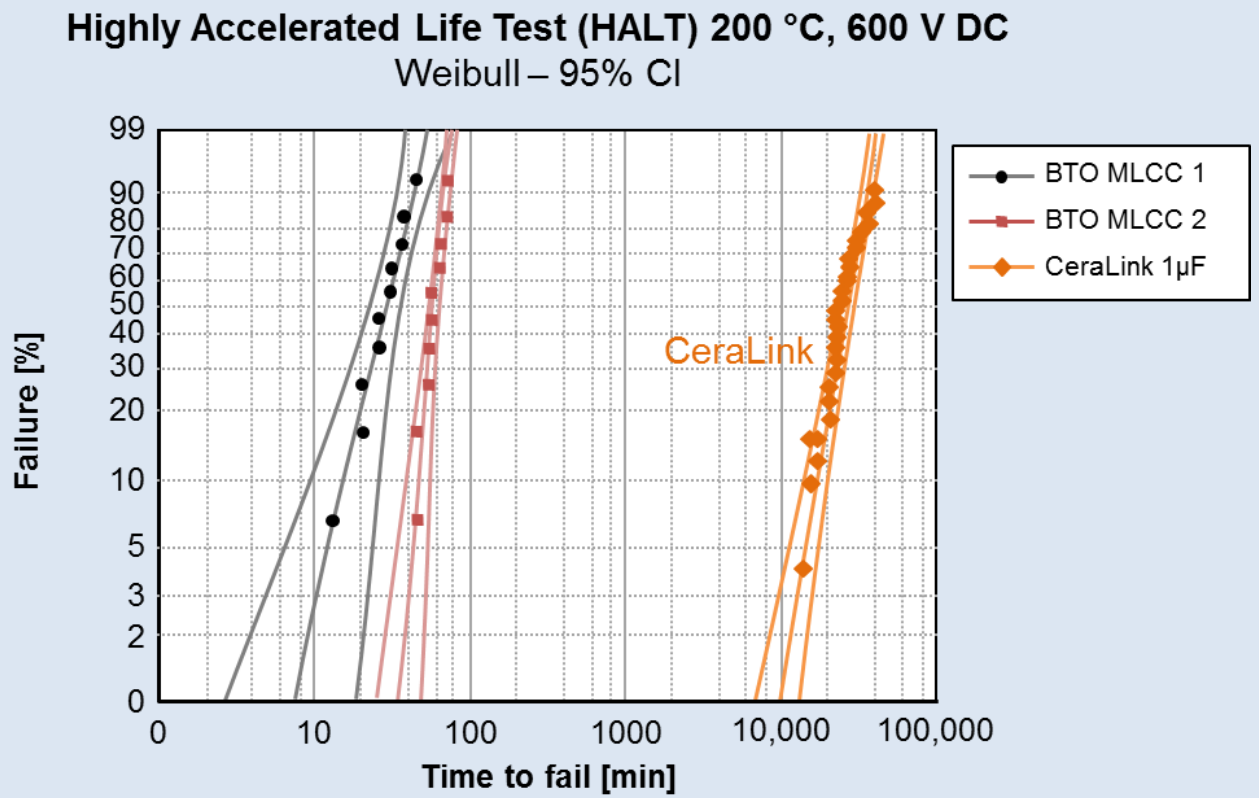


Comparison @ 400 V_{DC}, 85 °C, 5 A_{rms}



Measurements were carried out without active cooling (no forced air flow, no heat sink)

Exceptional lifetime at high temperatures



Lifetime @ 200 °C three orders of magnitude higher than that of conventional ceramic capacitors

Lifetime at high temperatures – comparison of ceramic capacitors

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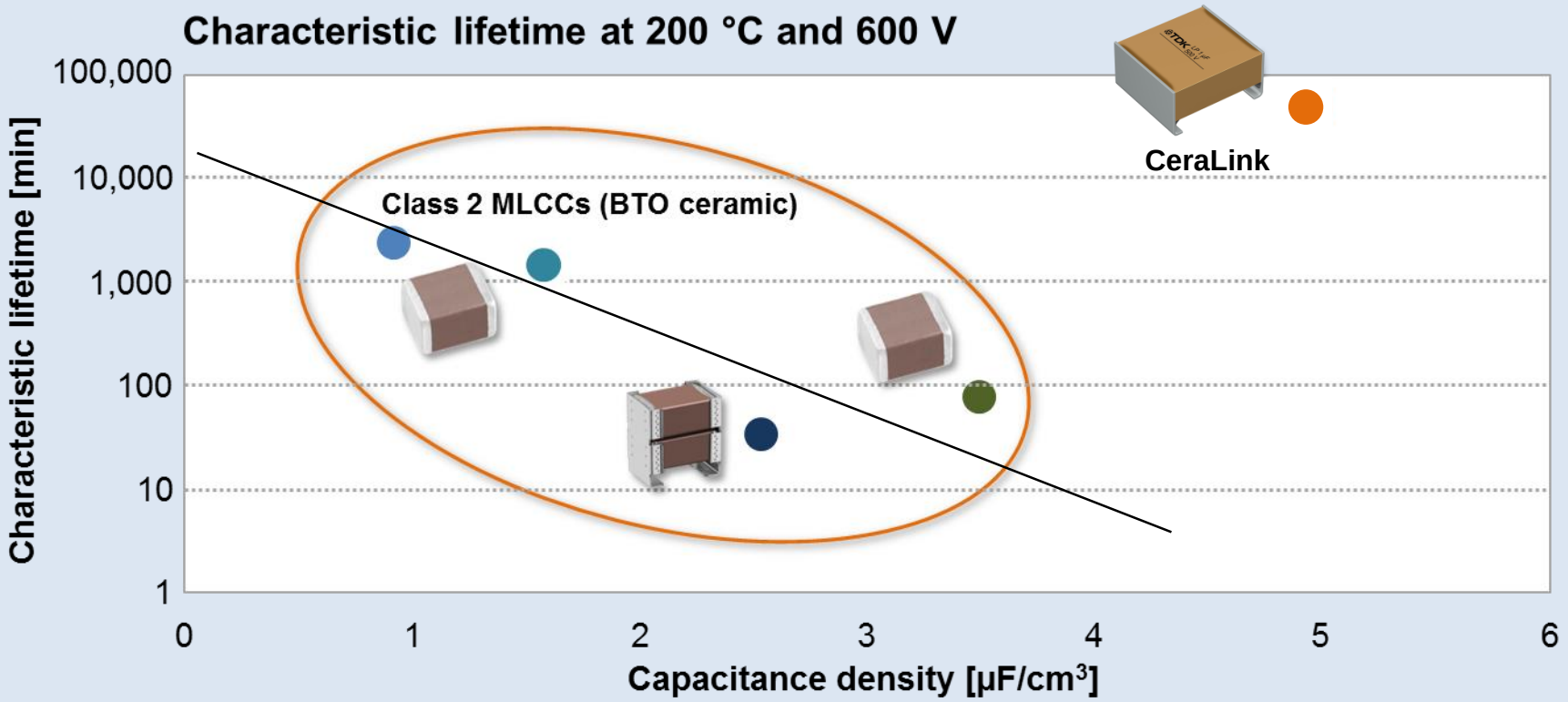


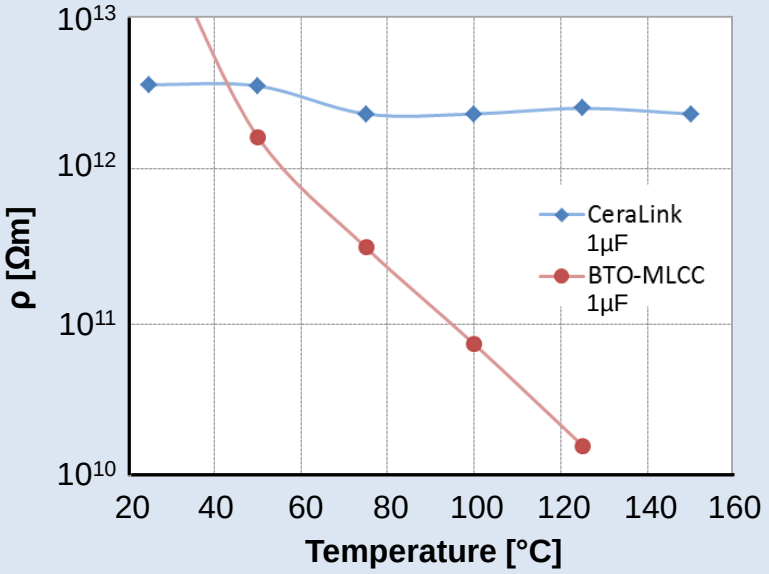
CeraLink offers highest lifetime and capacitance density compared to conventional ceramic capacitors

Low leakage current at high temperatures

CeraLink shows stable and outstanding high isolation properties compared to all existing capacitor technologies

- low leakage current at elevated temperatures even above 150 °C
- No thermal runaway observed for CeraLink ceramic material

Comparison @ 400 V_{DC}



Parallel capacitors
No thermal runaway

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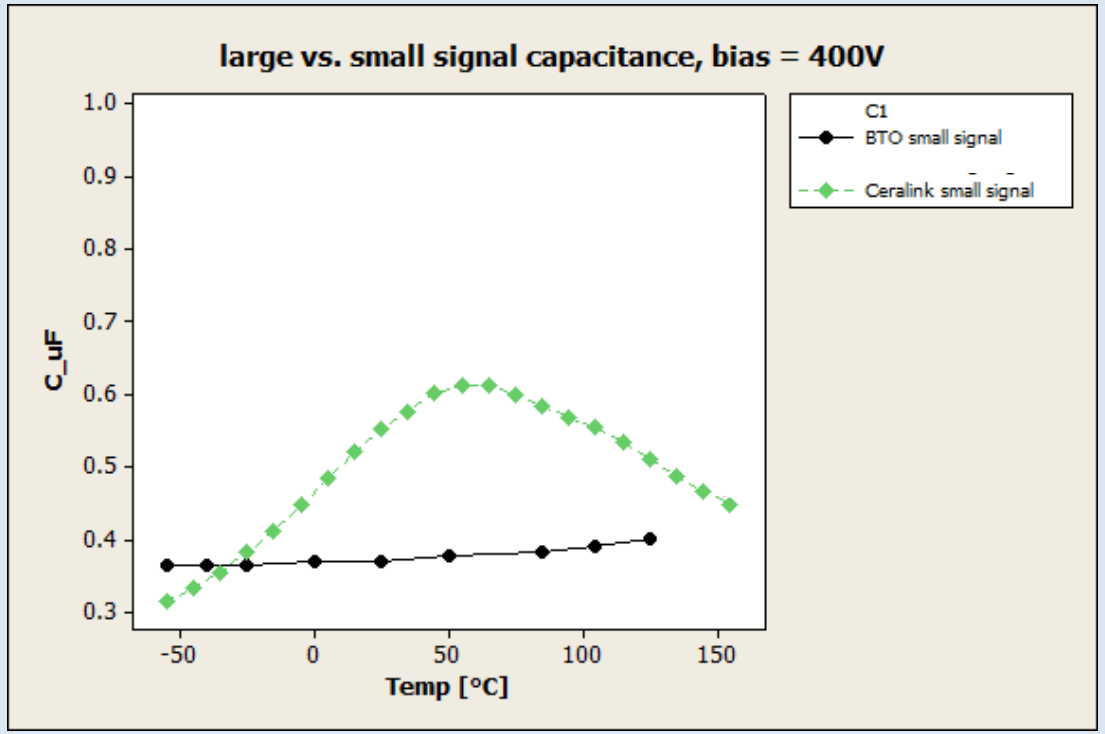
The capacitance characteristic and low ESR of CeraLink avoid a thermal runaway:

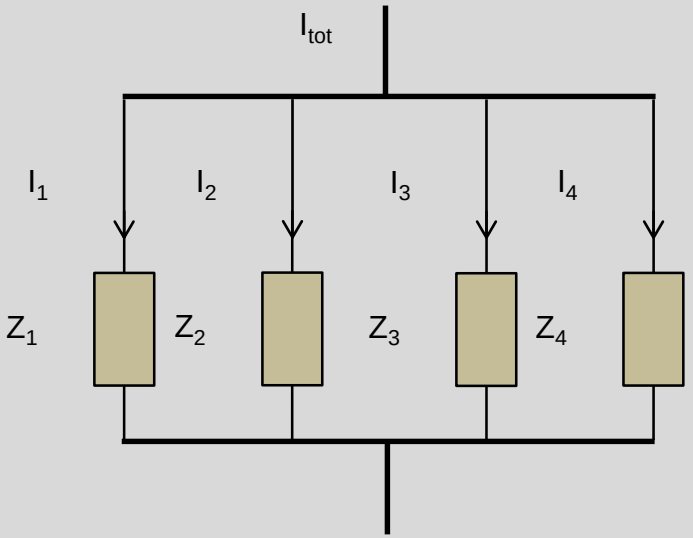


Green: CeraLink small signal capacitance measurement (0.1 V_{rms}, 1 kHz)

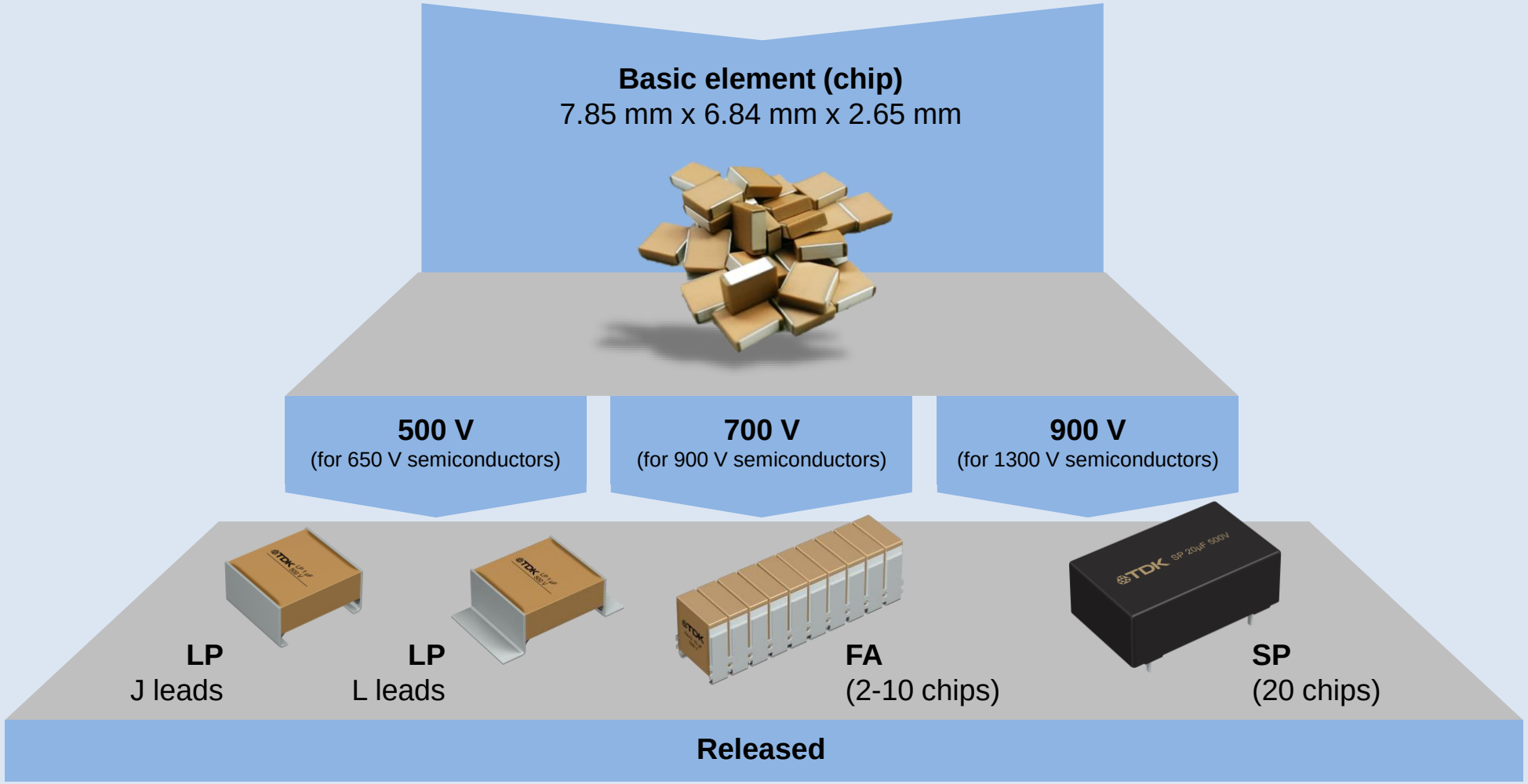
Black: TDK Megacap 1 µF 630 V → measurement (0.1 V_{rms}, 1 kHz)

Higher temperature leads to:

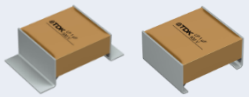
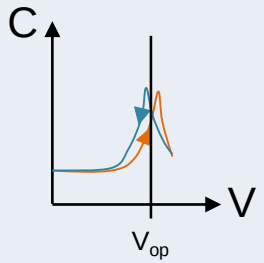
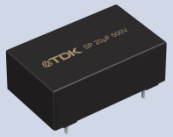
- Lower capacitance
- Higher impedance
- Lowest current through the **hottest** capacitor



CeraLink Product portfolio – modular design



CeraLink product range

Series	Maximum voltage ratings			Features
	650 V	900 V	1300 V	
Low Profile **LP (L /J leads)** 	**1 µF / 500 V**	**0.5 µF / 700 V**	**0.25 µF / 900 V**	Innovative anti-ferroelectric ceramic material  Use CeraLink when • Temperature is demanding (+150 °C) • High current rating is vital • Requirements for capacitance density are tough • High switching frequencies are applied (SiC, GaN) Qualified based on AEC-Q200 and RoHS compliant
Flex Assembly **FA2 / FA3** 	**2/3 µF / 500 V**	**1/1.5 µF / 700 V**	**0.5/0.75 µF / 900 V**	
Flex Assembly **FA10** 	**10 µF / 500 V**	**5 µF / 700 V**	**2.5 µF / 900 V**	
Solder Pin **SP** 	**20 µF / 500 V**	**10 µF / 700 V**	**5 µF / 900 V**	

Application examples
Integrated servo drive

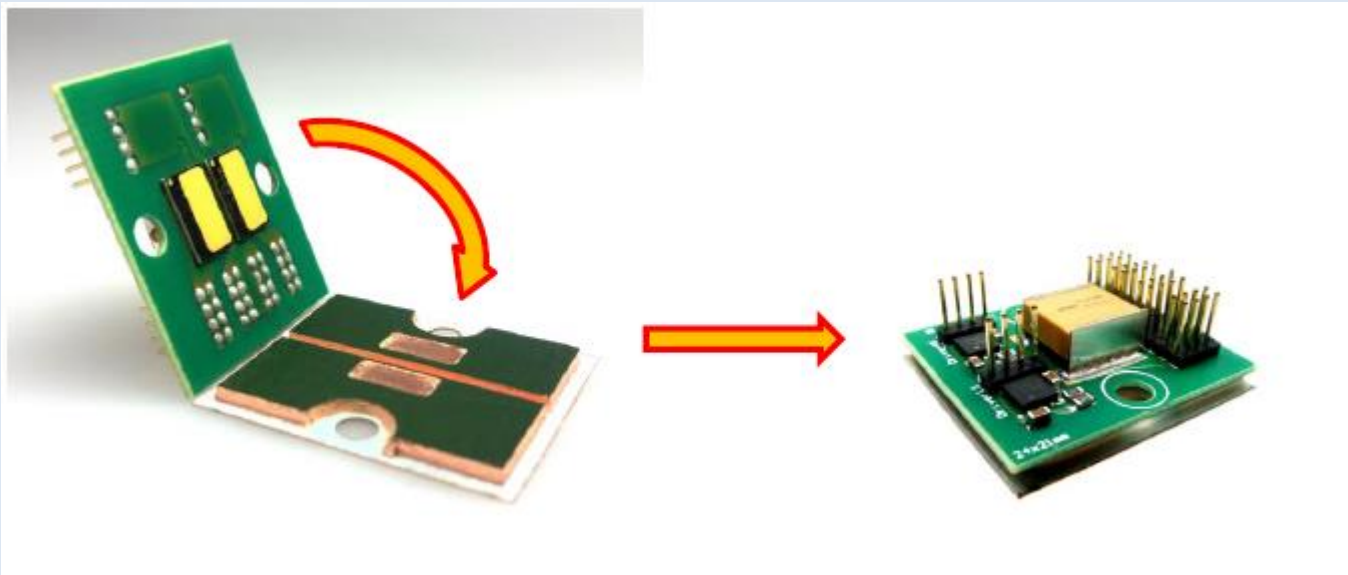
Traditional design

Integrated servo drive

Temperature

Low ESL

GaN power module with integrated driver and DC-Link capacitor



- 1x CeraLink LP 500 V, 1 µF → low inductive commutation loop ~3nH
- 2x integrated driver for 2x GaN systems 650 V

CeraLink as DC-Link capacitors

- Supports **miniaturization** with low inductive design
- Supports **fast-switching GaN** and high switching frequencies

Source: Fraunhofer IZM

Application examples
Onboard chargers

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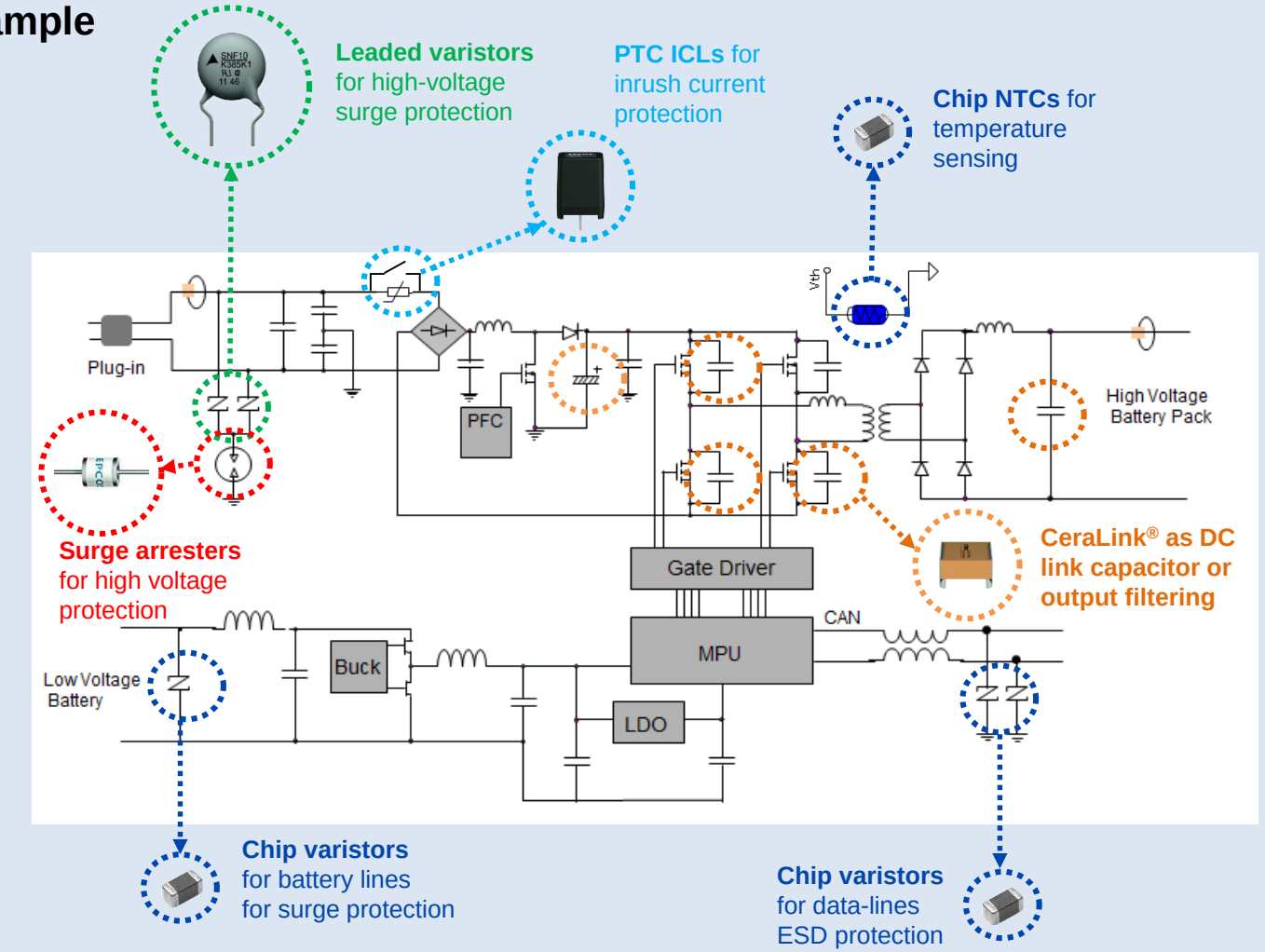
Example



Recommended products (selection)

1. **Chip NTCs (thermal sensing against overheating)**
   - B57232V5103+360
   - B57332V5103+360
   - NTCG164LH104H
2. **Chip varistors (ESD protection for data lines)**
   - CT0402S17AG
   - CT0603L25HSG
   - AVRM1608C270MT*
3. **Chip varistors (low voltage surge protection)**
   - CT0805S14BAUTOG
   - CT1206S14BAUTOG
   - CT2220K30G
   - AVRM2012C390KT6AB
4. **Leaded varistors (high voltage surge protection)**
   - SNF14K***E2K1
   - SNF20K***E2K1
5. **Surge arresters (high voltage protection)**
   - EHV6*-H…B1-B7
   - EHV60-H…SMD
6. **PTC ICLs (inrush current protection)**
   - J21x series
7. **CeraLink® (DC link capacitor or output filtering)**
   - **B58031***
   - **Flex Assembly FA2 or FA3**

CeraLink as Snubber

1 per half bridge - *mounted close to the semiconductor*

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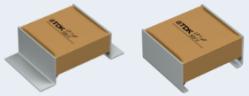
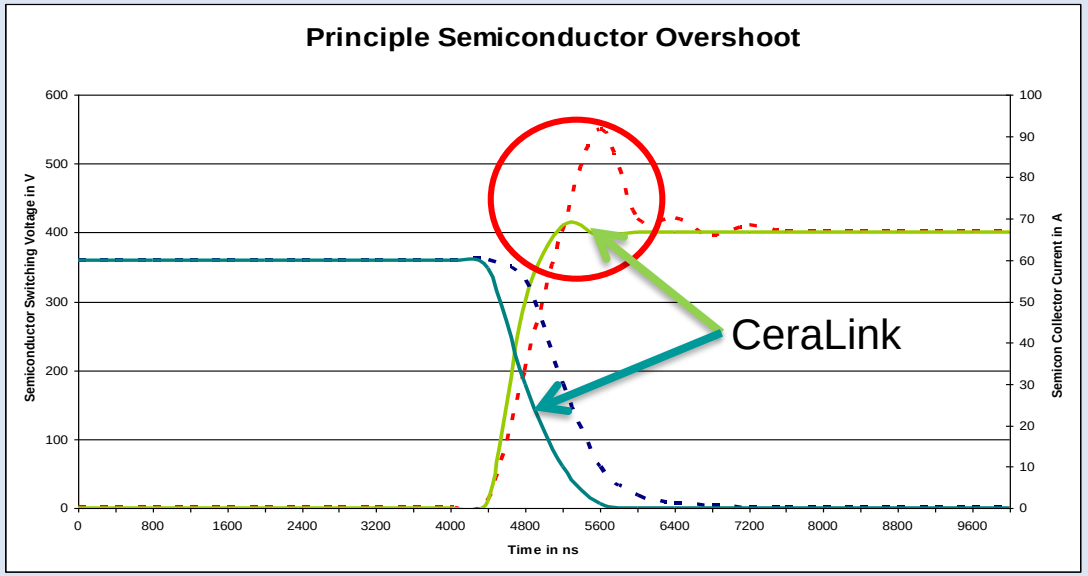
Series	Maximum voltage ratings			Features
	650 V	900 V	1300 V	
Low Profile **LP (L /J leads)** 	**1 µF / 500 V**	**0.5 µF / 700 V**	**0.25 µF / 900 V**	• Low ESL (typ. 3 nH) • Low losses at high frequencies and high temperatures (up to +150 °C) • No limitation of dV/dt
Flex Assembly **FA2 / FA3** 	**2/3 µF / 500 V**	**1/1.5 µF / 700 V**	**0.5/0.75 µF / 900 V**	

Over-voltages or over-shoots occur when switching off a Semiconductor.
This will cause an overvoltage according the formula (see left)
The low inductance of the CeraLink enables a faster switching of the semiconductor resulting in lower switching losses, enabling a reduction of switching losses of up to **40%**!

$$V = -L \cdot \frac{di}{dt}$$



Application examples
Ideal for demanding applications

Attracting Tomorrow

TDK

Motor sports

Power supplies for medical equipment

Test & measurement

Electric aircraft

Down-hole power supplies (gas & oil)

Traction (SiC)

Temperature

Robust Design

Low weight
Small size

Outlook:
Chip CeraLink 2220 in development

Attracting Tomorrow TDK

	TDK MLCC Height: 2.5 mm	CeraLink 2220 Height: 1.4 mm	
Capacitance @ 0 V DC, 25 °C	470 nF	60 nF	✘
Capacitance @ 400 V DC, 25 °C	183 nF	110 nF	✘
Capacitance @ 400 V DC, large signal, 25 °C	183 nF	220 nF	✓
Size [l x w x h]	5.7 x 5 x 2.5 mm	5.6 x 4.7 x 1.4 mm	✓
Capacitance density @ 400 V DC (400 V DC large signal)	2.57 µF/cm³	3.4 (6.6) µF/cm³	✓
T_{max}	125 °C	150 °C	✓
I_{rms} @ 100 kHz*	2.1 A_{RMS}	4.0 A_{RMS}	✓

* T_{amb} = 85 °C / f = 100 kHz / VDC = 400V / calculated from I_{rms} = 3 A and device temperature after 15 min

Target:
CeraLink 2220
2220 200 nF 500 V
Standard termination

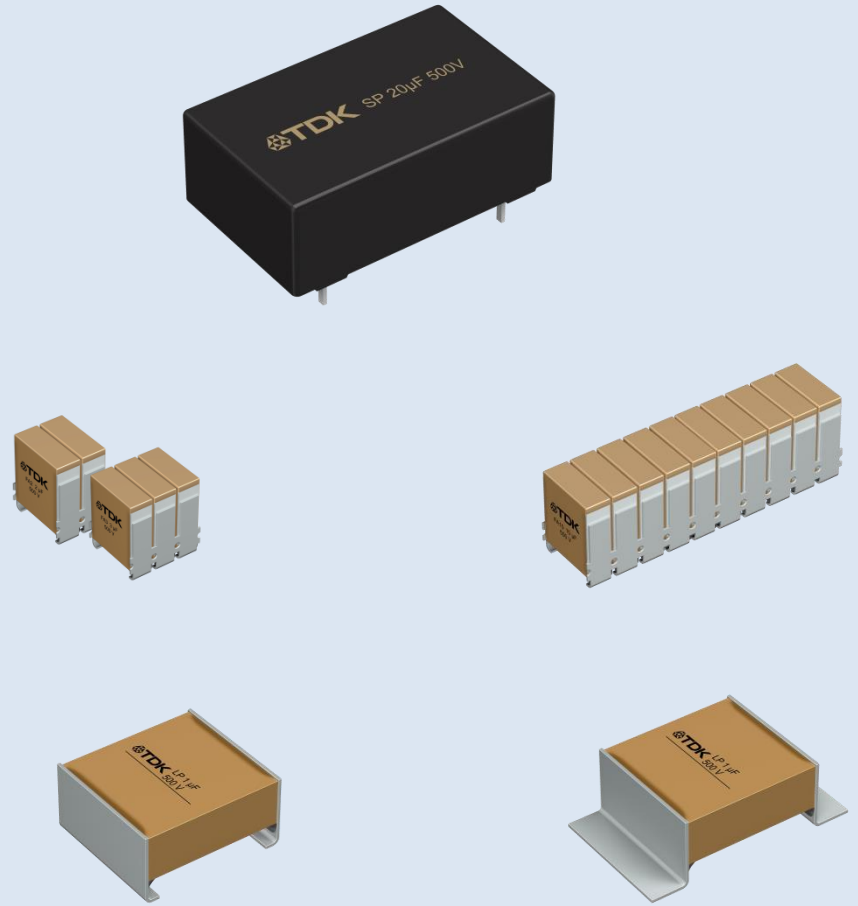
Benchmark MLCC:
C5750X7T2J474K250KC
2220 470 nF 630 V
Standard termination

- Optimized for capacitance density (MLCC design)
- No stress-relief layer necessary for 1 mm active packet (1.4 mm chip height)
- Termination: Cu cap with Ni/Sn galvanics

Summary

Key benefits of CeraLink®

- Effective capacitance increases with rising voltage and leads to **high capacitance density**
- **Low ESL** and low inductive connection
- **Low ESR** especially at high frequencies and high temperatures
- **High current density**
- **High operating and peak temperatures** with temperature excursions up to 150 °C
- **High robustness against high temperatures**
- Supports **fast-switching semiconductors** and high switching frequencies
- Supports further **miniaturization** of power electronics at the system level



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