CoolSiC™ 650 V G2 MOSFET

The latest generation of silicon carbide (SiC) MOSFETs

About this document

Scope and purpose

This document describes the differences between the earlier generation of CoolSiC™ MOSFETs and the latest CoolSiC™ 650 V G2 silicon carbide (SiC) MOSFET from Infineon.

This application note includes technology parameters and describes the latest and most important additional benefits for designers. Finally, the document provides benchmarking against many available SiC MOSFET vendors in the targeted topologies.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems.

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1 Introduction

CoolSiC™ 650 V MOSFETs have been designed tailored to gain the highest efficiency, especially in hard-switching topologies in which there is a continuous hard commutation of a conducting body diode, such as in the CCM Totem Pole PFC (continuous conduction totem pole power factor correction).

Infineon is continuously working on improving the product performance, increasing system efficiency and giving designers a higher degree of freedom for designing new applications. This new generation of SiC trench MOSFETs address these needs.

1.1 Portfolio

Table 1 CoolSiC™ 650 V G2 MOSFETs portfolio

$R_{DS(on),typ}$ [mΩ]	TO-247-3	TO-247-4	D^2PAK-7
			
50	IMW65R050M2H	IMZA65R050M2H	IMBG65R050M2H
40	IMW65R040M2H	IMZA65R040M2H	IMBG65R040M2H
20	IMW65R020M2H	IMZA65R020M2H	IMBG65R020M2H
15	IMW65R015M2H	IMZA65R015M2H	IMBG65R015M2H
7	IMW65R007M2H	IMZA65R007M2H	IMBG65R007M2H

Table 1 shows the first part of the product roadmap which will continue over the next few years with different packages and further $R_{DS(on)}$ granularity. The next section of this document provides a short introduction of the target applications or precisely the topology that gains more attraction on the market in high-power and lower-power applications such as AI, server, telecom, EV charging, solar, TV, and adapter applications.

For more information on Infineon products, visit www.infineon.com.

1.2 Target topology

This new-generation technology is ideal for various applications in which a continuous hard commutation on a conducting body diode is present. The following sections introduce the applications that provide usage scenarios without limits for designers.

1.2.1 Totem Pole PFC

The principle of operation of the CCM Totem Pole PFC is divided into four phases over one AC cycle: two phases for the positive and two phases for the negative cycle of the AC input voltage.

Positive AC line cycle:

The low ohmic superjunction (SJ) MOSFET (SJ2) is in a continuously conducting state. During the magnetizing phase, the SiC MOSFET (SiC2) turns on and operates like in a standard PFC; it is necessary to magnetize the PFC choke. After SiC2 turns off, the body diode of SiC1 conducts. Finally, SiC1 actively turns on and the demagnetizing phase starts. During this time, SiC1 acts as a synchronous boost. Exactly during the time when synchronous boost turns off, there is a short period in which the body diode of SiC1 is conducting again and SiC2 actively turns on, leading to a hard commutation on the conducting body diode. It means that this hard commutation is present in every switching cycle on one of the SiC MOSFETs. Therefore, the switching energy and the losses increase during this turn on based on the Q_{fr}.

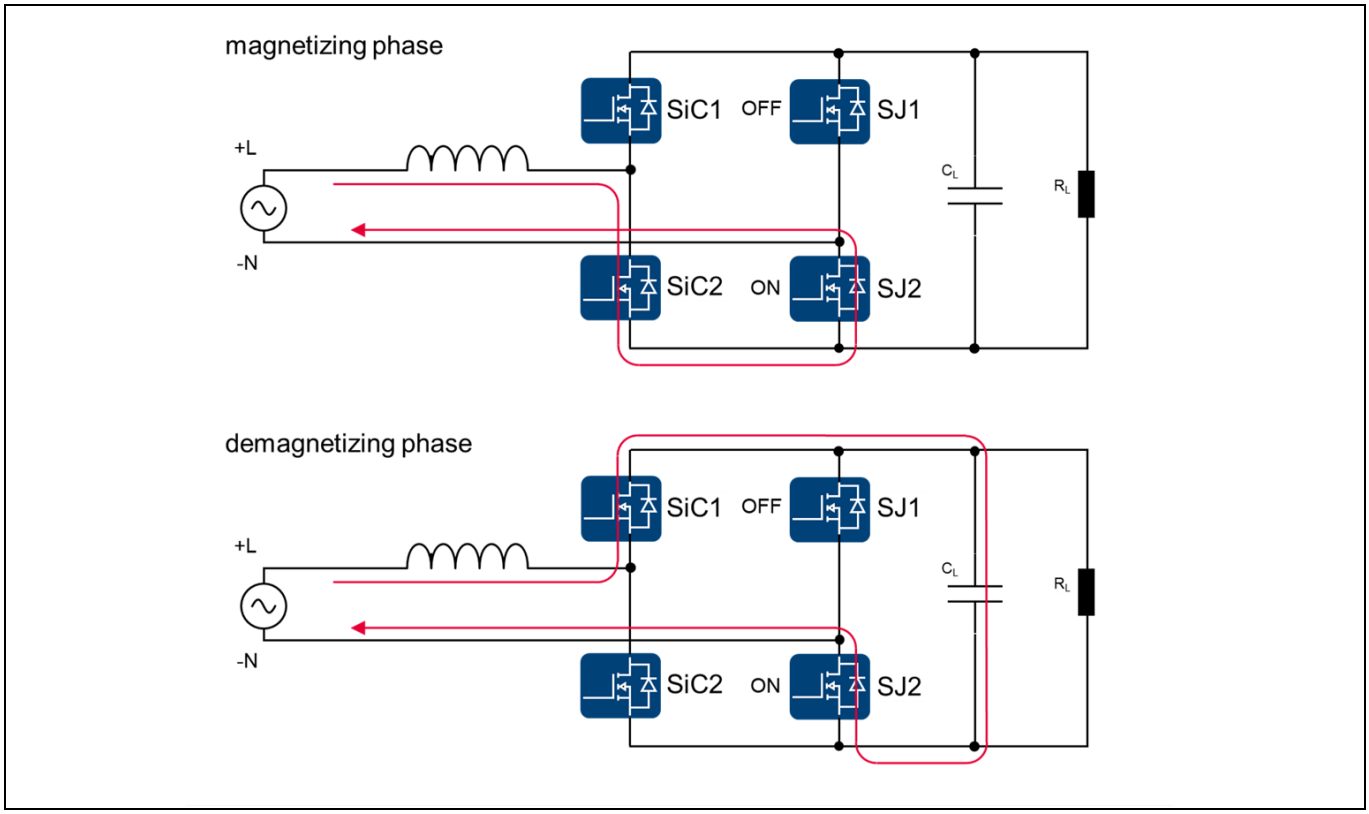

Figure 1 Operation principle of positive AC line cycle

Negative AC line cycle:

The negative AC line cycle operation is the same as the inverted positive AC line cycle. In this case, the low ohmic SJ MOSFET (SJ1) is in continuously conducting state. During the magnetizing phase, the SiC MOSFET (SiC1) turns on and operates like in a standard PFC; it is necessary to magnetize the PFC choke. After SiC1 turns off, the body diode of SiC2 conducts. Finally, SiC2 actively turns on and the demagnetizing phase starts. During this time, SiC2 acts as a synchronous boost. As seen in this topology, the lowest possible Q_{fr} is required during every switching cycle; there is a hard commutation on the conducting body diode.

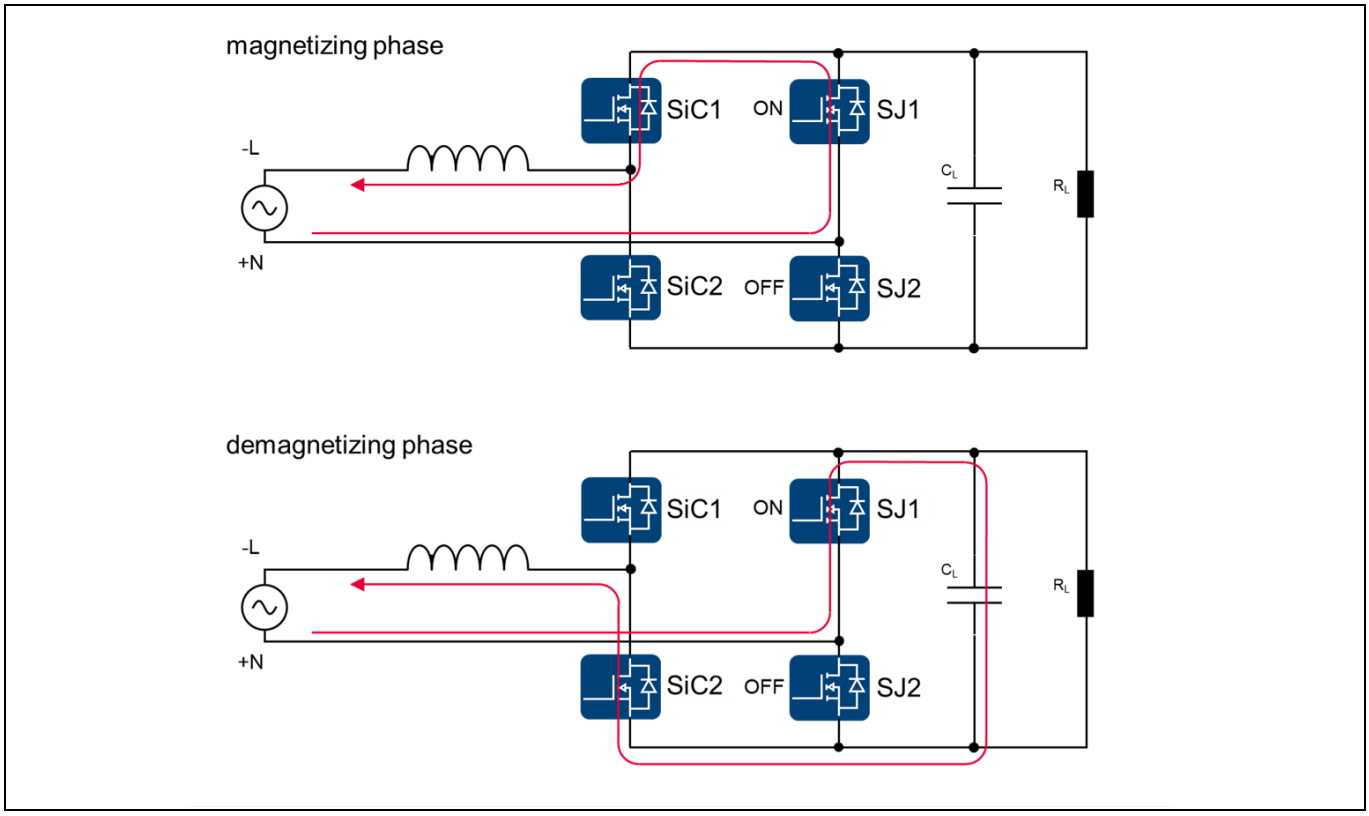

Figure 2 Operation principle of negative AC line cycle

Therefore, the SiC MOSFET and its related technology parameters are the optimum choice for easily achieving 99% efficiency and further increasing the system efficiency in comparison to the first generation.

1.2.2 LLC converter

Due to the low Q_{fr}, CoolSiC™ MOSFETs enable the system to achieve increased system reliability in abnormal operating conditions and during fast changes in switching frequency, e.g., load jumps. Additionally, CoolSiC™ MOSFETs offer higher efficiency and the possibility to boost the switching frequency due to the ease of achieving full zero-voltage switching (ZVS) under any load conditions and/or a reduction of the resonant current can be achieved.

2 Technology parameters

This section describes the most important technology parameters and provides general recommendations for the usage of CoolSiC™ MOSFETs. The comparison is represented for IMBG65R040M2H against IMBG65R039M1H because these products represent the closest $R_{DS(on)}$.

2.1 $R_{DS(on)}$ over junction temperature

In all device datasheets, the typical $R_{DS(on)}$ value is represented at 25°C junction temperature. Usually, the devices operate at higher junction temperatures. Therefore, it is mandatory to know the $R_{DS(on)}$ value at higher temperatures such as at 100°C. The $R_{DS(on)}$ shows a positive temperature coefficient which results in an increased $R_{DS(on)}$ value at higher temperatures.

As shown in Figure 3, the X-axis is the junction temperature and the Y-axis is the normalized $R_{DS(on)}$ value. It is shown that at 25°C the $R_{DS(on)}$ is the same for Gen1 and Gen2 CoolSiC™ MOSFETs. This 25°C value is represented in the datasheets and in the naming convention.

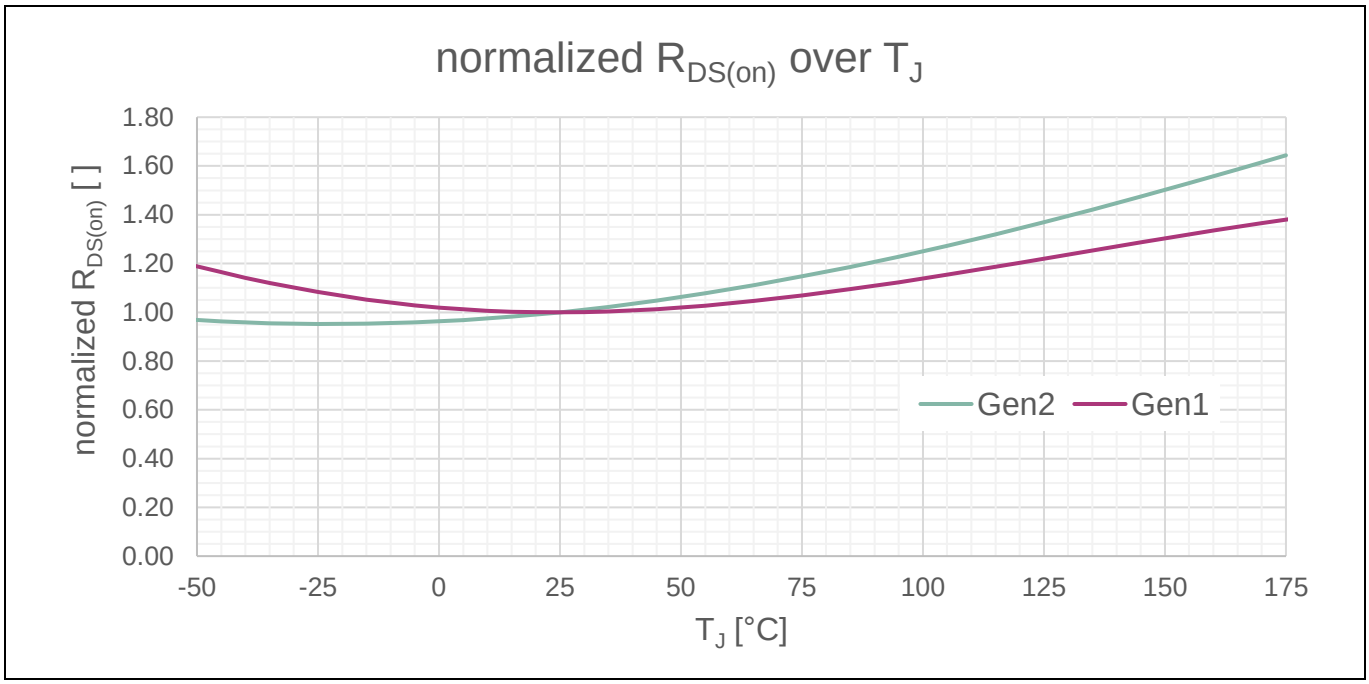

Figure 3 Normalized $R_{DS(on)}$ value over temperature comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

CoolSiC™ Gen2 MOSFETs have a slightly worse behavior than CoolSiC™ Gen1 MOSFETs; however, this little drawback can be completely ignored due to the reduced switching losses from CoolSiC™ Gen2 MOSFETs, allowing CoolSiC™ Gen2 MOSFETs to be still better in efficiency than CoolSiC™ Gen1 MOSFETs in the target applications (described in a later section of this document). Furthermore, this behavior is the result of a channel improvement. Therefore, the $R_{DS(on)}$ distribution is shifted to the drift region of the device, resulting in an increased process stability leading to a reduction of the required typical to maximum $R_{DS(on)}$ margin in the final datasheets for CoolSiC™ Gen2 MOSFETs.

2.2 Q_{fr} – MOSFET forward recovery charge

Note that CoolSiC™ Gen2 MOSFETs use a different nomenclature for the body diode recovery parameters from CoolSiC™ Gen1 MOSFETs. The old nomenclature of Q_{rr} is not sufficient to explain the values which are represented as from the standards perspective; Q_{rr} represents the reverse recovery charge only. During the measurement of the reverse recovery charge also Q_{oss} is in place for the active switch. It means that the value in the datasheet of Q_{fr} is the sum of Q_{oss} and Q_{rr}. Figure 4 shows the difference in nomenclature and definition.

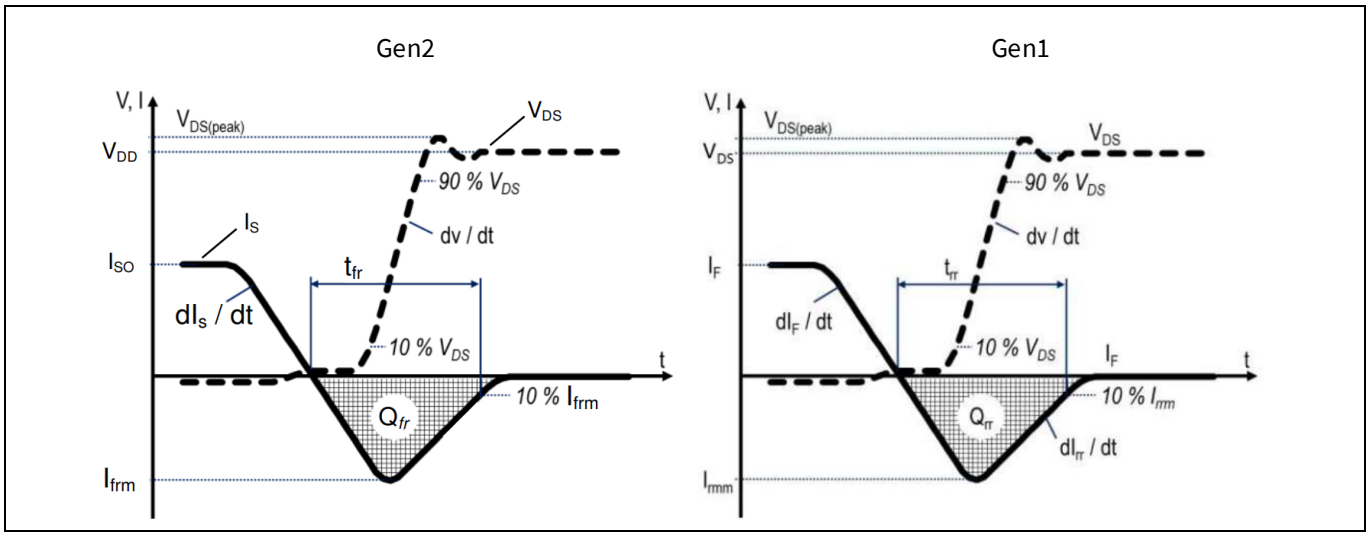

Figure 4 MOSFET diode recovery waveform comparison CoolSiC™ Gen2 vs. Gen1 MOSFETs

In several CoolSiC™ Gen1 MOSFET datasheets, this nomenclature is already changed to the new definition; this is going to be continued until all CoolSiC™ products are synchronized.

At nearly the same test condition, CoolSiC™ Gen2 MOSFETs have approximately 45% lower Q_{fr} than CoolSiC™ Gen1 MOSFETs.

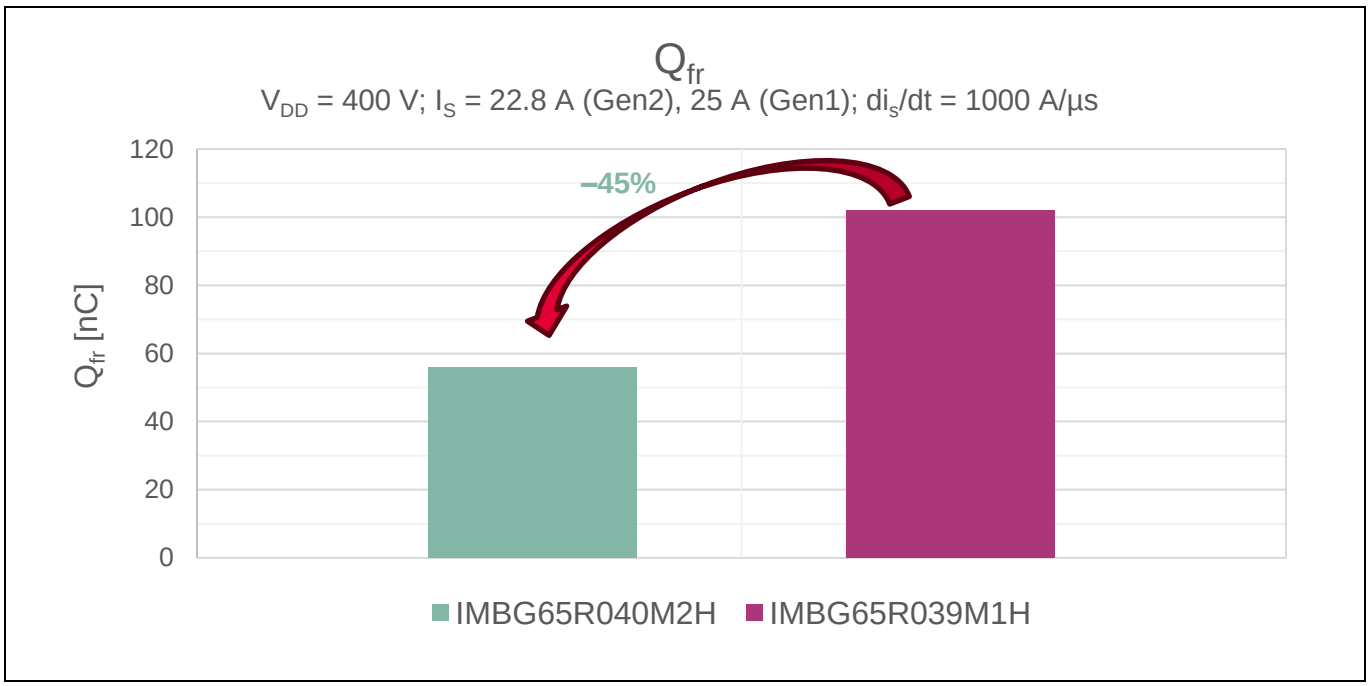

Figure 5 Q_{fr} comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

Figure 5 also implies that the E_{on} losses are dramatically reduced in comparison to CoolSiC™ Gen1 MOSFETs under the same test conditions.

2.3 V_{DSS} – drain-source voltage limit

In general, the behavior of the breakdown voltage from CoolSiC™ Gen2 and Gen1 MOSFETs are equal. The main difference is that CoolSiC™ Gen2 MOSFETs have a lower slope as shown in Figure 6, in which the X-axis corresponds to the junction temperature and the Y-axis represents the voltage breakdown. The key difference is that at lower temperatures, the breakdown voltage is higher for CoolSiC™ Gen2 MOSFETs compared to CoolSiC™ Gen1 MOSFETs, which gives the benefit for customers for outdoor applications or applications which have a startup at lower temperatures. Furthermore, the rated blocking voltage is ≥ 650 V over the whole T_J range.

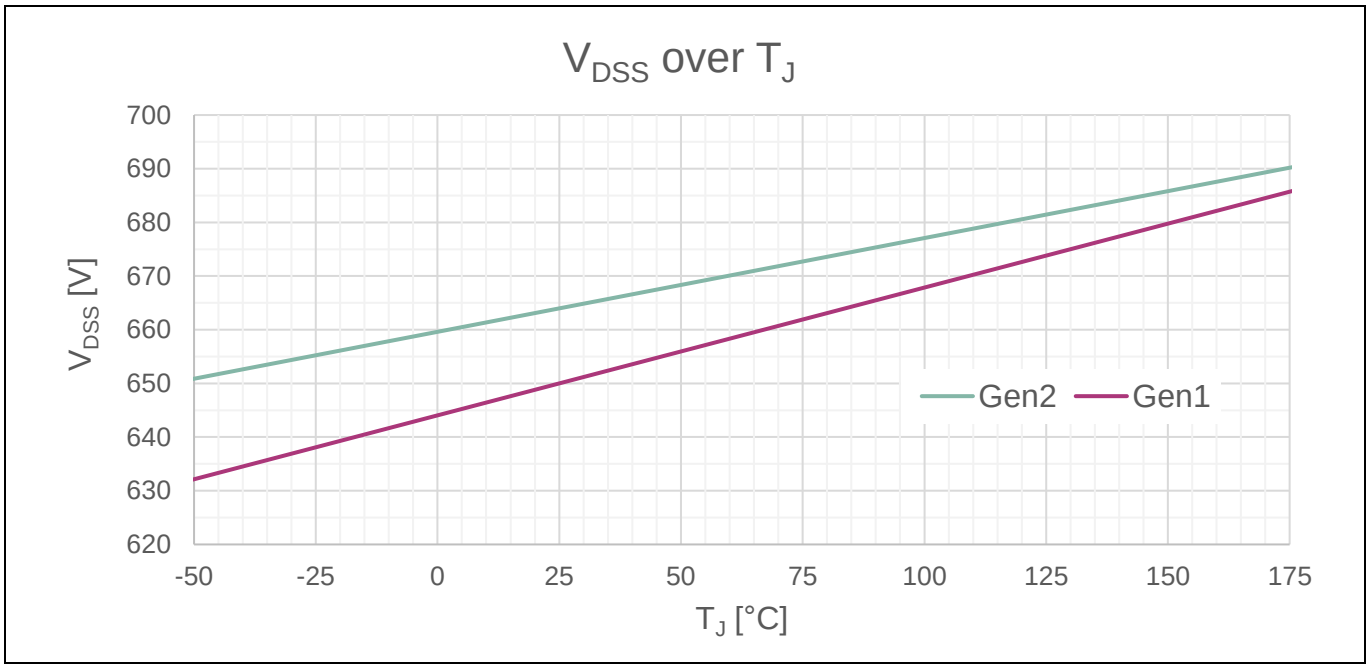

Figure 6 V_{DSS} comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

Note: It is not recommended to apply voltages above the rated breakdown voltage even during switching transients and abnormal operating conditions.

2.4 Transfer characteristics

The transfer characteristics show an important difference related to the driving capability of the new generation. The crossing point between the 25°C (straight line) and the 175°C (dashed line) line is named the “thermal instability point”. Below the thermal instability point, the MOSFET allows a higher current transfer at a higher temperature that can lead to thermal runaway in the application, depending on the applied gate source voltage.

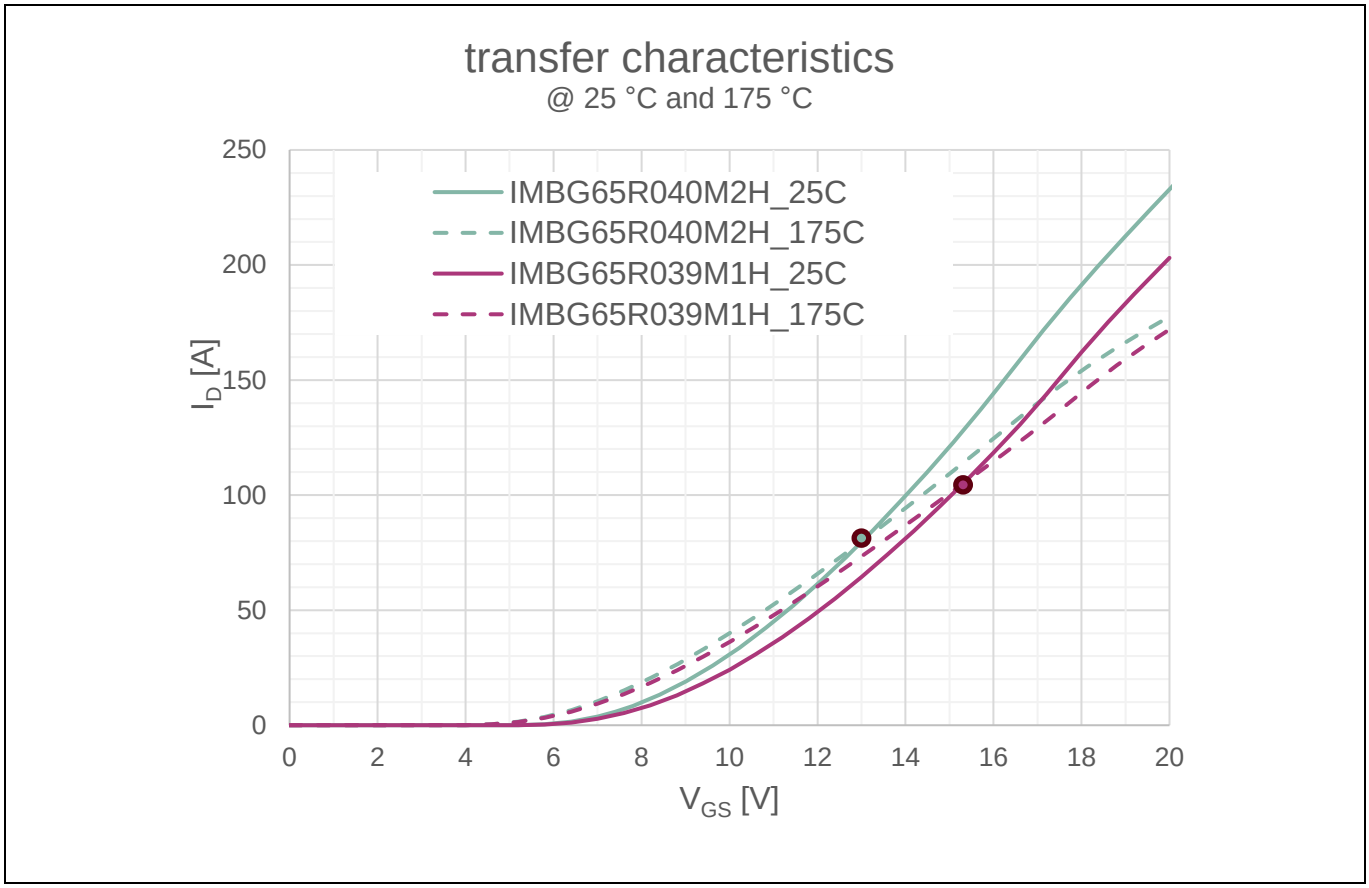

Figure 7 Transfer characteristics comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

For CoolSiC™ Gen1 MOSFETs, the thermal instability point is at V_{GS} = ~15.3 V which makes it possible to operate at 15 V driving voltage, but designers need to take precaution on the thermal runaway during high-current operation. On the other side, the thermal instability point for CoolSiC™ Gen2 MOSFETs is at V_{GS} = 13 V. This results in a full compatible 15 V gate driving. However, Infineon recommends to operate the device with a driving voltage of 18 V because there is an additional $R_{DS(on)}$ benefit of approximately 30%.

2.5 C_{oss} – output capacitance

The output capacitance is an indicator of the present switching losses including the Q_{oss} and the E_{oss}, which are two additional factors influencing the behavior in the application and efficiency.

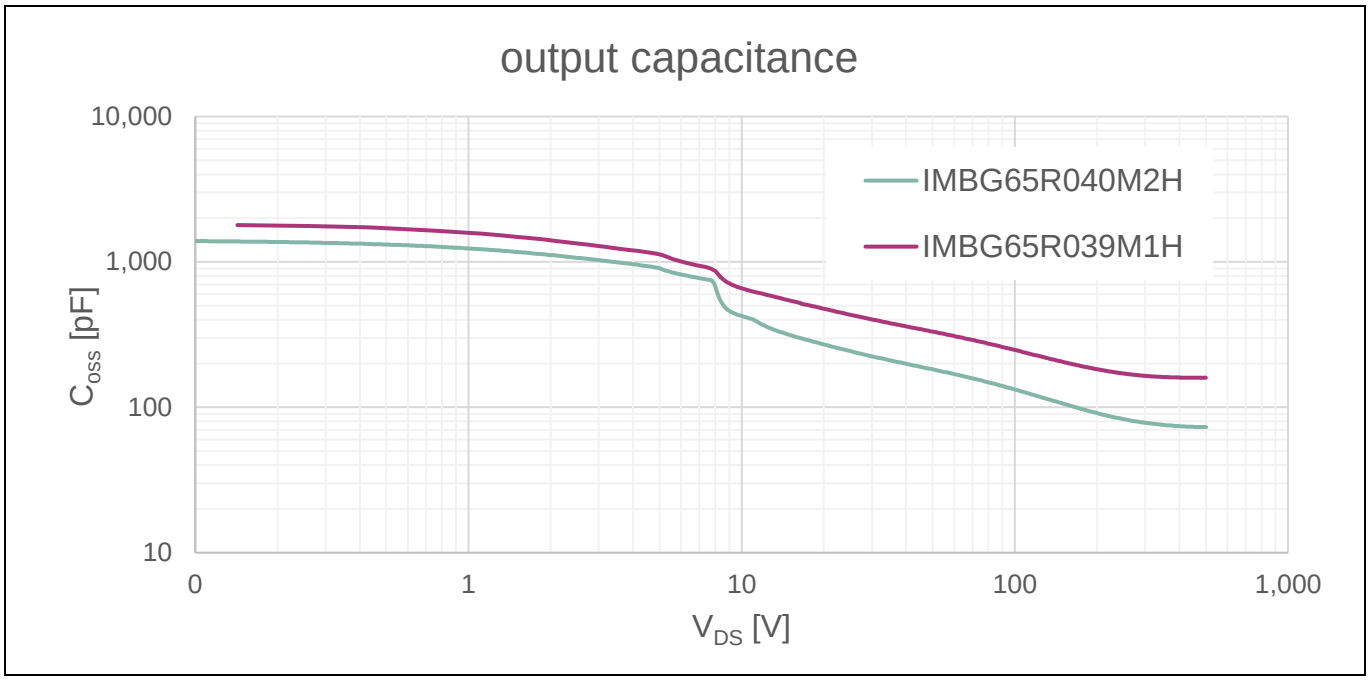

Figure 8 Output capacitance comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

The C_{oss} of CoolSiC™ Gen2 MOSFETs follows the same pattern as CoolSiC™ Gen1 MOSFETs only with a reduced absolute value. At V_{DS} = 400 V, there is a reduction of ~54%. In CoolSiC™ Gen1 MOSFETs, the main drawback is the increased E_{oss} due to the large C_{oss}. Figure 9 compares E_{oss} and Q_{oss} over V_{DS}.

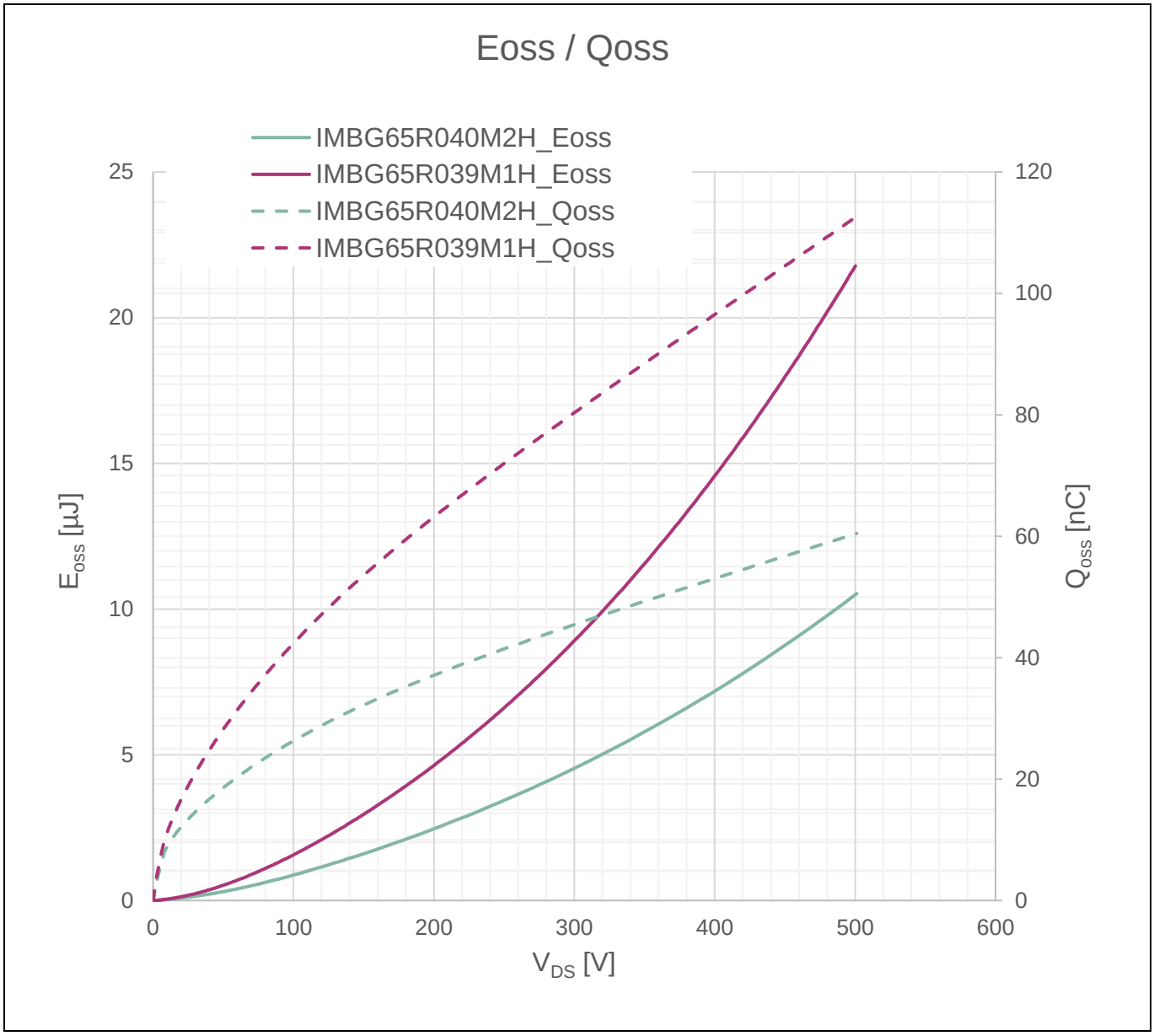

Figure 9 E_{oss} and Q_{oss} comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

As the E_{oss} and the Q_{oss} are derived by the C_{oss} according to the following two equations:

$$E_{oss} = \int_0^{400\,V} C_{oss} \cdot V \, dV$$

$$Q_{oss} = \int_0^{400\,V} C_{oss} \cdot \frac{\mathrm{dV}}{\mathrm{dt}} \, \mathrm{d}t$$

Equation 1 Calculation of E_{oss} and Q_{oss}

The benefit of the lower C_{oss} over the whole voltage range of CoolSiC™ Gen2 MOSFETs is that E_{oss} and Q_{oss} show the same behavior with a reduction of 45 – 50% in comparison to CoolSiC™ Gen1 MOSFETs.

2.6 Q_G – gate charge

The gate charge is an indicator of how fast a device can be turned on and off. Furthermore, it describes the charge needed to fully activate the device and provides an indicator for switching losses.

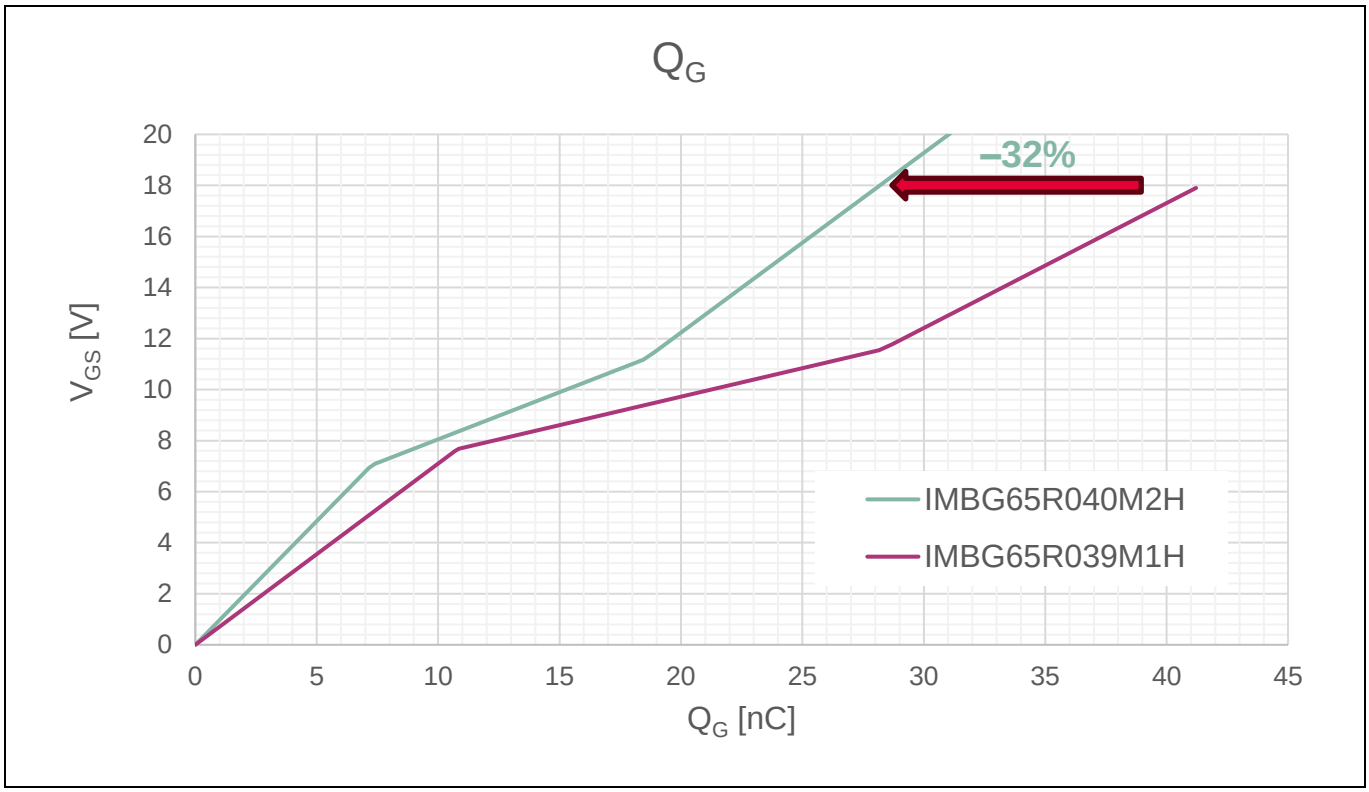

Figure 10 Q_G comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

The gate charge from CoolSiC™ Gen2 MOSFETs is strongly reduced in comparison to CoolSiC™ Gen1 MOSFETs. This indicates that CoolSiC™ Gen2 MOSFETs are more prone to PCB parasitics, especially on the V_{GS} oscillation and the limits stated in the datasheet due to voltage peaks. However, Infineon has increased these limits and therefore, it is possible to use the same $R_{G,ext}$ as in CoolSiC™ Gen1 MOSFETs and gain the benefit of the lower switching losses.

Furthermore, the ratio of C_{GS} and C_{GD} is dramatically reduced and therefore, reduce the possibility of a dV/dt induced re-turn-on. This parasitic turn-on (PTO) factor can be calculated based on datasheet values according to the following formula:

$$PTO\ factor = \frac{Q_{GD\ @\ 400\ V}}{Q_{GS}\ @\ V_{GS(th)\ @\ 25°C}}$$

Equation 2 Parasitic turn-on factor calculation

Applying this formula to CoolSiC™ Gen2 and Gen1 MOSFETs results in the following diagram:

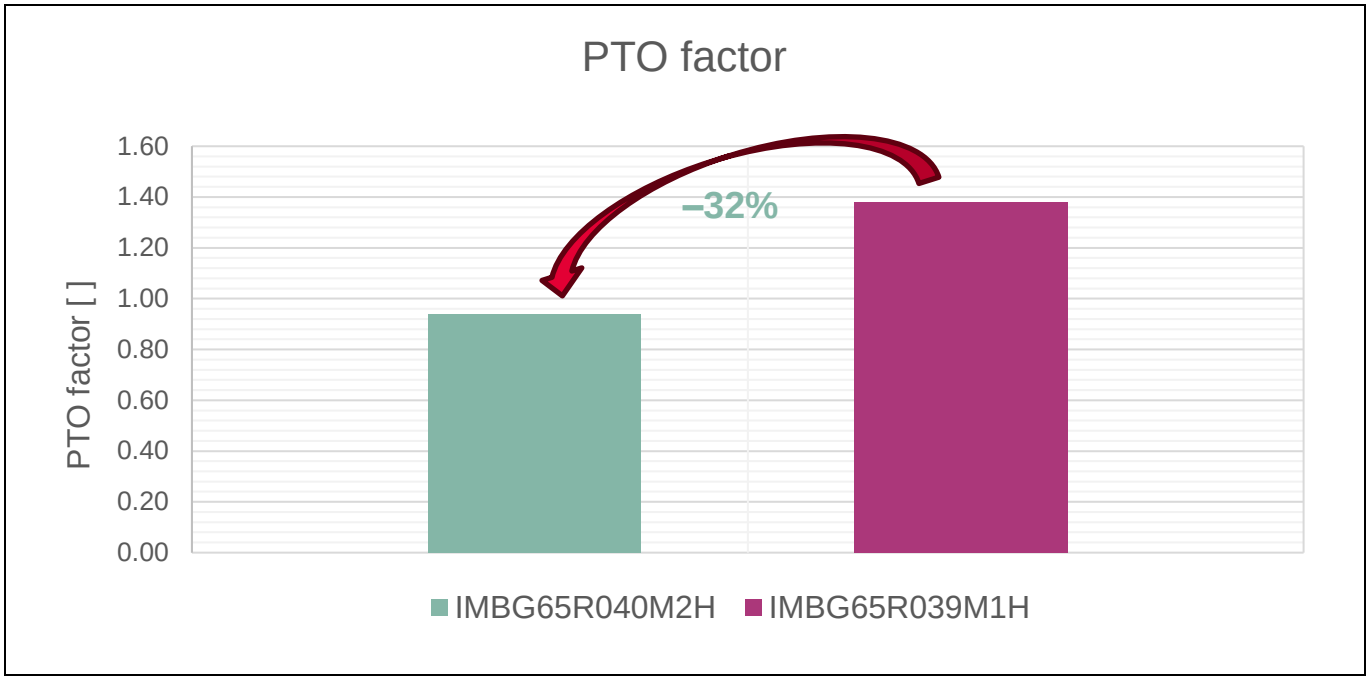

Figure 11 PTO factor comparison: CoolSiC™ Gen2 vs. Gen1 MOSFETs

As shown in Figure 11, CoolSiC™ Gen2 MOSFETs show a lower value than CoolSiC™ Gen1 MOSFETs. The lower the value, the less possibility of a dV/dt driven re-turn-on. Note that this is still at 0 V turn off voltage.

3 Negative gate driving voltage

CoolSiC™ MOSFETs from Infineon do not need negative gate drive voltage because the PTO factor is very low and show the best behavior with respect to re-turn-on on the market. However, due to second source possibility, CoolSiC™ Gen2 MOSFETs have an improved gate oxide allowing negative gate source voltage as the turn-off voltage. Because a lot of SiC MOSFETs on the market can only perform at V_{GS} = –5 V, this new gate oxide is introduced. This results in an even easier-to-use and easier-to-drive for CoolSiC™ Gen2 MOSFETs.

It cannot be neglected that there is still a V_{th} drift and a corresponding $R_{DS(on)}$ drift over the lifetime, as with all SiC MOSFETs which are available on the market. However, this $R_{DS(on)}$ impact can be negligible as shown in Figure 12.

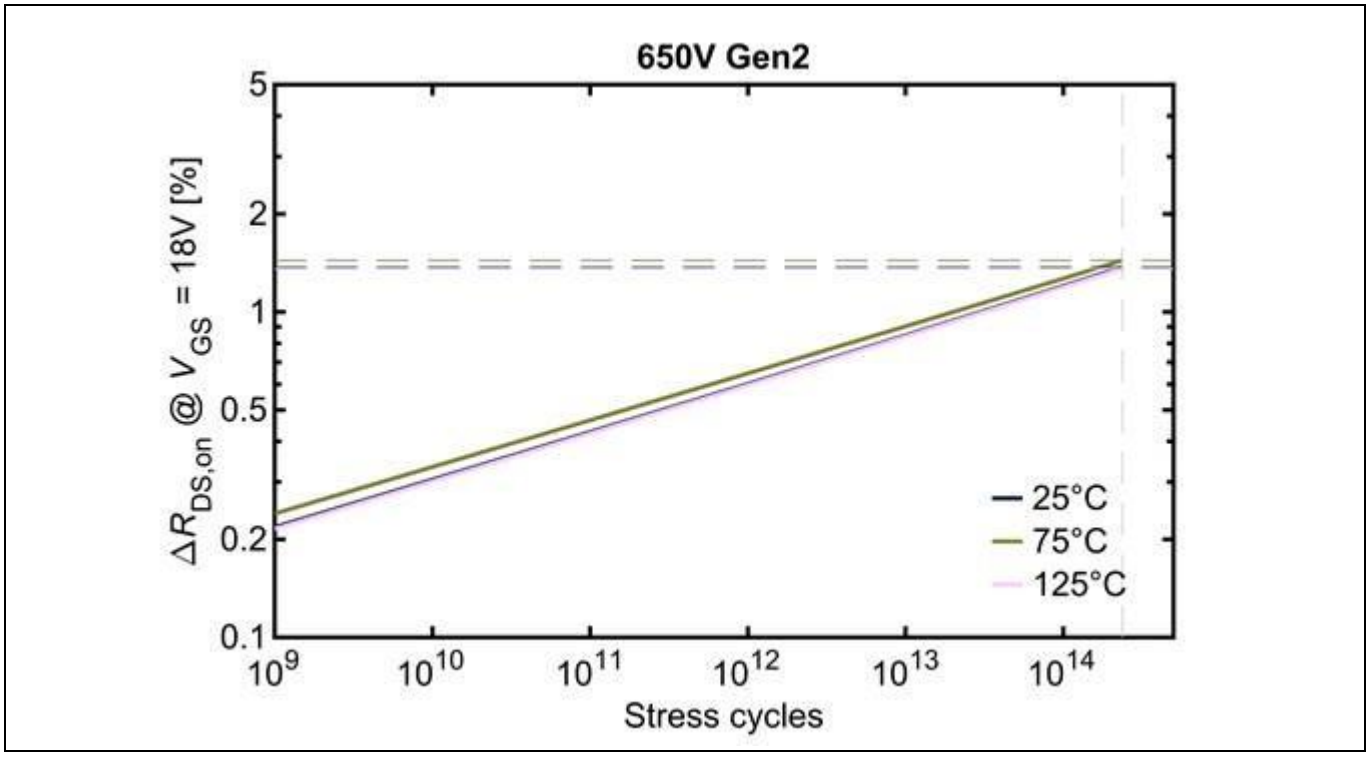

Figure 12 $R_{DS(on)}$ drift over lifetime

As shown in Figure 12, the $R_{DS(on)}$ drift over lifetime does not exceed 2% in typical operation conditions between 75°C and 125°C and –5 V to 18 V gate driving. This drift has no impact on efficiency and performance. Additionally, the gate oxide reliability and the screening remain the same as in CoolSiC™ Gen1 MOSFETs.

Furthermore, CoolSiC™ Gen2 MOSFETs allow voltage peaks down to –10 V, allowing headroom for voltage peaks coming from high dV/dt or parasitic inductances from the PCB design.

4 Application tests

This section provides the benchmarking against the SiC MOSFETs that are currently available on the market in a 3.3 kW CCM Totem Pole PFC and in a 3.3 kW LLC converter.

4.1 3.3 kW CCM Totem Pole PFC

The CCM Totem Pole PFC is the highest-efficient bridgeless topology achieving efficiency higher than 99% peak. The 99% efficiency is mandatory to achieve a system efficiency of a SMPS of above 98%. This AC to DC converter is a full Infineon solution, using IMZA6R048M1H as boost stage including CoolMOS™ 600 V, C7 17 mΩ devices as grid rectifier, Infineon 18 V auxiliary bias supply, XMC1404, and more. The input voltage is from 176 V AC to 360 V AC, fully capable of 3.3 kW output power at 400 V output voltage and a switching frequency of 65 kHz.

For benchmarking the system, each device is optimized with respect to dead-time setting that a maximum of 20–30 ns is achieved to have ZVS operation. Furthermore, $R_{G,ext}$ is adjusted to have all voltages (V_{GS} and V_{DS}) within the datasheet limits. The efficiency measurement is performed with WT3000 power analyzer from Yokogawa with an applied line filter of 500 Hz for each device under test and the fan (cooling concept) supplied externally.

4.1.1 D2PAK

Several devices have been tested; this section starts with the devices in D2PAK. The following $R_{G,ext}$ settings have been used.

Table 2 D2PAK $R_{G,ext}$ settings for 3.3 kW CCM Totem Pole PFC

DUTs	$R_{G,ext}$	$V_{GS,min}$ V_{in} = 176 V AC I_{out} = 8.3 A	$V_{DS,max}$ V_{in} = 176 V AC I_{out} = 8.3 A	Peak efficiency (eta) V_{in} = 230 V AC
IMBG65R040M2H	10 Ω	–9.9 V (–10 V)	525 V (580 V)	99.16%
IMBG65R039M1H	10 Ω	–6.4 V (–7 V)	579 V (580 V)	99.00%
Vendor 1 MOSFET	8.2 Ω	–10.8 V (–11V)	564 V (580 V)	98.83%

As anticipated earlier, CoolSiC™ Gen2 and Gen1 MOSFETs can use the same $R_{G,ext}$ of 10 Ω as mentioned in the datasheet limit (values in parentheses) that has been increased. With this CoolSiC™ Gen2 MOSFET, it can deliver the highest peak efficiency of 99.16%. Figure 13 and Figure 14 show the efficiency delta at 230 V AC and 176 V AC.

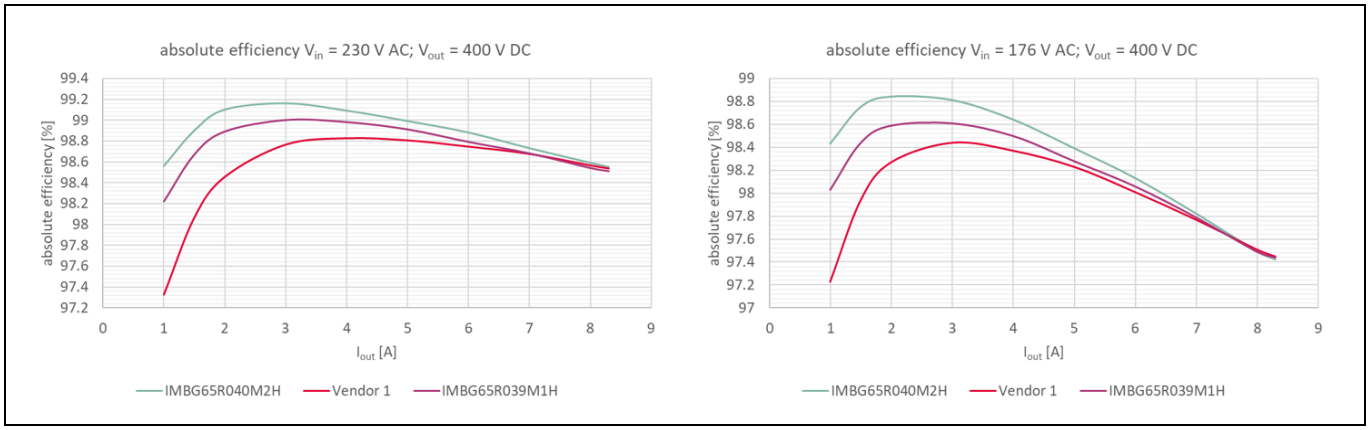

Figure 13 D2PAK absolute efficiency comparison: 3.3 kW CCM Totem Pole PFC

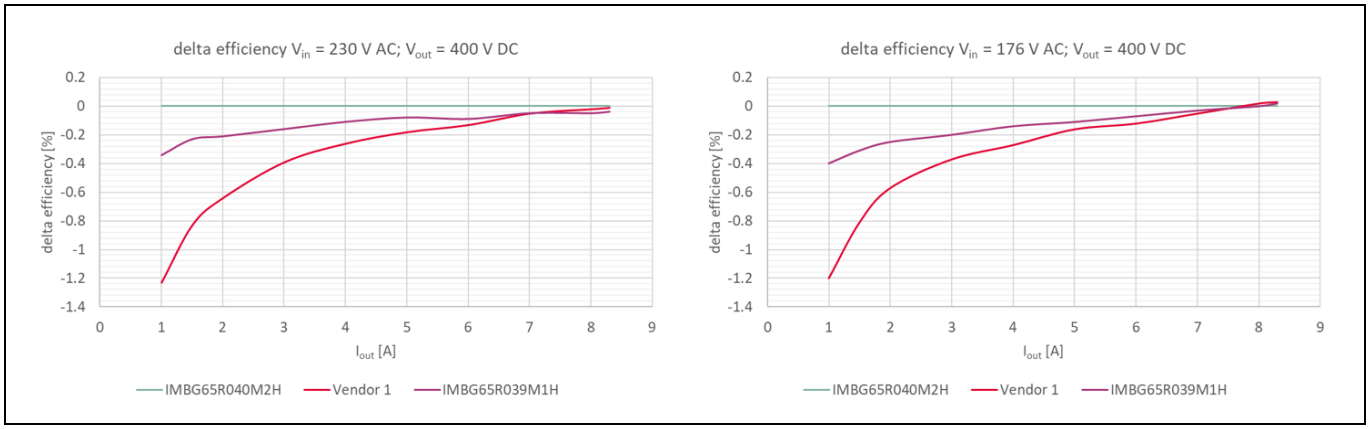

Figure 14 D2PAK delta efficiency comparison: 3.3 kW CCM Totem Pole PFC

As Figure 14 shows, the Vendor 1 product shows a strong drawback in efficiency over the whole load range. This is due to 0 V gate driving; the Vendor 1 product shows strong re-turn-on behavior as shown in Figure 15.

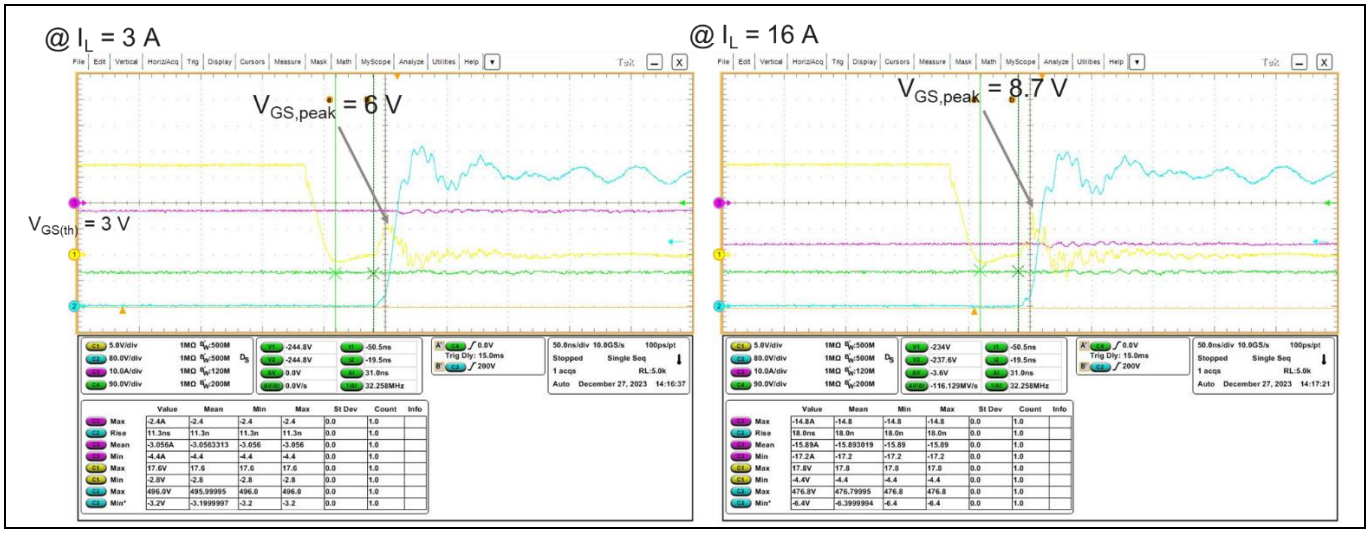

Figure 15 D2PAK re-turn-on of Vendor 1 product

To get high efficiency, the Vendor 1 product can only be used with –5 V turn-off voltage; however, even there, a re-turn-on will be visible: already at a choke current (I_L) of 16 A, the $V_{GS,peak}$ is 8.7 V and the $V_{GS(th)}$ of the device is between 1.8 V and 4.2 V according to the datasheet.

4.1.2 TO-247-4

To see the efficiency delta between several devices and the impact of the $R_{DS(on)}$, the following test scenario is represented.

Table 3 TO-247-4 $R_{G,ext}$ settings: 3.3 kW CCM Totem Pole PFC

DUTs	$R_{G,ext}$	$V_{GS,min}$ V_{in} = 176 V AC I_{out} = 8.3 A	$V_{DS,max}$ V_{in} = 176 V AC I_{out} = 8.3 A	Peak eta V_{in} = 230 V AC
IMZA65R040M2H	6.8 Ω	–9.6 V (–10 V)	510 V (580 V)	99.19%
IMZA65R050M2H	6.8 Ω	–9.8 V (–10 V)	521 V (580 V)	99.20%
IMZA65R039M1H	6.8 Ω	–6 V (–7 V)	511 V (580 V)	99.03%
IMZA65R048M1H	6.8 Ω	–6.8 V (–7 V)	512 V (580 V)	99.04%
Vendor 2	10 Ω	–4 V (–4 V)	477 V (580 V)	98.99%
Vendor 3	3.8 Ω	–6 V (–8 V)	508 V (580 V)	98.83%

The same procedure is performed in this benchmark. Only for the Vendor 3 product, it is not possible to further reduce $R_{G,ext}$ because changing from 3.8 Ω to 3.2 Ω shows the violation of the –8 V on the gate source voltage. By applying these settings, the following efficiency delta is achieved.

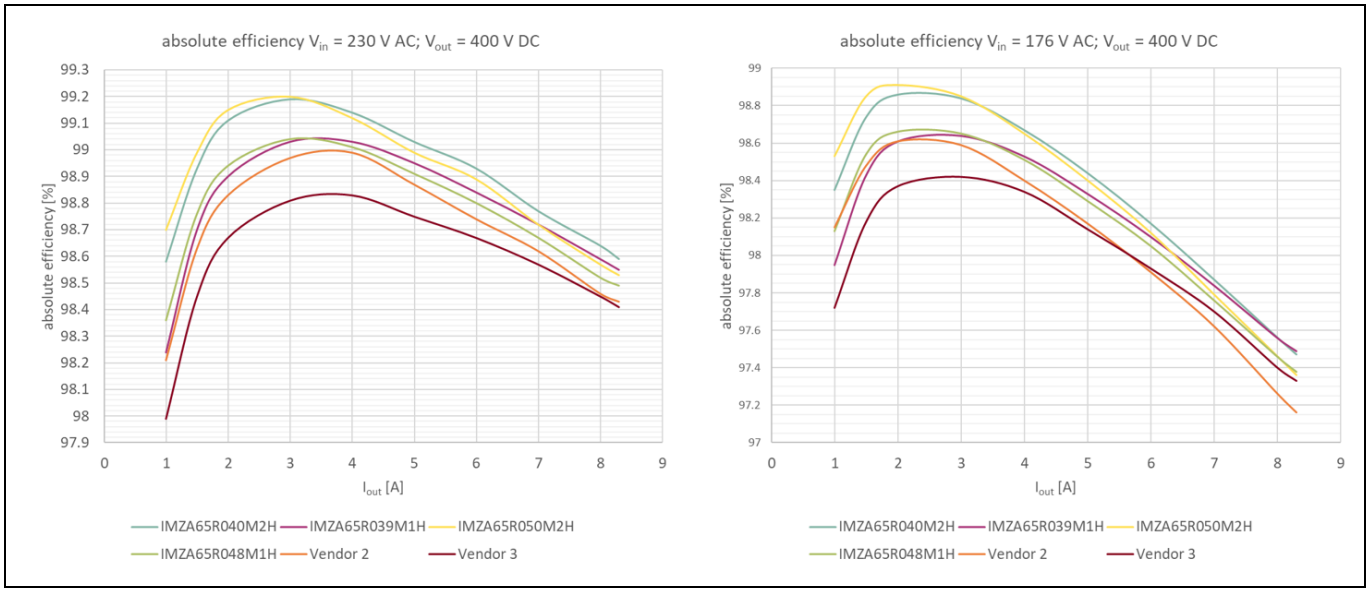

Figure 16 TO-247-4 absolute efficiency comparison: 3.3 kW CCM Totem Pole PFC

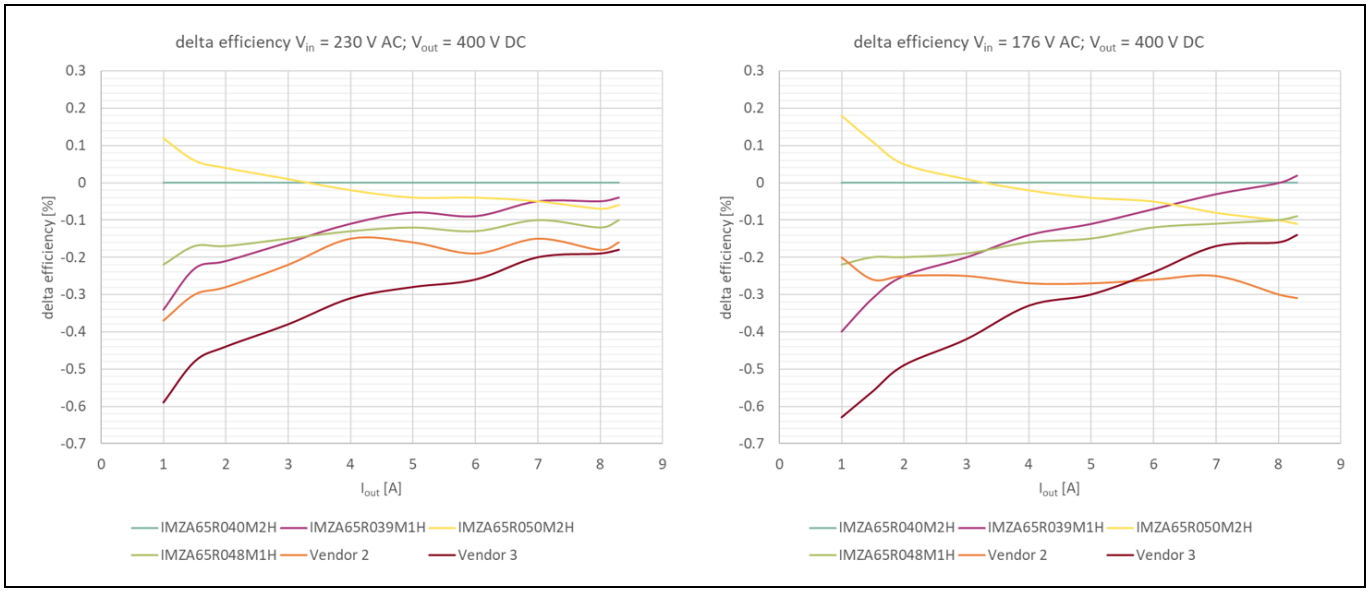

Figure 17 TO-247-4 delta efficiency comparison: 3.3 kW CCM Totem Pole PFC

It shows that the CoolSiC™ Gen2 MOSFET outperforms when compared with all other devices under test at both input voltages. Furthermore, the 50 mΩ device behaves as expected, leading to higher efficiency in light load and lower efficiency in full load due to the capacitances (light load) and the $R_{DS(on)}$ (full load). Especially such a behavior can be achieved as even though there is a chip size reduction; Infineon has improved the R_{th} values for the products as they use the diffusion solder process. This results in keeping the R_{th} from CoolSiC™ Gen2 MOSFETs on the same values as in CoolSiC™ Gen1 MOSFETs.

Table 4 R_{th} comparison: Gen2 vs. Gen1

DUTs	$R_{th,JC}$ max [K/W]
IMZA65R040M2H	0.87
IMZA65R039M1H	0.85

4.2 3.3 kW LLC converter

As described in the technology parameters, CoolSiC™ MOSFETs are a good fit for resonant topologies like LLC converters. The body diode behavior can improve the system stability under certain operating conditions in which a hard commutation can occur.

This test board is based on telecom requirements with an input voltage of 380 V DC and an output power of 3.3 kW at 52 V output voltage.

Continuing in this test, the setup is always optimized for each device under test leading to the following settings.

Table 5 TO-247-4 $R_{G,ext}$ settings: 3.3 kW LLC converter

DUTs	$R_{G,on}$	$R_{G,off}$	$V_{DS,max}$ at startup (no load)
IMZA65R040M2H	10 Ω	9 Ω	453.1 V
IMZA65R050M2H	20 Ω	10 Ω	453.1 V
IMZA65R039M1H	6 Ω	4 Ω	444.3 V
IMZA65R048M1H	6 Ω	4 Ω	451.7 V
Vendor 2	3 Ω	1 Ω	460.5 V
Vendor 4	6 Ω	5 Ω	464.9 V
Vendor 3	4 Ω	2 Ω	438.9 V

This setup leads to the following results.

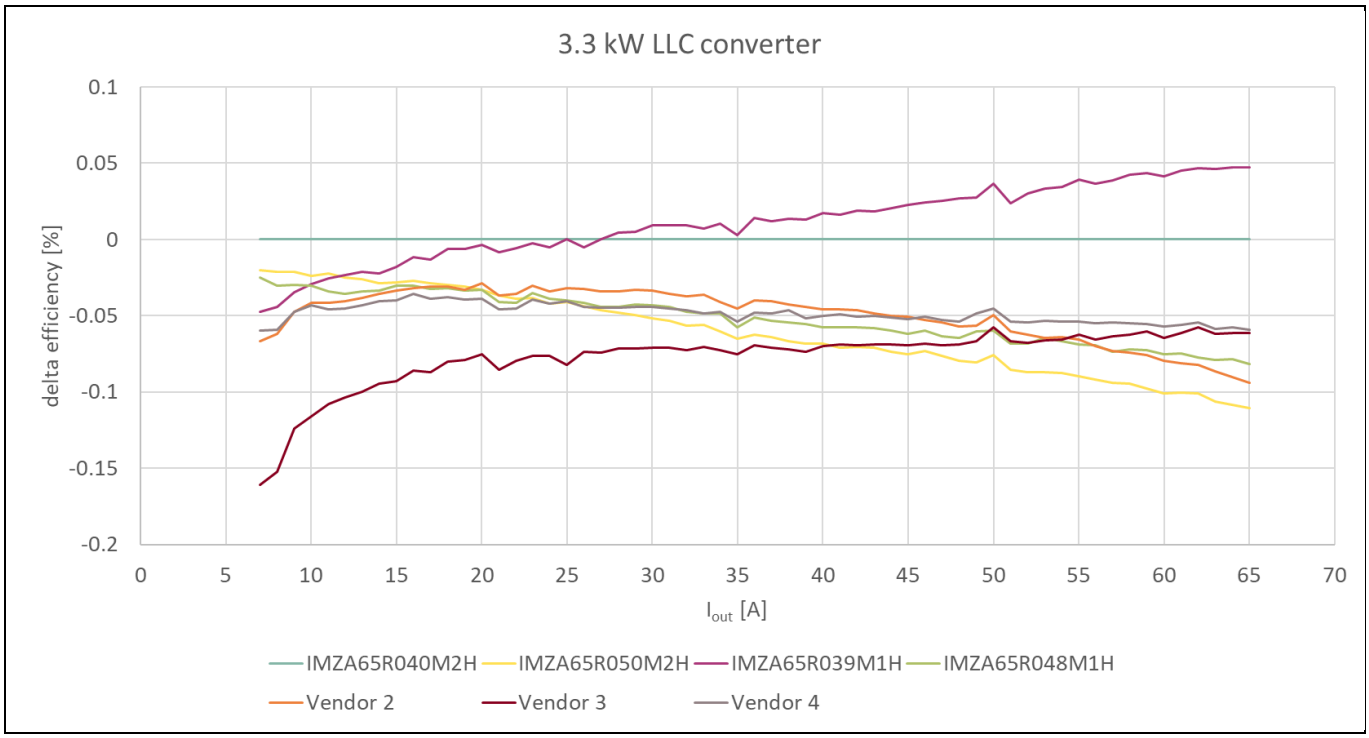

Figure 18 CoolSiC™ efficiency comparison: 3.3 kW LLC converter

CoolSiC™ Gen2 MOSFETs also perform in the LLC converter as expected. However, the difference is not as pronounced as in the 3.3 kW CCM Totem Pole PFC; nearly all devices stay within the 0.1% measurement tolerance. Only the Vendor 3 product shows the lowest performance in this benchmark.

As this test setup uses a resonant frequency of 70 kHz, there are a lot of optimizations possible. When including improved PCB parasitics and the improved technology parameters such as Q_{oss}, Q_g, and C_{oss} of CoolSiC™ Gen2 MOSFETs, the advantage from CoolSiC™ Gen2 MOSFETs can be translated into achieving high power density by increasing the switching frequency and/or improving the efficiency even further.

5 Summary

This document described the newest generation of CoolSiC™ MOSFETs in comparison with the earlier generation. The superior gate oxide allows the use of negative gate driving while the thermal coefficient point lies below 15 V, resulting in a full 15 V capable driving scheme. Furthermore, the technology parameters have improved dramatically leading to an enhanced behavior in the end-user application reaching the highest efficiency and ease of use.

Revision history

Document revision	Date	Description of changes
V 1.0	2024-02-22	Initial release

Trademarks
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