AN11158

Understanding power MOSFET data sheet parameters
Rev. 6.0 — 6 July 2020
application note

nexperia

1. Introduction

This application note explains the parameters and diagrams given in a Nexperia Semiconductors Power MOSFET data sheet. The goal is to help an engineer decide what device is most suitable for a particular application.

It is important to pay attention to the conditions for which the parameters are listed, as they can vary between suppliers. These conditions can affect the values of the parameters making it difficult to choose between different suppliers. Throughout this document, the data sheet for BUK7Y3R5-40H is used as an example. BUK7Y3R5-40H is an automotive-qualified part in a SOT669 (LFPAK56) package, with a voltage rating of 40 V.

The layout of this data sheet is representative of the general arrangement of Nexperia power MOSFET data sheets.

Nexperia Power MOSFETs are designed with particular applications in mind. For example, switching charge is minimized where switching losses dominate, whereas on-resistance is minimized where conductive losses dominate.

2. Data sheet technical sections

Nexperia power MOSFET data sheets begin with an overview of the device, giving the designer the key information regarding device suitability. The overview consists of:

- General description, describing the technology used, the package and relevant qualifications, e.g. AEC-Q101
- Features and benefits, listing important features of the MOSFET and the benefit they offer.
- Applications, listing the applications for which the MOSFET is particularity suited.

The product overview is followed by these technical sections:

- Quick reference data
- Pinning information
- Ordering information
- Limiting values
- Thermal characteristics
- Electrical characteristics
- Package outline

2.1. Quick reference data

The quick reference data table contains more detailed information and the key parameters for the intended application. An example of a quick reference data table is shown in Table 1 "Quick reference data".

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1	[1]	-	-	120	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	115	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C		2	2.9	3.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 20 A; V_{DS} = 44 V; V_{GS} = 10 V		-	6	15	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	16	-	nC

[1] 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

The general format for describing a parameter is to provide the official symbol and then the correct parameter name. Any relevant conditions and information are listed after the parameter names. The values and units of the values are entered in the remaining columns. Generally, measurement methods are as described in IEC 60747-8.
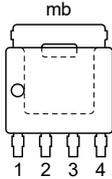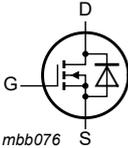
The quick reference data parameters are described in more detail in the characteristics section of the data sheet. The following list is an introduction to some of the key symbols together with a description of the parameter each represents:

- **V_{DS}** - the maximum voltage between drain and source that the device is guaranteed to block in the off state. This section of the data sheet deals with the most commonly used temperature range, as opposed to the full temperature range of the device.
- **I_D** - the maximum continuous current the device can carry with the mounting base held continuously at 25 °C with the device fully on. In the example provided in Table 1, I_D requires a V_{GS} of 10 V.
- **P_{tot}** - the maximum continuous power the device can dissipate with the mounting base held continuously at 25 °C.
- **R_{DSon}** (drain-source on state resistance) - the typical and maximum resistance of the device in the on-state under the conditions described. R_{DSon} varies greatly with both T_j and the gate-source voltage (V_{GS}). Graphs are provided in the data sheet to assist in determining R_{DSon} under various conditions.
- **Q_{GD}** (gate-drain charge) - an important switching parameter that relates to switching loss, along with Q_{GS} and $Q_{G(tot)}$. Q_{GD} is inversely proportional to R_{DSon}, therefore choosing an appropriate balance between R_{DSon} and Q_{GD} is critical for optimal circuit performance.
- **Q_r** (recovered charge) – the total amount of charge recovered from the anti-parallel diode when it is switched from its conducting state to its reverse biased state under controlled conditions. Q_r is an important factor involved in voltage spiking when interacting with external inductances and an important consideration when investigating EMC and efficiency. Generally the higher the Q_r value the larger the voltage and current spikes at switch off leading to longer damping times. Nexperia includes stored charge Q_s as well as output charge Q_{oss} in its stated value for Q_r such that $Q_r = Q_s + Q_{oss}$.

2.2. Pinning information

This section describes the internal connections and general layout of the device. Note that the symbol is for an enhancement mode n-channel MOSFET with the source and body tied together, and a parallel diode between the source and drain. The parallel diode is known as the body diode and is inherent in power MOSFETs. N-channel power MOSFETs have the body diode between drain and source, as shown in Table 2.

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source	mb	D
4	G	gate		G
mb	D	mounting base; connected to drain	1 2 3 4 **LFPAK56; Power-SO8 (SOT669)**	mbb076　S

2.3. Ordering information

The ordering section provides information on how to order the device. The package version and decription are given as well as any commonly used package name.

2.3.1. Marking

Depending on the device package, the data sheet may include a marking section. This provides the marking code which is printed onto the device during manufacter, (else the device name will be printed).

2.4. Limiting values

The limiting values table provides the range of operating conditions allowed for the MOSFET. The conditions are defined in accordance with the absolute maximum rating system (IEC 60134). Operation outside of these conditions is not guaranteed, so it is recommended that these values are not exceeded. Doing so runs the risk of immediate device failure or reduced lifetime of the MOSFET. The avalanche ruggedness conditions, when given, describe the limited conditions for which the V_{DS} rating can be exceeded.

To calculate how the limiting values change with temperature, they are read together with the derating curves provided.

The limiting values table for the BUK7Y3R5-40H is given as an example of a standard limiting values table, in Table 3.

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-10	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C;		-	115	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1	[1]	-	120	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2	[1]	-	93	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C		-	526	A
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	120	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	526	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 120 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; [Fig. 3](#)	[2] [3]	-	45	mJ

[1] 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.

- **V_{DS}** (drain-source voltage) - the maximum voltage the device is guaranteed to block between the drain and source terminals in the off-state for the specified temperature range. For the BUK7Y3R5-40H, the temperature range is from +25 °C to +175 °C. For operation below 25 °C, the V_{DS} rating reduces due to the positive temperature coefficient of avalanche breakdown. This is covered in Section 2.4.1 of this document.

- **V_{GS}** (gate-source voltage) - the maximum voltage the device is specified to block between the gate and source terminals. Some Nexperia data sheets specify different values for DC and pulsed V_{GS}. In these cases the DC value is a constant gate voltage over the lifetime of the device at the maximum T_j, whilst the higher-value pulsed-rating is for a shorter, specified accumulated pulse duration at the maximum specified T_j.
  Gate-oxide lifetime (refer to AN90001) reduces with increasing temperature and/or increasing gate voltage. This means that V_{GS} lifetimes or ratings quoted for lower junction temperatures are significantly greater than if specified at higher temperatures. This can be important when comparing data sheet values from different manufacturers.

- **V_{DGR}** (drain-gate voltage) is typically the same value as the V_{DS} rating. This parameter appears in the data sheets of older devices but is not quoted for newer devices such as in the BUK7Y3R5-40H data sheet.

- **I_D** (drain current) - the maximum continuous current the device is allowed to carry under the conditions described. This value can be related to either package construction, or the maximum current that would result in the maximum T_j. As such it depends on an assumed mounting base temperature (T_{mb}), the thermal resistance (R_{th}) of the device, and its R_{DSon} at maximum T_j. Note that some suppliers quote the "theoretical" silicon limit, while indicating the package limited value in the characteristic curves.

- **I_{DM}** (peak drain current) is the maximum drain current the device is allowed to carry for a pulse of 10 µs or less.

- **P_{tot}** (total power dissipation) is the maximum allowed continuous power dissipation for a device with a mounting base at 25 °C. The power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C. In reality, it is difficult to keep the mounting base at this temperature while dissipating the 105 W that is the calculated power dissipation for the BUK7Y3R5-40H. In other words, P_{tot} indicates how good the thermal conductivity of the device is, and its maximum allowed junction temperature.
  Note that some other semiconductor vendors quote performance when mounted on a copper PCB usually 1 inch square. In practice, this information is rather meaningless as the semiconductor vendor has no control over how the device is cooled. See *AN10874 - LFPAK MOSFET thermal design guide. AN10874* describes different techniques that can be used during the design phase to ensure that the PCB layout provides optimum thermal performance.

- **T_{stg}** (storage temperature) is the temperature range in which the device can be stored without affecting its reliability. Long term storage should be in an inert atmosphere to prevent device degradation, for example, by tarnishing of the metal leads.

- **T_j** (junction temperature) is the operational temperature range of the device. Typically, T_j is the same as the storage temperature. Outside of this range, device parameters are outside the range of the data sheet and device lifetime is reduced.

- **I_S** (source current) - the maximum continuous current of the MOSFET body diode, which is briefly discussed in Section 2.2. The same considerations apply as for I_D.

- **I_{SM}** (peak source current) - the maximum current pulse that the MOSFET body diode is guaranteed to carry. The same considerations apply as for I_{DM}.
- **E_{DS(AL)S}** (non-repetitive drain-source avalanche energy) - the maximum allowed single overvoltage energy pulse under the conditions specified. For this example, the conditions are the maximum continuous drain current allowed for a mounting base temperature of 25 °C. The avalanche energy allowed is the energy pulse that would raise the device temperature from 25 °C to its maximum allowed T_j, while the mounting base temperature is held at 25 °C. The avalanche energy is specified for the maximum continuous drain current. Some vendors specify the avalanche energy for a different current and higher inductive load, which can increase the apparent avalanche energy for an inferior performance. An example is given with the derating curve as described in Section 2.4.3 of this document.
- **E_{DS(AL)R}** (repetitive drain-source avalanche energy) - the maximum amount of energy allowed in each avalanche event when more than one avalanche event occurs. The thermal constraints imposed for repeated avalanche operation is given by curve 3 of Fig. 3 in Section 2.4.3 of this document. There are also the standard thermal requirements in addition to the energy requirements for repetitive avalanche events. These requirements are assessed with the thermal characteristic curves as described in Section 2.5. Avalanche performance is covered in detail in application note *AN10273*.
  This parameter is only listed on Nexperia data sheets where the repetitive avalanche capability has been assessed. It is not shown in Nexperia data sheets where it has not been assessed, for example non-automotive MOSFETs.

2.4.1. Derating curves

The derating curves are provided immediately after the tabulated limiting value data, and help the designer calculate how the limits change with temperature.

2.4.1.1. Continuous drain current

The following procedure serves as an example to calculate the maximum continuous drain current for the BUK7Y3R5-40H. Assume an application with a mounting base temperature T_{mb} of 75 °C.

Refer to the graph depicted in Fig. 1 which depicts the continuous drain current as a function of mounting base temperature.

Fig. 1 shows that for a T_{mb} of 75 °C, the maximum continuous drain current has reduced from 120 A, listed at 25 °C, to 105 A, see Equation (1) and Equation (2) below.
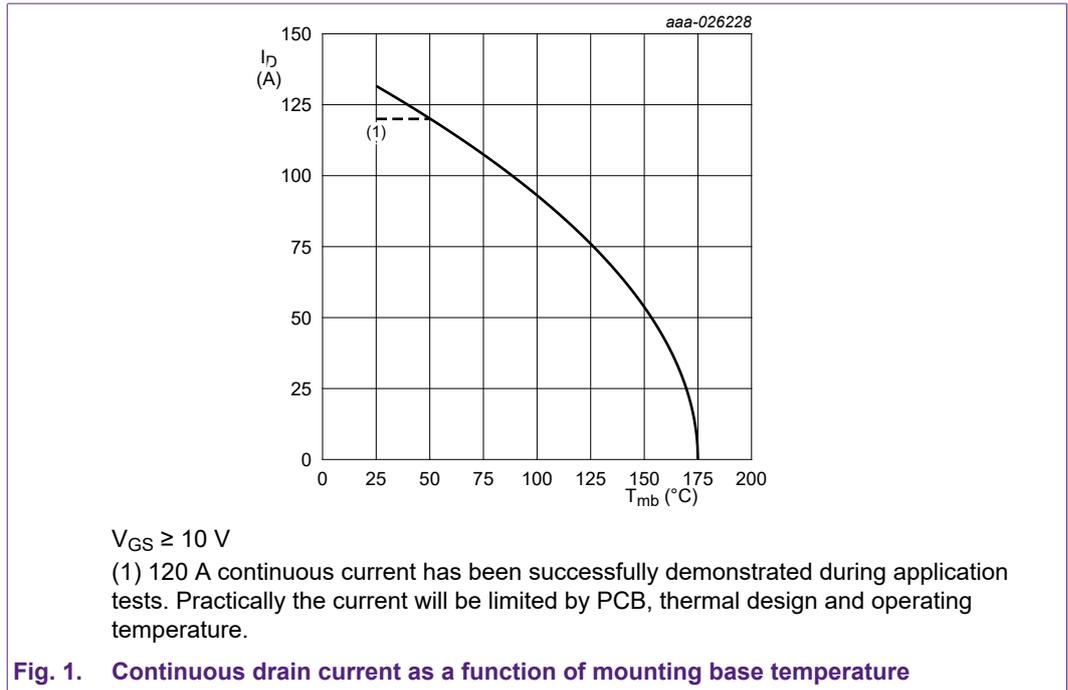
The maximum current at any T_{mb}, is the current that increases T_j to the maximum allowed temperature (175 °C). $P = I^2 \times R_{DSon}$ represents the power dissipation at T_j, where the R_{DSon} used is the maximum value for the maximum T_j. Therefore, the allowed current is proportional to the square root of the allowed power dissipation.

The power dissipation allowed for a given T_{mb} is proportional to the allowed temperature increase. This means that the derating curve shown, is based on the following equations:

$$I_D{}^2 (T_{mb}) \propto \frac{T_j - T_{mb}}{T_j - 25\,°C} \tag{1}$$

$$I_D (T_{mb}) = I_D (25\,°C) \times \sqrt{\frac{T_j - T_{mb}}{T_j - 25\,°C}} \tag{2}$$

At the maximum allowed junction temperature of 175 °C, this current has decreased to zero.

$V_{GS} \geq 10$ V

(1) 120 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 1.   Continuous drain current as a function of mounting base temperature

2.4.2. Power dissipation

Power dissipation varies with different temperatures. However, in this case, the power dissipation curve is normalized. The allowed power is presented as a percentage of the allowed power dissipation at 25 °C, as opposed to an absolute value.

Example:

By observing the curve in Fig. 2, the allowed power dissipation for a T_{mb} of 75 °C is approximately 66 % of that allowed at 25 °C. The graphic data in Fig. 2, shows the maximum continuous power dissipation (P_{tot}) at 25 °C is 105 W.

This means that the maximum power dissipation allowed at 75 °C, is 66 % of 105 W which is 70 W.

Equation (3) is the equation to calculate power dissipation:

$$P_{tot}(Tmb) = P_{tot}(25\,°C) \times \frac{Tj - Tmb}{Tj - 25\,°C} \qquad (3)$$

Where T_j = $T_{j(max)}$, usually 175 °C.

AN11158

application note   **Rev. 6.0 — 6 July 2020**   **7 / 29**

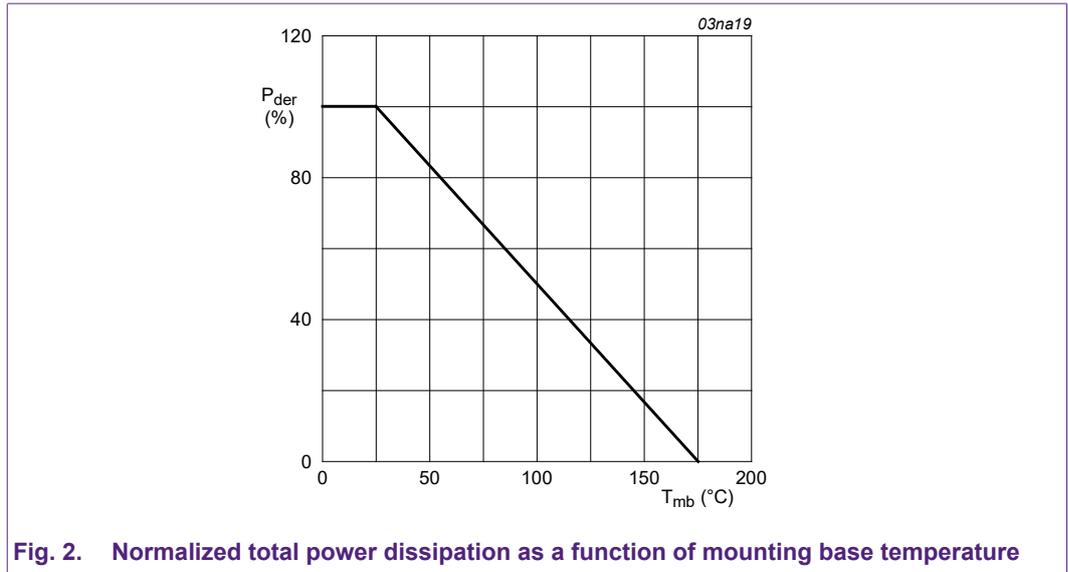**Fig. 2.**   **Normalized total power dissipation as a function of mounting base temperature**

The curves provided in Fig. 1 and Fig. 2 are read in conjunction with the limiting values tables. The information extracted, assists in calculating the maximum current allowed and the power dissipation with respect to temperature.

2.4.3. Avalanche ruggedness

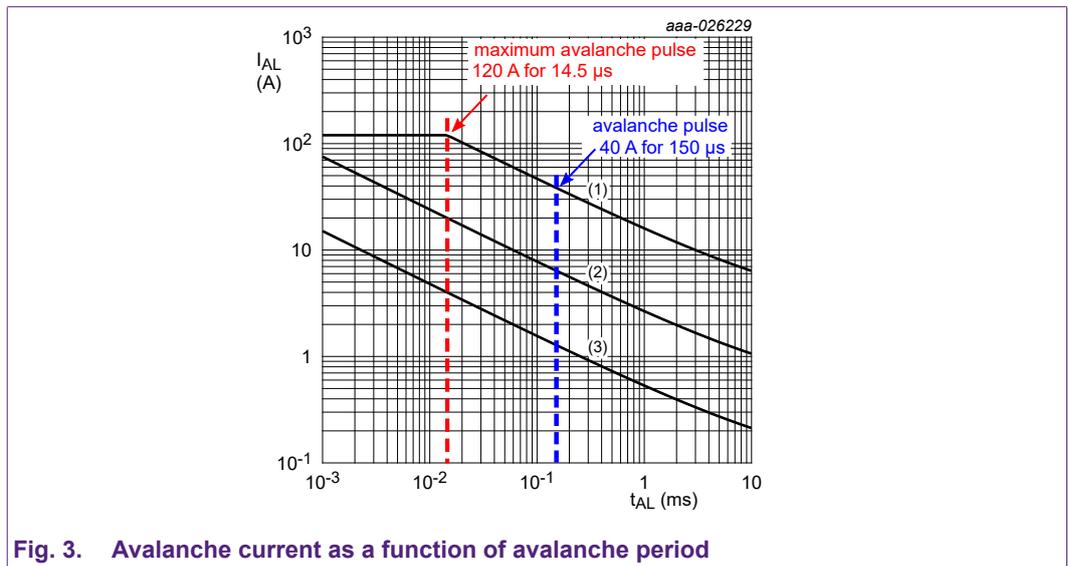Avalanche ruggedness is covered in detail in *AN10273*.

Fig. 3.   **Avalanche current as a function of avalanche period**

A simple example for the BUK7Y3R5-40H, using the information in *AN10273*, is extracted from the limiting values Table 3:

With I_D = 120 A, V_{sup} ≤ 40 V, R_{GS} = 50 Ω, V_{GS} = 10 V and $T_{j(init)}$ = 25 °C unclamped, the maximum $E_{DS(AL)S}$ is 45 mJ.

An avalanche event has a triangular pulse shape, so the average power is calculated as $(0.5 \times V_{DS} \times I_{DS})$.

AN10273 states that the assumed breakdown voltage is 130 % of the rated voltage, in the case of the BUK7Y3R5-40H this is 52 V (40 V x 1.3).

Fig. 3 shows a maximum current of 120 A at 25 °C (the limiting values Table 3 confirms this value).

The time for the maximum avalanche energy can be read from Fig. 3 as 14.5 μs.

This means that the maximum avalanche energy allowed is:
0.5 × (40 V × 1.3) × 120 A × 14.5 μs = 45.24 mJ.

However the limit value quoted in Table 5 of the data sheet is rounded to 45 mJ.

If a competitor quotes avalanche energy at 40 A, the graph shows that the avalanche time for the BUK7Y3R5-40H has increased to 150 μs. The avalanche energy is now 0.5 × (40 V × 1.3) × 40 A × 150 μs = 156 mJ, which is much higher than data sheet limiting value.

Ruggedness events lie outside the Safe Operating Area (SOA).

2.4.4. Safe Operating Area (SOA)

The Safe Operating Area (SOA) curves are some of the most important on the data sheet.
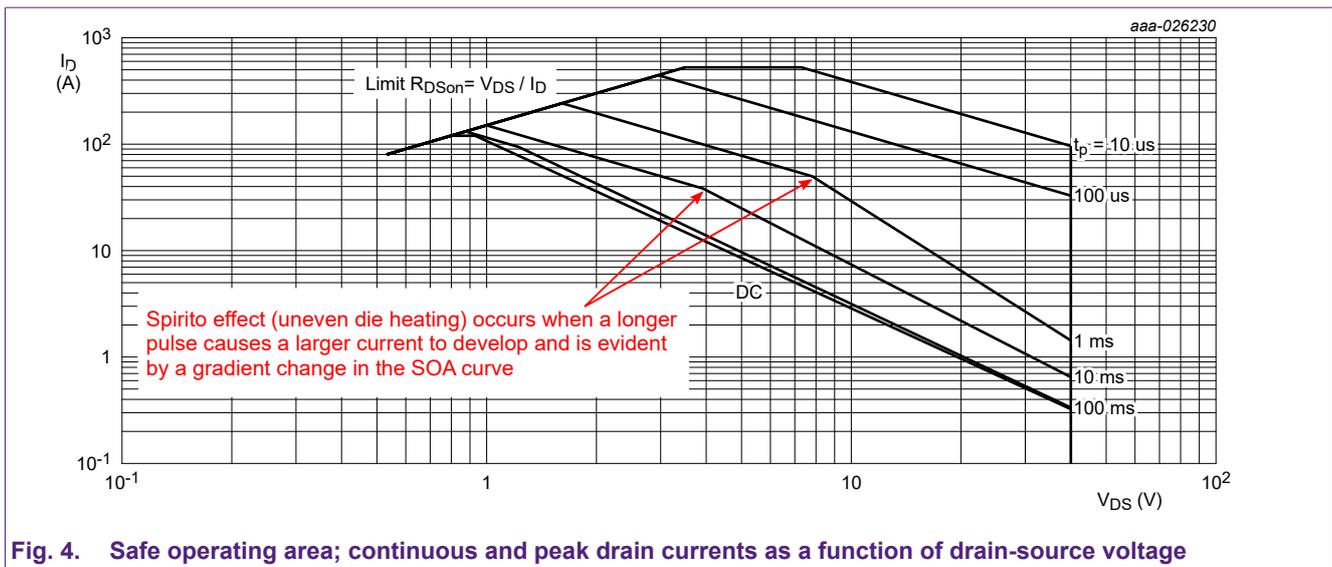
Fig. 4.   Safe operating area; continuous and peak drain currents as a function of drain-source voltage

The SOA curves show the voltage allowed, the current and time envelope of operation for the MOSFET. These values are for an initial T_{mb} of 25 °C and a single current pulse. This is a complex subject which is further discussed in the appendix (Section 3.1).

2.5. Thermal characteristics

This section describes the thermal impedance as a function of pulse duration for different duty cycles. This information is required to determine the temperature that the silicon reaches under particular operating conditions, and whether it is within the guaranteed operation envelope.

The thermal characteristics are shown in Table 4. The thermal impedance changes with pulse length because the MOSFET is made from different materials. For shorter durations, the thermal capacity is more important, while for longer pulses, the thermal resistance is more important.

The thermal characteristics are used to check whether particular power loading pulses above the DC limit would take T_j above its safe maximum limit. Repetitive avalanche pulses must be considered in addition to the constraints specific to avalanche and repetitive avalanche events.

Table 4. Thermal characteristics

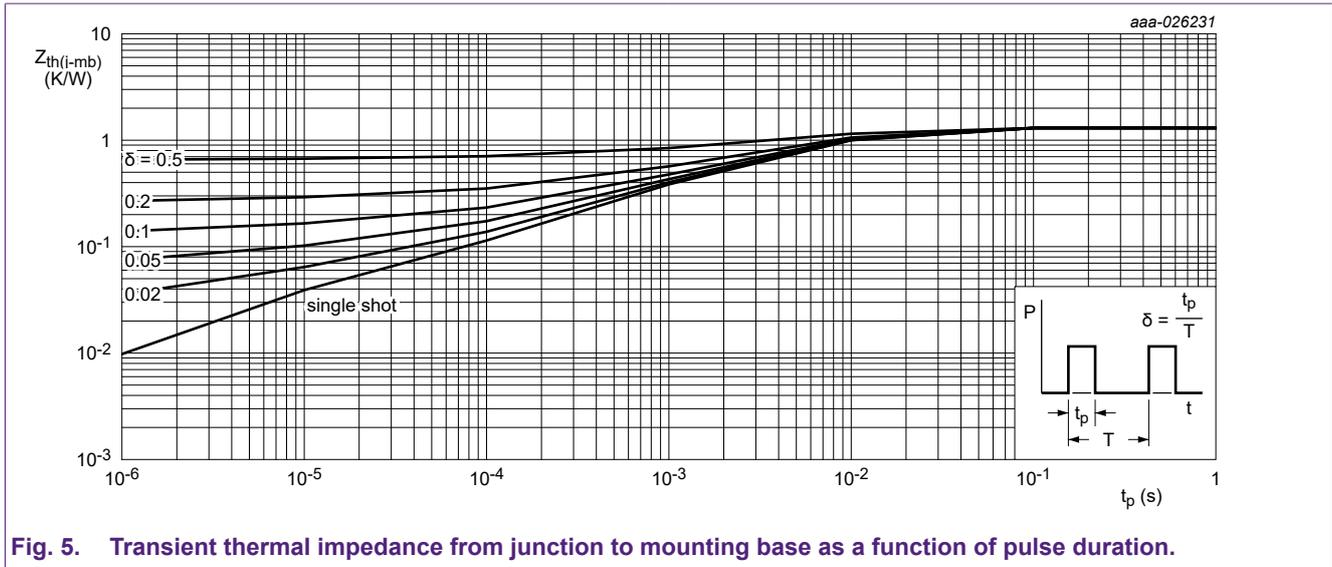| Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.18	1.3	K/W

Fig. 5.   **Transient thermal impedance from junction to mounting base as a function of pulse duration.**

Thermal resistance (R_{th}) and thermal impedance (Z_{th}) are related because the thermal resistance is the steady-state measure of how the device blocks heat flow. Thermal impedance is how the device responds to transient thermal events. It involves different thermal capacities of parts of the device and the thermal resistances between these parts. Under DC conditions, Z_{th} is equal to R_{th}. Equation (4) represents the temperature rise for a particular power dissipation:

$$\Delta T_j = |Z_{th(j - mb)}| \times Power \tag{4}$$

A worked example is discussed in the appendix (Section 3.1.2).

AN11158

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2.6. Electrical characteristics

This section is used to determine whether the MOSFET would be suitable in a particular application. This section differs from the previous two sections that are used to determine whether the MOSFET would survive within the application. The examples in this section are taken from the data sheet for the BUK7Y3R5-40H unless otherwise stated.

2.6.1. Static characteristics

The static characteristics are the first set of parameters listed in this section and an example is shown in Table 5:

Table 5. Static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	42.7	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40.1	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	39.7	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} =V_{GS} ; T_j = 25 °C; Fig. 6; Fig. 7		2.4	3	3.6	V
		I_D = 1 mA; V_{DS} =V_{GS} ; T_j = -55 °C; Fig. 6		-	-	4.3	V
		I_D = 1 mA; V_{DS} =V_{GS} ; T_j = 175 °C; Fig. 6		1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.03	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	1	10	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	37	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		2	2.9	3.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 9		2.7	4.1	5.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 9		2.9	4.5	5.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 9		3.4	5.4	6.7	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.32	0.8	2	Ω

- **$V_{BR(DSS)}$** (drain-source breakdown voltage) - an expansion of the parameter listed and explained in Section 2.4. This section lists the minimum voltage the device is guaranteed to block between the drain and source terminals in the off-state over the entire MOSFET temperature range. The temperature range is from -55 °C to +175 °C. The current between the drain and the source terminals of the BUK7Y3R5-40H when testing $V_{(BR)DSS}$ is 250 µA at the temperatures stated. $V_{(BR)DSS}$ is 40 V or less if the device is cooler than +25 °C and 40 V if the device is between +25 °C and +175 °C.
  The effect of temperature on the off-state characteristics is twofold. The leakage current increases with temperature, turning the device on. Competing against the leakage current increase, the breakdown voltage also increases with temperature.
- **$V_{GS(th)}$** (gate-source threshold voltage) is important for determining the on-state and the off-state of the MOSFET. $V_{GS(th)}$ is defined where V_{DS} = V_{GS}, although it is sometimes quoted for a fixed V_{DS} (e.g. 10 V). Note that the definition of the threshold voltage for a particular current where the gate and drain are shorted together, can differ from examples in textbooks. The parameter in textbooks describes a change in the physical state of the MOSFET and is independent of the MOSFET chip size. The parameter used in the data sheet is for a specified current and is dependent on the chip size, as the current flow is proportional to the chip area.

The threshold voltage in the data sheet is defined in a way that is best for routine measurement, but not how the actual device would typically be used. Consequently, the graphs provided in Fig. 6 and Fig. 7.
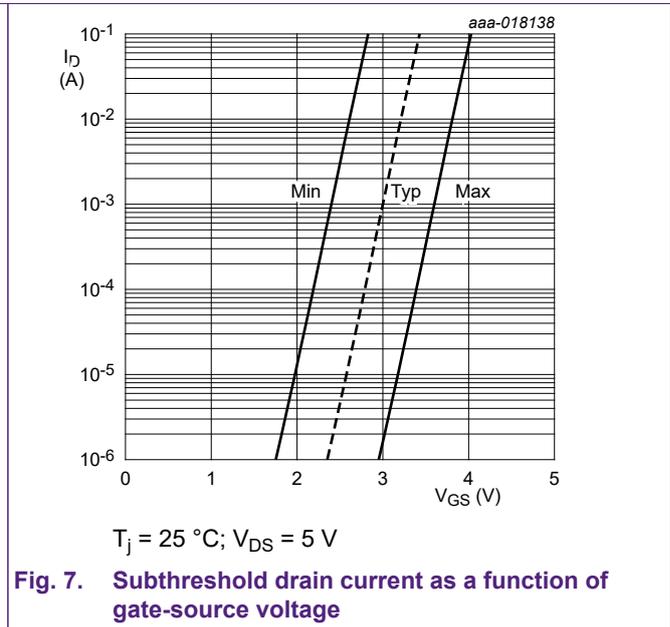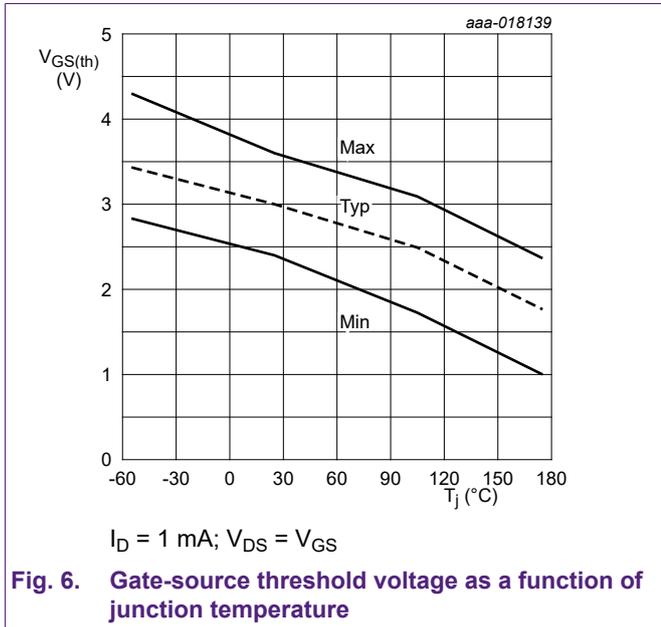

I_D = 1 mA; V_{DS} = V_{GS}

Fig. 6. **Gate-source threshold voltage as a function of junction temperature**

T_j = 25 °C; V_{DS} = 5 V

Fig. 7. **Subthreshold drain current as a function of gate-source voltage**

Fig. 6 shows the variation in the threshold voltage for the typical and limit devices over the rated temperature range. All the MOSFETs are guaranteed to have a threshold voltage between the lines.

Consequently, for the BUK7Y3R5-40H at 65 °C, if V_{DS} and V_{GS} are both less than 2 V, all devices carry less than 1 mA. Also, all devices carry more than 1 mA if V_{DS} and V_{GS} are both greater than 4 V. At 175 °C, the lower limit has fallen to 1 V, while the upper limit has fallen to 2.4 V. The lower limit is usually more important as it determines when the device is guaranteed to be turned off, and the gate driver performance an application needs.

Fig. 7 shows how the device turns on around this threshold voltage. For the BUK7Y3R5-40H, the current increases 100,000 times for an increase in gate voltage of less than 1 V. An example is given for the situation when the drain-source voltage is fixed at 5 V.

- **I_{DSS}** (drain leakage current) guarantees the maximum leakage current that the device passes at its maximum rated drain-source voltage(40V in this case) during the off-state. It is important to note how much higher I_{DSS} is at high temperature, which is the worst case.
- **I_{GSS}** (gate leakage current) guarantees the maximum leakage current through the gate of the MOSFET. The I_{GSS} is important when calculating how much current is required to keep the device turned on. Because it is a leakage current through an insulator, this current is independent of temperature, unlike I_{DSS}.
- **R_{DSon}** (drain-source on-state resistance) is one of the most important parameters. The previous parameters guarantee how the device functions when it is off, how it turns off and what leakage currents could be expected. These factors are important when battery capacity is an issue in the application.

R_{DSon} is a measure of how good a closed-switch the MOSFET is, when turned-on. It is a key factor in determining the power loss and efficiency of a circuit containing a MOSFET. The on-resistance R_{DSon} x I_D^2 gives the power dissipated in the MOSFET when it is turned **fully** on. Power MOSFETs are capable of carrying tens or hundreds of amps in the on-state.

Power dissipated in the MOSFET makes the die temperature rise above that of its mounting base. Also when the MOSFET die temperature increases, its R_{DSon} increases proportionally. Maximum recommended junction temperature is 175 °C (for all Nexperia **packaged** MOSFETs).

Using the BUK7Y3R5-40H data sheet as an example:

$R_{th(j-mb)}$ temperature rise per Watt between junction (die) and mounting base = 1.3 K/W (1.3 °C/W).

Maximum power dissipation for temperature rise of 150 K (T_{mb} = 25 °C, T_j = 175 °C) = 150 / 1.3 = 115.38 W, note data sheet P_{tot} is rounded to 115 W.

Maximum R_{DSon} at a die temperature (T_j) of 175 °C = 6.7 mΩ.

Therefore, at steady state with T_{mb} = 25 °C and T_j = 175 °C; P = 115.38 W = I_{max}^2 × R_{DSon}(175 °C).

Therefore:

$$Imax = \sqrt{\frac{P_{(max)175\,°C}}{R_{DSon\,175\,°C}}} = \sqrt{\frac{115.38\,W}{0.0067\,\Omega}}$$ (5)

= 131.23 A (rounded down to 120 A in the data sheet).

Note this value appears on the curve for I_D vs T_{mb} in Fig. 1 but only 120 A is claimed in the data sheet. Practically, limitations are placed on MOSFET performance due to PCB, thermal design and operating temperature, which will all act together to raise the mounting base temperature.

Fig. 8 shows the dependency of R_{DSon} on the gate-source voltage for a standard level MOSFET (e.g. BUK7Y12-55B); the red dashed line shows the curve for a hot device and is indicative of how the dependency changes at a high temperature.

This diagram is for illustrative purposes only and not to be taken as an indication of hot R_{DSon} performance for any device.

Fig. 8. **Drain-source on-state resistance as a function of gate-source voltage at 25 °C and high temperature**
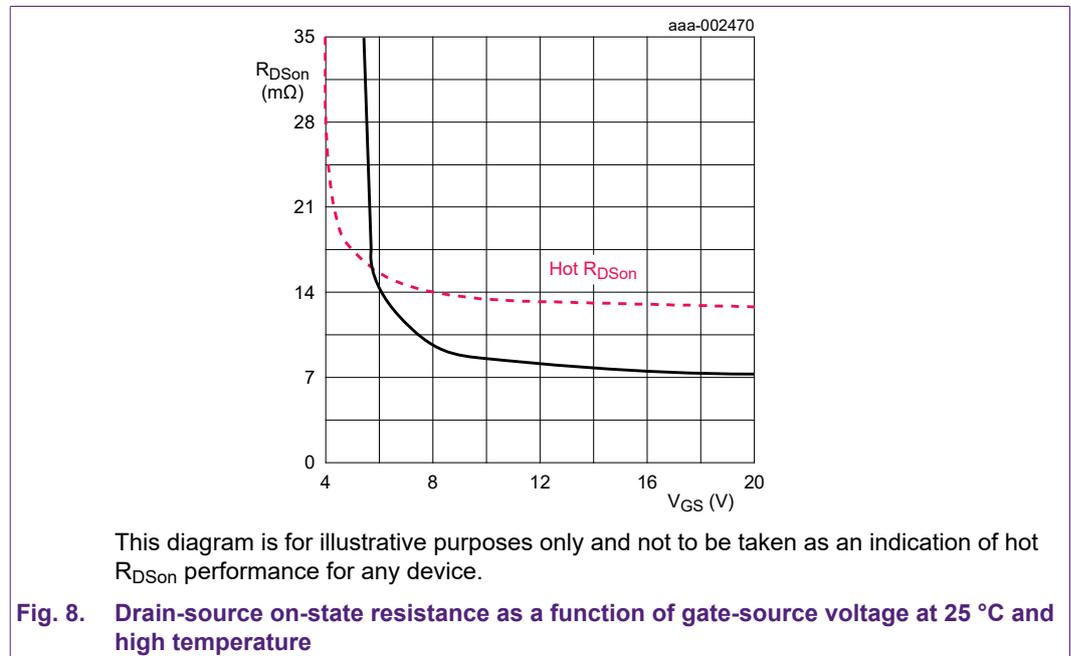
If an application requires good R_{DSon} performance for lower gate-source voltages, then MOSFETs are made with lower threshold voltages, e.g. the BUK9Y12-55B (logic level MOSFET). However, the lower threshold voltage of such a device means that it has a lower headroom for its off-state at high temperature. This lower headroom often means that a device with a higher threshold voltage is needed.

Fig. 9 shows how the ratio of R_{DSon} to R_{DSon} at 25 °C typically varies with junction temperature for BUK7Y3R5-40H.

$$a = \frac{R_{DSon}}{R_{DSon\ 25\ °C}}$$

Fig. 9. **Normalized drain-source on-state resistance factor as a function of junction temperature**
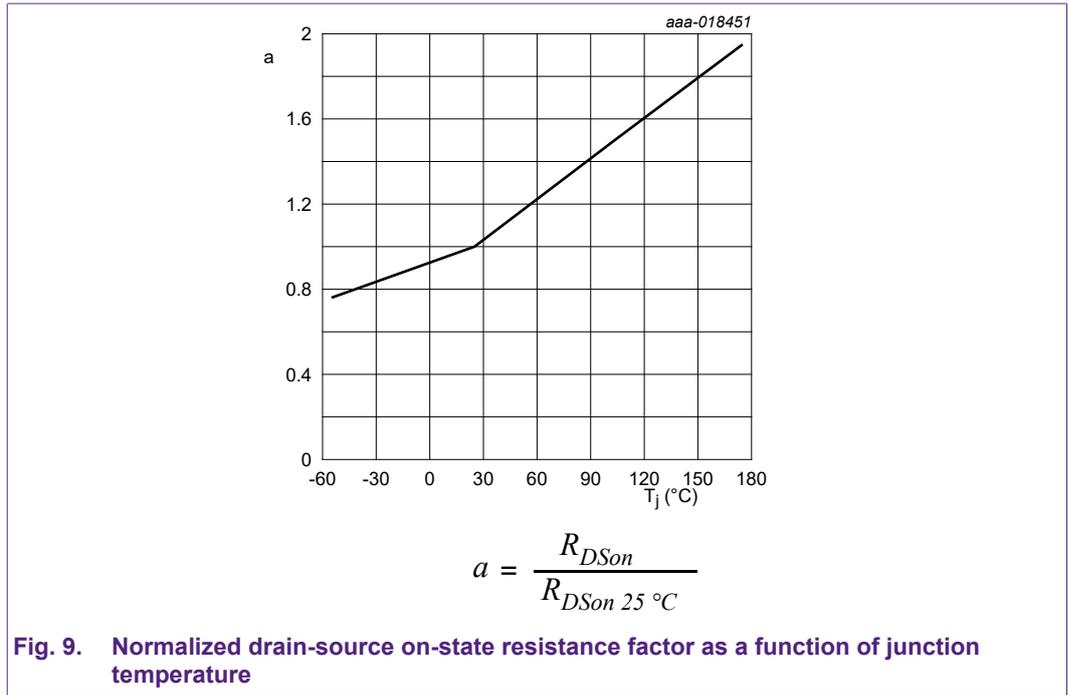
R_G (gate resistance) is the internal series resistance presented to the gate pin. In most applications an external "gate stopper" resistance of a larger value is employed to mitigate gate oscillation and, dependent on value chosen, decrease output slew rate.

2.6.2. Dynamic characteristics

The dynamic characteristics determine the switching performance of the device. Several of these parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions. Table 6 is a sample dynamic characteristics table.

Table 6. Dynamic characteristics

List of constants and limitations relating to the table i.e. voltages, currents and temperatures

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V;		-	31	53	nC
Q_{GS}	gate-source charge			-	10	15	nC
Q_{GD}	gate-drain charge			-	6	15	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C;		-	2294	3441	pF
C_{oss}	output capacitance			-	682	954	pF
C_{rss}	reverse transfer capacitance			-	112	247	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	10	-	ns
t_r	rise time			-	8	-	ns
$t_{d(off)}$	turn-off delay time			-	19	-	ns
t_f	fall time			-	9	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C;		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 V/µs; V_{GS} = 20 V;		-	25	-	ns
Q_r	recovered charge			-	16	-	nC

2.6.2.1. Gate charge

$Q_{G(tot)}$, Q_{GS}, and Q_{GD} are all parameters from the same gate charge curve. They describe how much gate charge the MOSFET requires to switch, for certain conditions. This is particularly important in high frequency switching applications. Much of the power loss occurs during switching, when there are significant voltage and current changes simultaneously between the drain, gate and source. In the blocking state, there are significant voltages but negligible currents. In the full-on state, there are significant currents and small voltages

The gate charge parameters are dependent on the threshold voltage and the switching dynamics as well as the load that is being switched. There is a difference between a resistive load and an inductive load.

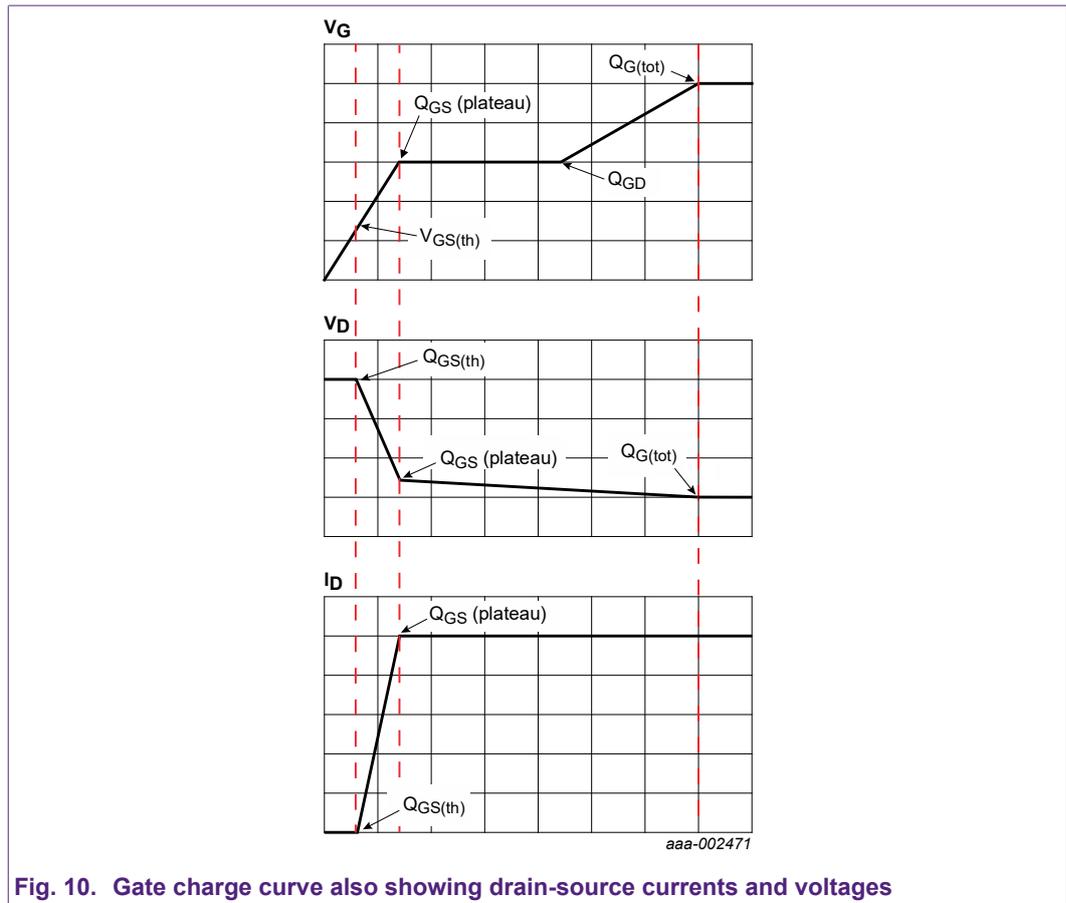An example of a gate charge curve is shown in Fig. 10:

Fig. 10. Gate charge curve also showing drain-source currents and voltages

Due to capacitance variation with voltage and current, it is better to look at the gate charge data rather than the capacitance data when determining switching performance. This is especially true if the gate-driver circuit for the MOSFET is limited to a particular current, and a rapid switch is required.

The gate charge curve describes what happens to a MOSFET which has a drain supply limited to a particular current and voltage. The operation of the test circuit means that during the gate charge curve, the MOSFET is provided with either a constant voltage or a constant current.

During this time, the drain-source voltage begins to fall because the increased charge on the MOSFET allows easier conduction. Consequently, although the gate-source voltage is constant, the drain-gate voltage is falling.

Eventually the capacitance stops increasing and any further increases in gate charge increase the gate-source voltage. This characteristic is sometimes referred to as the "Miller plateau" as it refers to the time during which the so-called Miller capacitance increases. The Miller plateau is also known as the gate-drain charge (Q_{GD}).

During this period, there are significant currents and voltages between the drain and source, so Q_{GD} is important when determining switching losses.

Once the end of the Miller plateau is reached, the gate-source voltage increases again, but with a larger capacitance than before Q_{GS} had been reached. The gradient of the gate charge curve is less above the Miller plateau.

The gate-charge parameters are highly dependent on the measurement conditions. Different suppliers often quote their gate-charge parameters for different conditions, demanding care when comparing gate charge parameters from different sources.

Higher currents lead to higher values of gate-source charge because the plateau voltage is also higher. Higher drain-source voltages, lead to higher values of gate-drain charge and total gate charge, as the plateau increases.

The drain-source currents and voltages during the gate charge switching period are shown in Fig. 10.

If the MOSFET starts in the off state (V_{GS} = 0 V), an increase in charge on the gate initially leads to an increase in the gate-source voltage. In this mode, a constant voltage (V_{DS}) is supplied between the source and drain.

When the gate-source voltage reaches the threshold voltage for the limiting current at that drain-source voltage, the capacitance of the MOSFET increases and the gate-voltage stays constant. This is known as the plateau voltage and the onset charge is referred to as Q_{GS}. The higher the current is, the higher the plateau voltage (see Fig. 11). This relates to the transfer characteristic, see Fig. 15. The transfer curve shows the dependency of drain current on gate voltage. The higher the voltage on the gate the higher the charge applied, ($Q = C \times V$), hence making it the easier for the MOSFET to conduct.
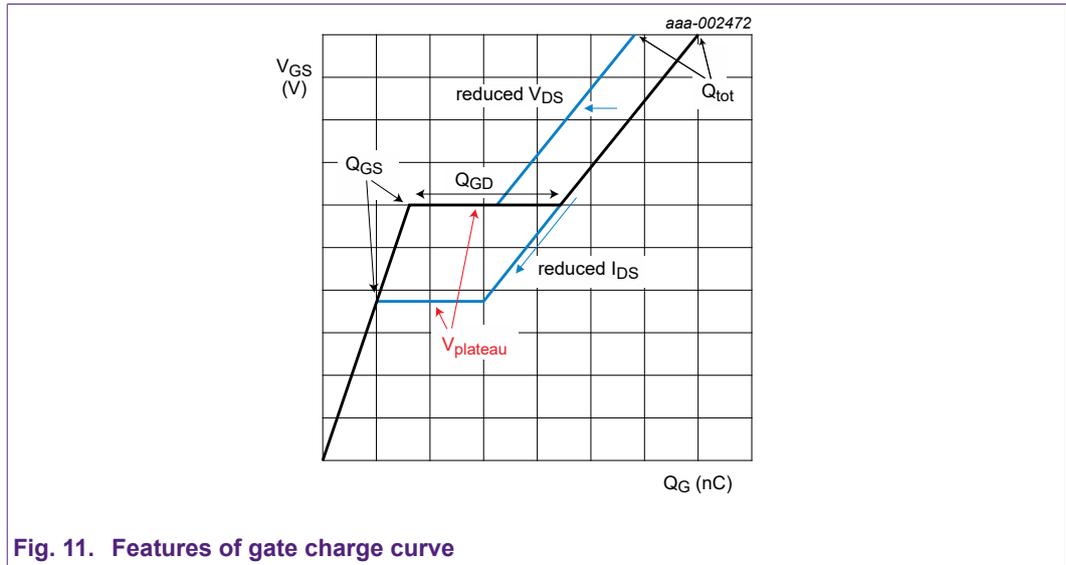
Fig. 11. Features of gate charge curve

2.6.2.2. Capacitances

Capacitance characteristics are generally less useful than the gate charge parameters, for the reasons already discussed. However, they are still listed on data sheets. The three capacitances that are normally listed are as follows:

- **C_{iss}** (input capacitance) is the capacitance between the gate and the other two terminals (source and drain).
- **C_{oss}** (output capacitance) is the capacitance between the drain and the other two terminals (gate and source).
- **C_{rss}** (reverse transfer capacitance) is the capacitance between the drain and the gate.

See Fig. 13.

Semiconductor capacitances generally depend on both voltage and the frequency of the capacitance measurement. Although it is difficult to compare capacitances measured under different conditions, many suppliers specify a measurement frequency of 1 MHz. Consequently, the capacitances vary with drain-source voltage (see Fig. 12). However, the capacitances also vary with gate-source voltage, which is why the gradients in the gate-charge curve vary for different voltages (see Fig. 10).

The relationship between charge, voltage and capacitance in the gate charge curve is:
$\Delta Q = \Delta C \times \Delta V$. For different gradients at different gate voltages, the capacitance changes significantly with gate-source voltage.
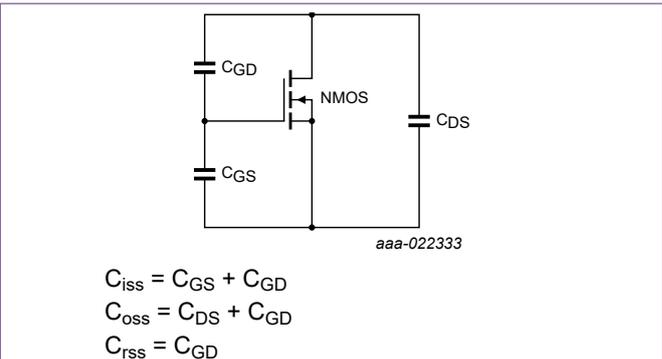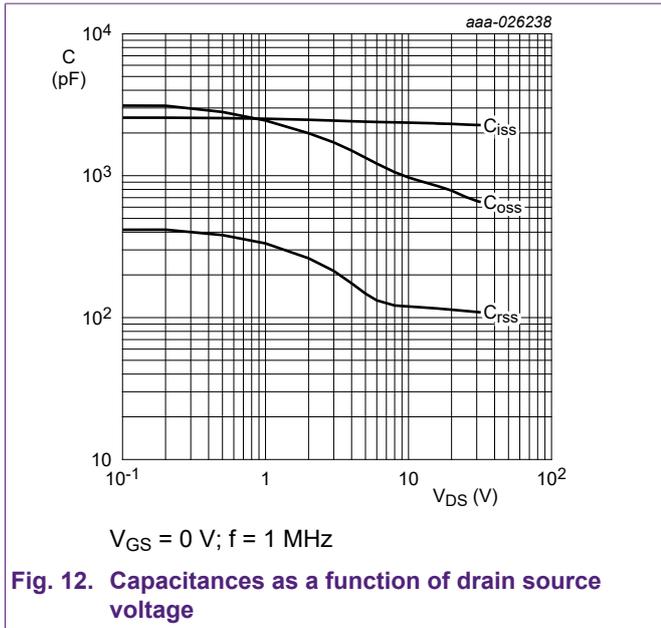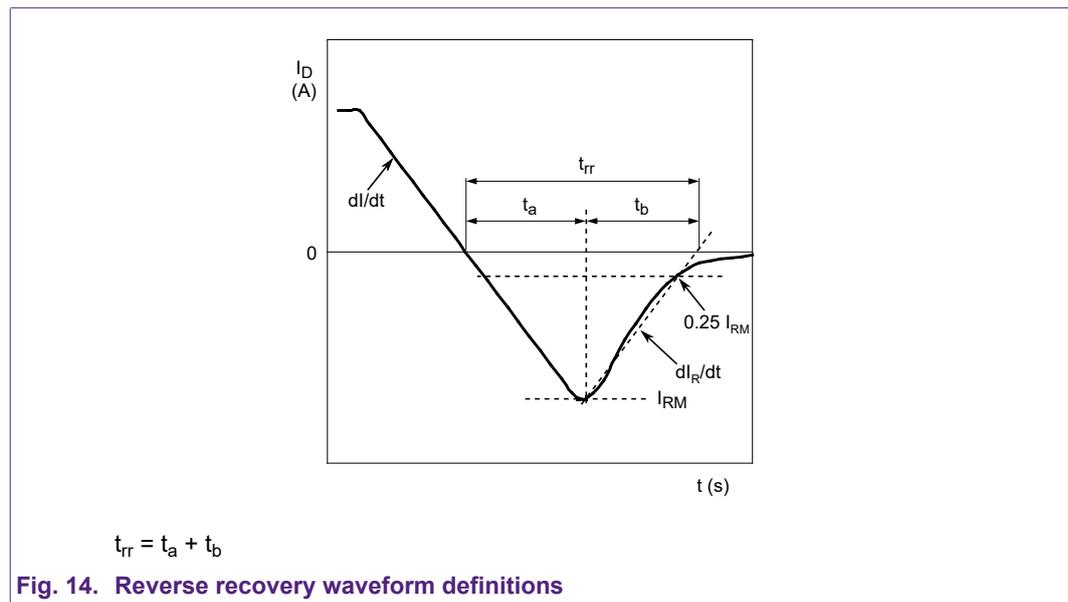
AN11158

application note **Rev. 6.0 — 6 July 2020** **17 / 29**

$V_{GS} = 0$ V; f = 1 MHz

Fig. 12. Capacitances as a function of drain source voltage

$C_{iss} = C_{GS} + C_{GD}$
$C_{oss} = C_{DS} + C_{GD}$
$C_{rss} = C_{GD}$

Fig. 13. MOSFET capacitance parameters

2.6.2.3. Switching times

Most manufacturers quote resistive load switching times. However, extreme care is needed when comparing data from different manufacturers, as they are highly dependent on the resistance of the gate drive circuit used for the test and in the case of logic level devices, the gate voltage applied. In devices for fast switching applications, the gate resistance of the MOSFET is often quoted as capacitive time constants which are equally dependent on resistance and capacitance.

2.6.2.4. Diode characteristics

The diode characteristics are important if the MOSFET is being used in the so-called "third quadrant". The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery (Fig. 14) contributes to the power losses as well as oscillation and voltage spikes, which can cause EMC concerns.

$t_{rr} = t_a + t_b$

Fig. 14. Reverse recovery waveform definitions

AN11158

application note **Rev. 6.0 — 6 July 2020** 18 / 29

2.6.2.5. Transfer characteristics

Fig. 15 shows the transfer characteristics of the MOSFET which indicate the theoretical drain current that can be handled by the device as a result of applied gate to source voltage. The graph shows the temperature dependency of the characteristic. The convergent point indicates where the current is dependent only on gate voltage and not temperature hence the MOSFET's Zero Temperature Coefficient point I_ZTC. Gate charge test current and plateau voltage (refer to Fig. 10) can be directly read from the transfer curve.

V_{DS} = 12 V
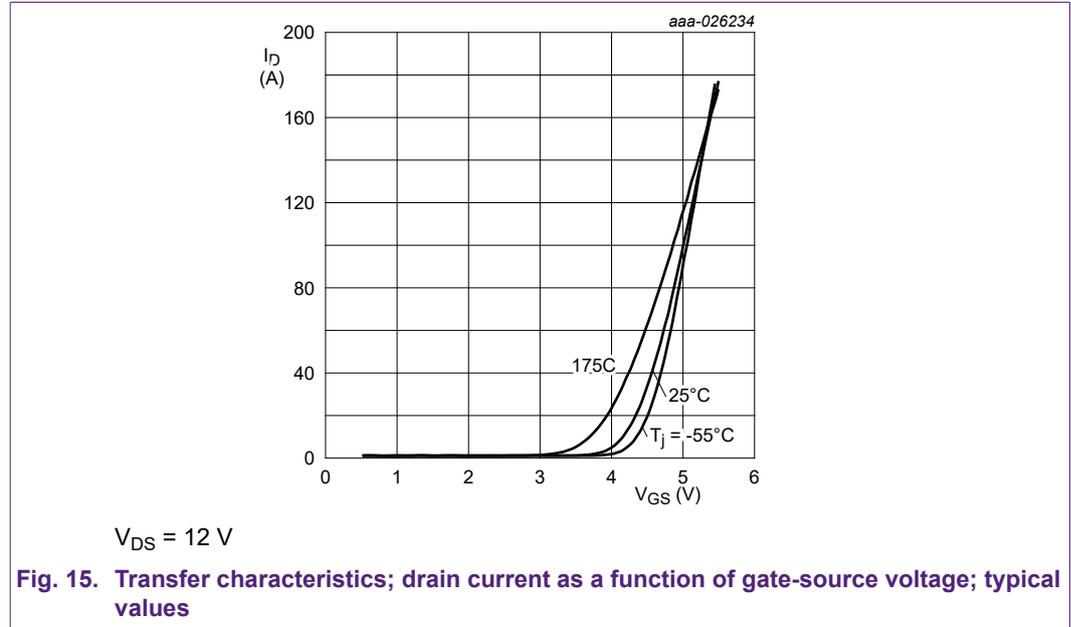
Fig. 15. Transfer characteristics; drain current as a function of gate-source voltage; typical values

2.7. Package outline

This section describes the package outline dimensions and tolerances.

3. Appendices

3.1. Safe Operating Area (SOA) curves

To highlight the key features, Fig. 16 provides an idealized SOA curve for a hypothetical MOSFET. Data for a hypothetical MOSFET for a single pulse length, is shown to highlight the region where it deviates from the ideal curve.

1. R_{DSon} limit (V_{DS}/I_{DS} is constant)
2. Maximum pulsed drain current (I_{DS} is constant)
3. Maximum pulsed power dissipation ($V_{DS} \times I_{DS}$ is constant)
4. Maximum allowed voltage (V_{DS} is constant)
5. Linear mode derating - a departure from the ideal behavior shown in (3) due to operation within a regime of positive feedback, and potential thermal runaway
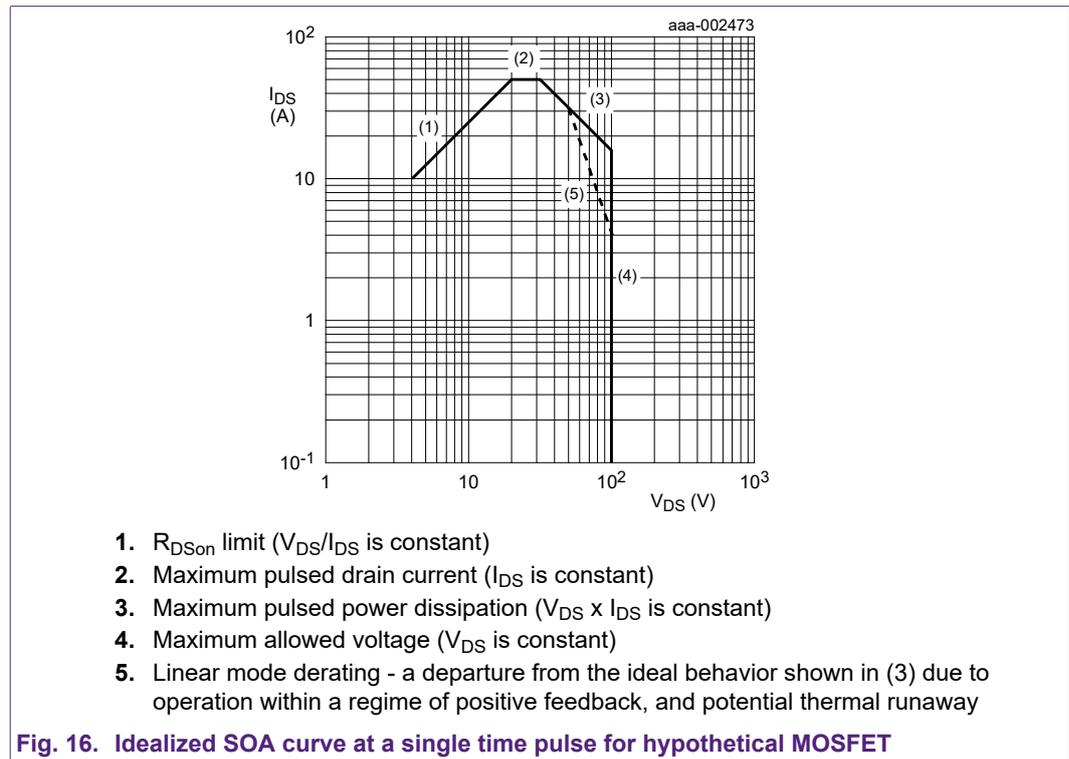
Fig. 16. Idealized SOA curve at a single time pulse for hypothetical MOSFET

The dashed line (5) is to emphasize where the curve deviates from the ideal. In reality, there is a single curve with a change of gradient where the linear mode derating becomes important.

R_{DSon} limit

R_{DSon} is region (1) of the graph and Equation (6) represents the limiting line:

$$\frac{V_{DS}}{I_{DS}} \leq R_{DSon(max)} \ (175 \ °C) \tag{6}$$

The limit is when the MOSFET is fully on and acting as a closed switch with a resistance that is no greater than the hot R_{DSon}.

Constant current region

The constant current region is region (2) of the graph. It is the maximum pulsed drain current, which is limited by the device manufacturer (for example, the wire-bonds within the package).

Maximum power dissipation (linear mode) limit

In this region, the MOSFET is acting as a (gate) voltage-controlled current source. This means that there are significant voltages and currents applied simultaneously, leading to significant power dissipation. Line (3) shows the idealized curve, whereas the dotted line (5) shows where it deviates from the ideal.

The limiting factor for the SOA curve in region (5), is the heating applied during a rectangular current and voltage pulse. Even in the ideal situation, this curve depends on the transient thermal impedance of the MOSFET, which is covered in Section 2.5.

The transient thermal impedance varies with the pulse length. This is due to the different materials in the MOSFET having different thermal resistances and capacities. The differences create a thermal equivalent to an RC network from the junction (where the heat is generated) to the mounting base. Equation (7) is the calculation used to determine the ideal curve in this region.

$$P = I_D \times V_{DS} = \frac{T_{j(max)} - T_{mb}}{Z_{th(j-mb)}} = Constant \qquad (7)$$

The ideal situation accurately describes the situation for sufficiently high current densities. However, it is overly optimistic for low current-densities, i.e. towards the bottom right of region (3). Low current densities and high voltages can lead to thermal runaway in the linear mode operation. Thermal runaway is discussed in the following section.

Thermal runaway in linear mode

Power MOSFETs are often considered to be immune to thermal runaway due to the temperature coefficient of resistance, which means that as temperature rises, current falls.

This is only true for MOSFETs that are fully on (i.e. in region 1), but it is not the whole story.

When a MOSFET is turned on, there are two competing effects that determine how its current behaves with increasing temperature. As the temperature rises, the threshold voltage falls. The MOSFET is effectively turned on more strongly, thereby increasing the current. In opposition, the resistance of the silicon increases with increasing temperature, thereby reducing the current. The resultant effect for a constant drain-source voltage, is shown in Fig. 17. This situation occurs when the gate-source voltage of a MOSFET is being used to control the current, or when the MOSFET is switched sufficiently slowly.
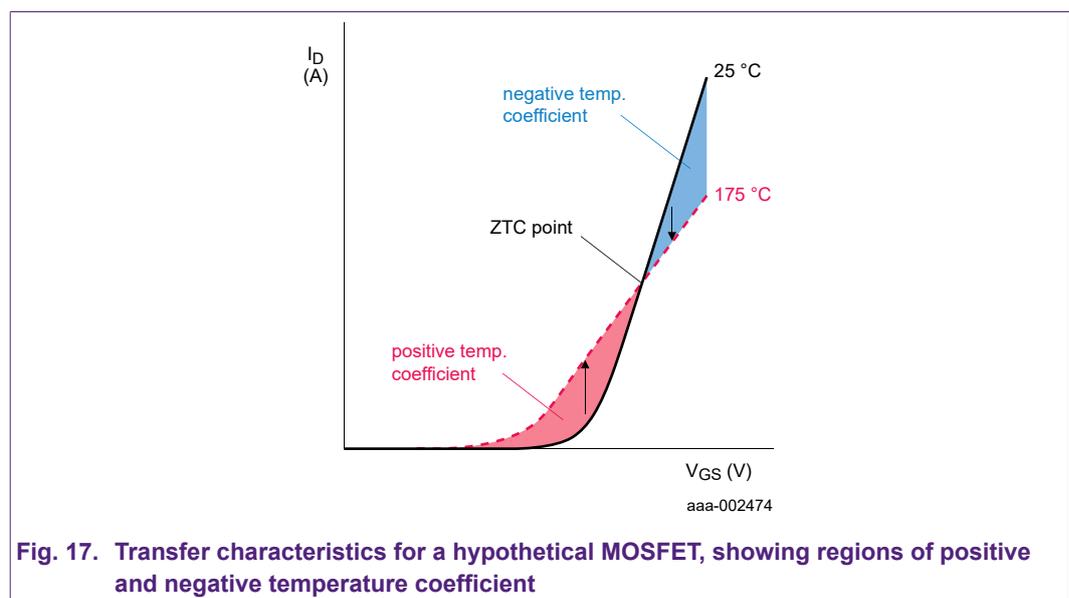

Fig. 17. Transfer characteristics for a hypothetical MOSFET, showing regions of positive and negative temperature coefficient

The resistance increase dominates at high currents, meaning that localized heating leads to lower currents. The threshold-voltage drop dominates at low currents, meaning that localized heating lowers the threshold voltage. This condition effectively turns on the device more, leading to higher currents and a risk of thermal runaway.

Consequently, for a given V_{DS}, there is a critical current below which there is a positive-feedback regime and a subsequent risk of thermal runaway. Above this critical current, there is negative feedback and thermal stability. This critical current is known as the Zero Temperature Coefficient (ZTC) point.

This effect reduces the SOA performance for low currents and high drain-source voltages. The constant power line must be reduced as shown in region (5). For short switching events, this effect is insignificant. However, as the duration of the switching event becomes longer, for example to reduce electromagnetic interference, the effect becomes more important and potentially hazardous.

Voltage-limited region

The device is limited by its breakdown voltage V_{DS} which is shown in region (4). The quick reference data provides values for V_{DS} at temperatures of 25 °C and above. In the hypothetical MOSFET shown in Fig. 16, the rating is 100 V. For the BUK7Y3R5-40H, the voltage is 40 V.

3.1.1. Safe operating area for temperatures above 25 °C

When reading from the SOA curves there are two main considerations:

1. The mounting base temperature is at 25 °C
2. The MOSFET is exposed to a rectangular power pulse

The SOA curves indicate the pulse power required to raise the MOSFET junction temperature, T_j, from 25 °C to its maximum rating of 175 °C, $T_{j(max)}$. The assumption being T_j is at the mounting base temperature T_{mb} = 25 °C when power dissipation begins.

Under DC conditions, where a product has been operating for some time (thermally soaked), T_j will be close to the mounting base temperature, T_{mb}.

Under high power short duration pulse conditions T_j, can be much greater than T_{mb}.

A reduction in MOSFET power handling capability results if the initial T_{mb} > 25 °C, so it is important to establish an accurate temperature for T_{mb} to determine T_j which is non-trivial activity.

The majority of automotive power applications thermally link the MOSFET mounting base via the PCB footprint and an electrically isolating barrier to a metallic mass (e.g. product housing) to act as a heatsink. Heatsink temperature T_{hs} is in turn thermally linked to the product's ambient temperature, T_{amb}, which may be 85 °C for in-cabin (inside the driver compartment) or 105 °C for under the hood (near and around the engine). In some automotive applications where, for example, the housing is mounted directly to the power train the customer may specify a temperature directly on the heatsink where $T_{hs} \geq 105$ °C.

Unless the offset relationship T_{mb} > T_{amb} is well defined by thermal flow modelling and test verification, the designer can only estimate T_{mb}.

It is important to remember that in a product which has been operating for some time (thermally soaked) MOSFETs which have similar thermal linkages to the same heatsink will have a similar T_{mb}, whether the MOSFET is switched on or switched off.

Calculation to determine the rise in die temperature above mounting base temperature is given below, see Equation (8).

$$T_{j(rise)} = T_{j(max)} - T_{j(mb)} = P_{peak} \cdot Z_{th(t)} \tag{8}$$

Where:

P_{peak} is the peak power, as this is a rectangular pulsed waveform.

$Z_{th(t)}$ is the thermal impedance value between junction and mounting base for a pulse of t seconds duration.

Note: In DC applications, (where the MOSFET is not pulsed), use $R_{th(j-mb)}$ instead of $Z_{th(j-mb)}$. Generally, for pulses above 100 ms, Z_{th} is indistinguishable from R_{th}.

Equation 8 assumes heating is uniformly spread across the whole die. A combination of higher V_{DS} with lower I_{DS} and pulse durations ≥ 100 µs can cause hot spotting (uneven heating) to occur known as the Spirito effect. Refer to TN00008 Section 5 for further details.

3.1.1.1. Example calculations

Calculate the max DC I_{DS} for BUK7Y3R5-40H, with V_{DS} = 10 V at 25 °C

Rewrite Equation (10) to bring out I_{DS} as the main subject (Power is substituted by $I_{DS} \times V_{DS}$). Since Equation (10) is being used for a DC situation, the $Z_{th(t)}$ parameter used in Equation (8) and Equation (9) is replaced by the R_{th} steady state condition.

$$T_{j(rise)} = I_{DS} \times V_{DS} \times Z_{th(t)} \tag{9}$$

$$\frac{T_{j(rise)}}{V_{DS} \times R_{th}} = I_{DS} \tag{10}$$

$$\frac{175\ °C - 25°C}{10\ V \times 1.3\ K/W} = 11.3\ A \tag{11}$$

When making these calculations always refer to the Safe Operating Area Curve for the device. The SOA curve for the BUK7Y3R5-40H is Fig. 4 which can be found in Section 2.4.4. The intersection of I_D = 11.3 A and V_{DS} = 10 V occurs above the DC curve and therefore this condition exceeds device capability. The reason being heat distribution is non-uniform within the die. In other words hot spotting is present, otherwise known as the Spirito effect.

The BUK7Y3R5-40H SOA curve shows for a DC condition the Spirito effect for this device (the point at which a gradient change occurs) is evident at V_{DS} = 0.94 V for I_D= 120 A. As I_D reduces, the allowable V_{DS} increases and by I_D = 11.3 A the maximum permissible V_{DS} = 4.4V. Thermal consideration are discussed further in Section 3.1.2.

3.1.2. Example using the SOA curve and thermal characteristics

Consider the following application during linear mode operation:

* I_{pulse} = 20 A
* V_{pulse} = 30 V
*   f = 2 kHz
* t_{pulse} = 100 µs
* T_{amb} = 25 °C

3.1.2.1. Calculation steps

The SOA curve (Fig. 4) is initially checked to see whether any single pulse would cause a problem. Observing the SOA curve, it can be seen that the 20 A, 30 V pulse lies between the 100 µs and 1 ms lines. This indicates that the pulse lies within acceptable limits.

The duty cycle for the pulses is now calculated using a frequency of 2 kHz for 100 µs pulses. These values give a duty cycle of 0.2. The Z_{th} curve (Fig. 5) indicates that for 100 µs, the line with the duty cycle (δ) has a transient thermal impedance of 0.35 K/W.

The power dissipation for the square pulse is 20 A × 30 V, which equals 600 W.

Using Equation (8), the temperature rise for the 100 µs pulse is calculated as being 600 W × 0.35 K/W, which equals 210 K. With a starting temperature of 25 °C, the temperature rise results in a

finishing temperature of 235 °C. As the MOSFET junction temperature must not exceed 175 °C, the MOSFET is not suitable for this application.

If the application requires a single pulse, then the curve shows that the transient thermal impedance for a 100 μs pulse is 0.12 K/W. As a result, the temperature rise is 600 W × 0.12 K/W which equals 72 K. The finishing temperature is then 97 °C for a starting temperature of 25 °C. The device is able to withstand this, thereby confirming what the SOA curve already indicated.

3.1.2.2. Derating for higher starting temperatures

The example Safe Operating Area calculations were performed for a mounting base temperature of 25 °C. At higher mounting base temperatures, the SOA curves must be de-rated, as the allowed temperature rise in the junction is reduced. The allowed power of the pulse is reduced proportionally to the reduced temperature rise. For example, with a mounting base temperature of 25 °C, the allowed temperature rise is 150 °C. At 100 °C, the allowed temperature rise is half of that (75 °C). The allowed power is half of that allowed at 25 °C.

The allowed drain current is de-rated while the allowed drain-source voltage is maintained.

The I_D derating of the SOA curve at 100 °C is shown in Fig. 18.

T_{mb} = 25 °C; I_{DM} is a single pulse
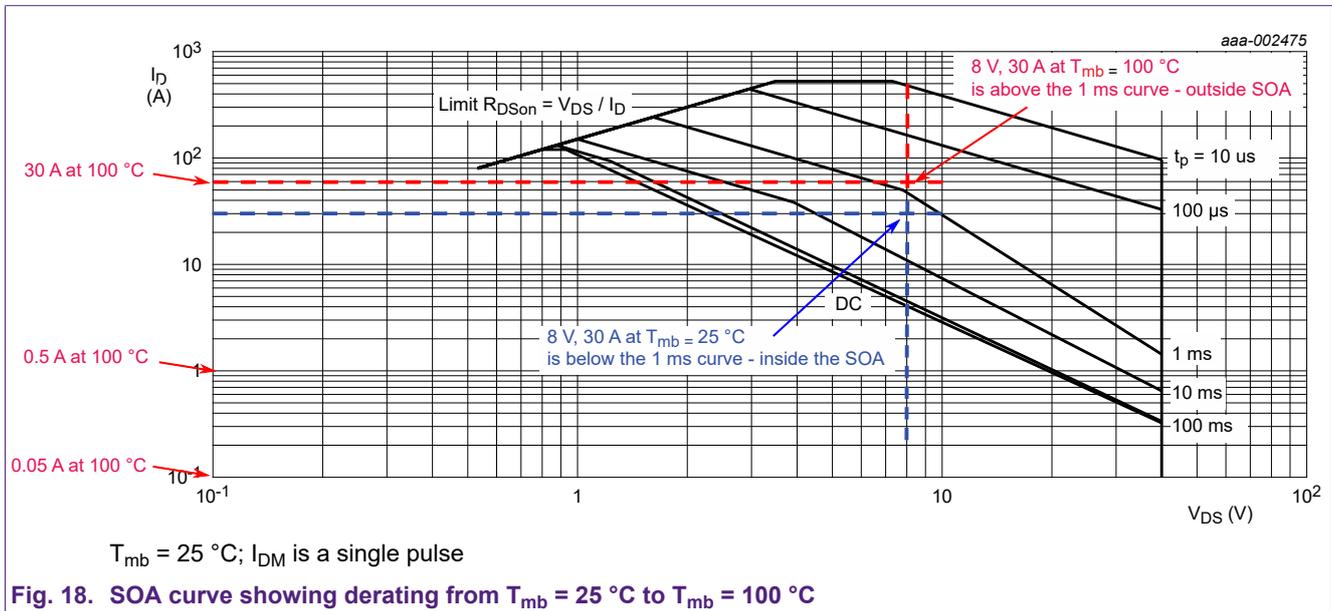
Fig. 18. SOA curve showing derating from T_{mb} = 25 °C to T_{mb} = 100 °C

Example:

Is a 1 ms pulse of 30 A and 8 V allowed at 100 °C?

See Fig. 18, the intersection of the blue lines of the rectangular power pulse I_D = 30 A * V_{DS} = 8 V below the 1 ms curve indicates that the device can safely handle this pulse with T_{mb} = 25 °C .

Power handling capability halves with T_{mb} = 100 °C. In Fig. 18 the red text shows I_D at 100 °C is half the value at 25 °C.

The intersection of the red lines of the rectangular power pulse I_D = 30 A * V_{DS} = 8 V above the 1 ms curve indicates the device cannot handle this pulse at T_{mb} = 100 °C.

AN11158

application note **Rev. 6.0 — 6 July 2020** **24 / 29**

4. References

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2. Semiconductor Devices - Physics and Technology S.M.Sze, 1985, John Wiley and Sons.
3. Nexperia application note *AN10273* - Power MOSFET single-shot and repetitive avalanche ruggedness rating.
4. Nexperia application note *AN10874* - LFPAK MOSFET thermal design guide.
5. Nexperia application note *AN90001* - Designing in MOSFETs for safe and reliable gate-drive operation.
6. Nexperia technical note *TN00008* - Power MOSFET frequently asked questions and answers.

5. Abbreviations

Table 7. Abbreviations

Acronym	Description
AEC-Q101	Automotive Electronics Council Quality System (applicable to MOSFETs)
IEC	International Electrotechnical Commission
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board [1]
SOA	Safe Operating Area
ZTC	Zero temperature coefficient

[1] For the purposes of this application note; FR-4 a flame retardent composite of woven fibreglass and epoxy resin binder.

6. Revision history

Table 8. Revision history

Revision number	Date	Description
6.0	20200706	Section 3.1.2.2 updated.
5.0	20200406	Document updated to reference the BUK7Y3R5-40H data sheet; other minor editorial changes.
4.0	20140204	Equation (2) corrected
3.0	20130107	Figure cross reference correction and temperature qualifier added on page 10
2.0	20120816	Second release
1.0	20120416	Initial release

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AN11158

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application note

Rev. 6.0 — 6 July 2020

26 / 29

List of Tables

AN11158

application note Rev. 6.0 — 6 July 2020 27 / 29

List of Figures

AN11158

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application note

Rev. 6.0 — 6 July 2020

28 / 29

Contents