



AN90021

Power GaN technology: the need for efficient power conversion

Rev. 2.0 — 14 August 2020

application note

Document information

Information	Content
Keywords	GaN FET
Abstract	Power Gallium Nitride(GaN) technology shows the greatest performance benefits against other incumbent technologies including silicon (Si) technology. This application notes details the scalability and growth of the technology as well as the quality and reliability of Nexperia GaN FETs. The performance of GaN FET power switches in various applications is examined.

1. Introduction

The biggest motivation and driver for semiconductor power device innovation is improved efficiency in power conversion. Power Gallium Nitride (GaN) technology shows the greatest performance benefits against other incumbent technologies, including silicon (Si) technology. A reduction in power losses is the key challenge industries are facing. Pressure from society and government legislation for reduced CO₂ emission are all trending towards more efficient power conversion and electrification.

Automotive electrification, telecom infrastructure, server storage and industrial automation using power electronics are the biggest trends in the technology sector. GaN field-effect transistors (FETs) can enable us to achieve the best efficiency with lower system costs while making the system lighter, smaller and cooler. Specifically, electrification in the automotive sector can be the biggest beneficiary of this new power GaN FET technology.

To make all-electric vehicles (xEVs) a real replacement for vehicles that have fossil-fuelled internal combustion engines, efficient power conversion is key. There are many challenges, such as range anxiety, harmful emissions, power losses, heat dissipation, cooling systems, system weight and power densities. On this journey, industry is working in many ways to address these major issues to reduce range anxiety and harmful emissions. These are integral parts to make the xEV platforms a commercial and social reality.

Application areas in which there is a drive for significant improvement include:

- Improved more efficient power conversion
 - AC-to-DC onboard charging
 - DC-to-DC power conversion
 - DC-to-AC inverter to drive the traction motors
 - Improved power density
 - Simpler driver and control scheme
- Improved traction motors
 - Improved efficiency
 - Better torque and power
 - Lower losses
 - Higher dV/dt handling
- Improved batteries, storage and battery management systems

Efficient power conversion helps significantly in many ways. An example is a 200 kW inverter with 95% efficiency versus 99% efficiency. The reduction in power loss at full load is from 10 kW to 2 kW, about one-fifth, meaning a significant decrease in the size and rating of the cooling system. Not only is the loss 8 kW lower, (which can be effectively used for traction power), but the smaller cooling system can also help with reducing the cooling energy consumption and with size and weight. Hence, a longer range or smaller battery can be achieved.

This highlights the importance of achieving very high efficiencies. Power GaN FETs based on GaN on Si epitaxy (epi) help significantly in this area, not only by offering higher efficiency but also the most desirable scalability for growth to support the xEV growth ambitions. The simple Si fabrication (fab) process steps also allow the best cost roadmap for commercial viability. Power GaN technology currently serves with 650 V products for 400 V battery voltage and can serve up to 800 V battery systems with up to 1,200 V power GaN devices. The power range can be up to 300 kW.

2. Power GaN FET switches

High-voltage (HV) power semiconductor switches are the fundamental building blocks of any power conversion. Si-based insulated-gate bipolar transistors (IGBTs) are currently dominating this market with significant maturity in the absence of any better alternatives. The improvement of Si IGBTs and combining them with silicon carbide (SiC) diodes helps to achieve incremental higher efficiencies, but has a limit on how much further improvement is possible. Si IGBTs are fundamentally limited in frequency of operation, speed and poor high-temperature performance along with poor low-current characteristics. Si super-junction (SJ) technology is dominating power conversion at higher frequencies like AC-to-DC power factor correction (PFC) and DC-to-DC power conversion. To achieve higher efficiency, these devices are fundamentally limited to size and cost due to their inherent material limitation for high-frequency operation. These limitations can be summarised by switching crossover losses, conduction, and reverse recovery losses.

In contrast however, wide band-gap (WBG) materials like GaN and SiC, as summarized in [Table 1](#) are free from reverse recovery loss and can offer very low switching cross-over losses (due to very fast turn on and off characteristics) and lower conduction losses. WBG materials with a higher critical electric field and higher mobility together give the lowest drain source on-state resistance ($R_{DS(on)}$) for higher voltages and a significantly better switching figure of merit. The WBG devices beginning to enter the market show significant promise and remove many of the limitations naturally imposed by Si IGBT and Si SJ devices. Some of the difficult switched-application topologies where Si SJ FETs cannot be used due to diode reverse recovery can easily use power GaN FETs and take full advantage of the reduced component counts and higher efficiency with simpler control schemes. The faster switching speeds and higher frequencies of operation enabled by GaN power transistors help improve signal control, higher cutoff frequencies for passive filter designs, and lower ripple currents, allowing for smaller inductors, capacitors, and transformers. Consequently, the compact and smaller system solution offers cost savings.

Table 1. Material properties

Material	Band Gap (eV)	Critical Electric Field E_c (MV/cm)	Electron mobility μ_0 (cm^2/Vs)	Thermal conductivity (W/cmK)	Saturation velocity (cm/s)
GaN	3.4	3.5	2,000	1.3	2.5×10^7
SiC	3.3	2.2	950	3.7	2×10^7
Si	1.12	0.23	1,400	1.5	1×10^7

There are two main options for current power GaN FETs: enhancement mode (E-mode) or single die normally off devices and depletion mode (D-mode) or two-die normally off devices. The stability and leakage currents of the E-mode gates are of concern but the two-die normally off or cascode configuration currently offers peace of mind as driving these FETs is simple and robust. The E-mode device drive is complex, especially for HV, high-power applications. For these applications, to avoid gate bounce and harmful shoot-through situations, it is necessary to have a high gate threshold voltage and stable gate drive without worrying about overdrive, which currently is not achievable with existing E-mode technologies. For operations up to 1 MHz switching frequency, cascode GaN FETs are best suited, although current HV power-conversion frequencies are around only 300 kHz and traction inverter frequencies are still below 40 kHz. The GaN on Si two-die normally off configuration allows significant design flexibility. Nexperia GaN FET offers a ± 20 V gate rating with an oxide/insulator gate, 4 V gate threshold voltage with 0 V turn off, and low gate charge. Hence, simple Si drivers are suitable for use with these devices and for 0 – 8, 10, or 12 V, any gate drive can be used. In contrast, the SiC technology generally requires at least 15 V, a very-high-current driver with a negative gate drive capability to turn off the device adds costs for the driver and increased driver and switching losses. Nexperia GaN also brings a very good anti-parallel diode built-in that helps with the robust freewheeling conduction path. The cascode version offers significant freedom to make the gate structure have the same robustness that automotive customers are used to. This is valid for both Si FET and the GaN high electron mobility transistor (HEMT) with insulated gates.

Power GaN technology: the need for efficient power conversion

Fig. 1 shows the cross-section for the GaN HEMT, which works with the formation of the 2D electron gas (2DEG) due to the spontaneous and piezoelectric polarization combined at the interface of GaN and $Al_xGa_{1-x}N$. GaN Epi is formed on the Si substrate via the seed layer and a graded layer of GaN and AlGaN layers before the pure GaN layer grows. A thin layer of AlGaN then forms the 2DEG. Electron mobility in this layer is very high, hence the name.

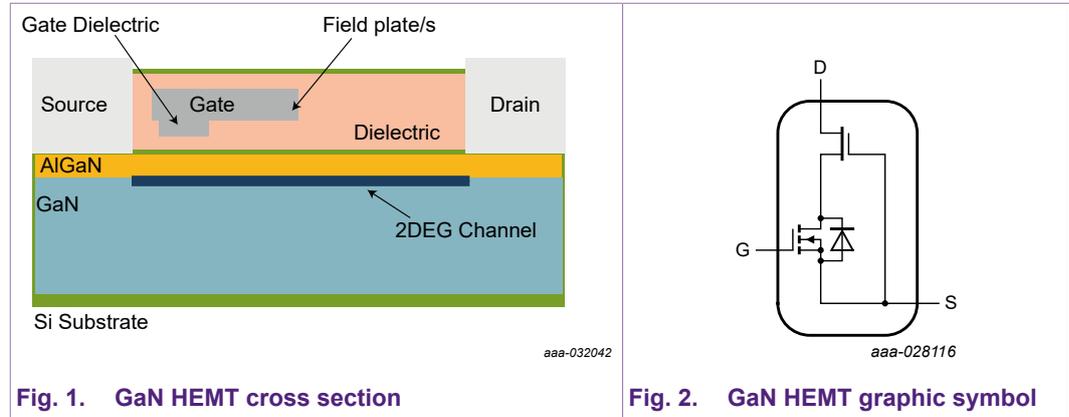
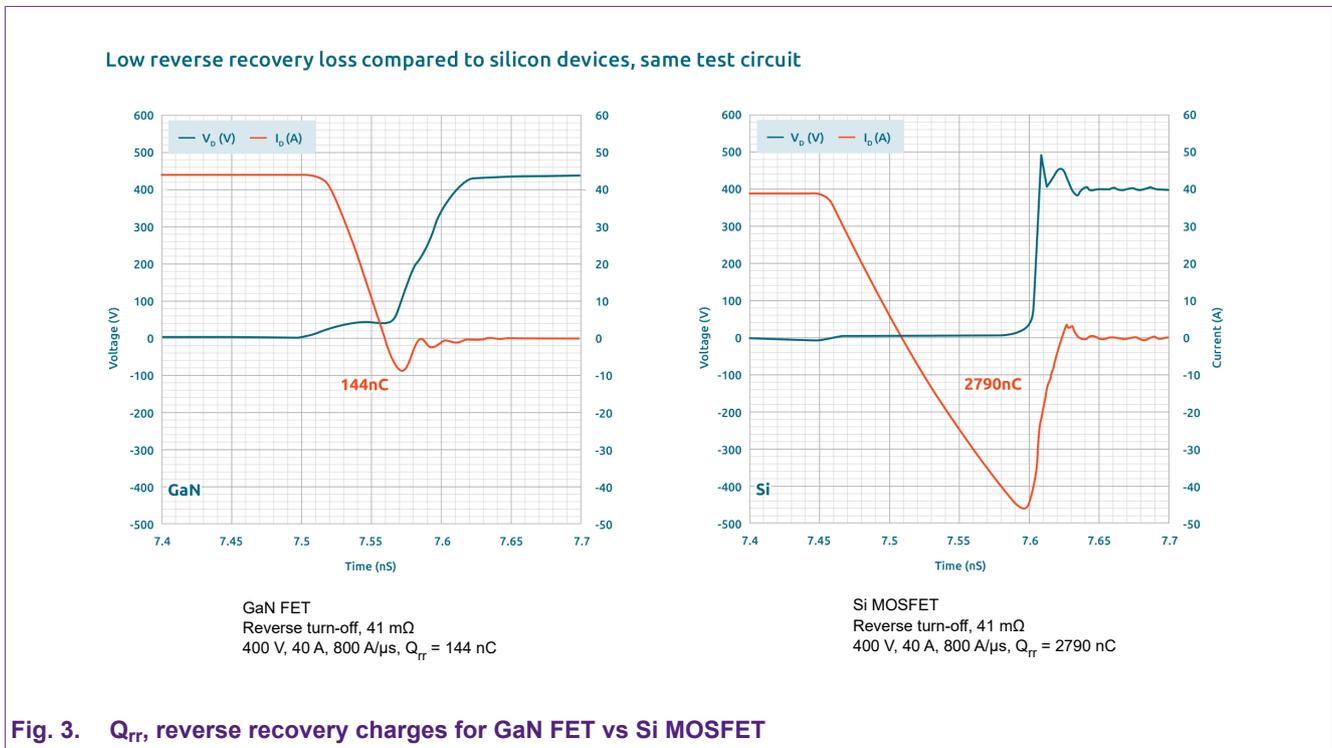


Fig. 2 shows how combining a low-voltage (LV; 30 V) robust Si MOSFET with the cascode configuration can eliminate all of the major concerns regarding the poor gate structures of the E-mode devices and make the entire usage very simple. An LV Si-based gate structure is a very mature technology and engineers are accustomed to using them.

The reverse recovery charge (Q_{rr}) for the cascode power GaN is very low as shown in Fig. 3 and mostly capacitive and allows the full potential of the power GaN technology. Actual reverse recovery charge (Q_{rr}) for the LV Si FET used here is only ~12 nC. The E-mode device channel mobility is much lower compared to the channel mobility in a D-mode GaN HEMT channel.



Driving a cascode device is also very simple. Cascode device operation is shown in Fig. 4 and Fig. 5 for different bias situations. Power GaN FETs can be used in a bi-directional form and also allow simpler bi-directional power conversion.

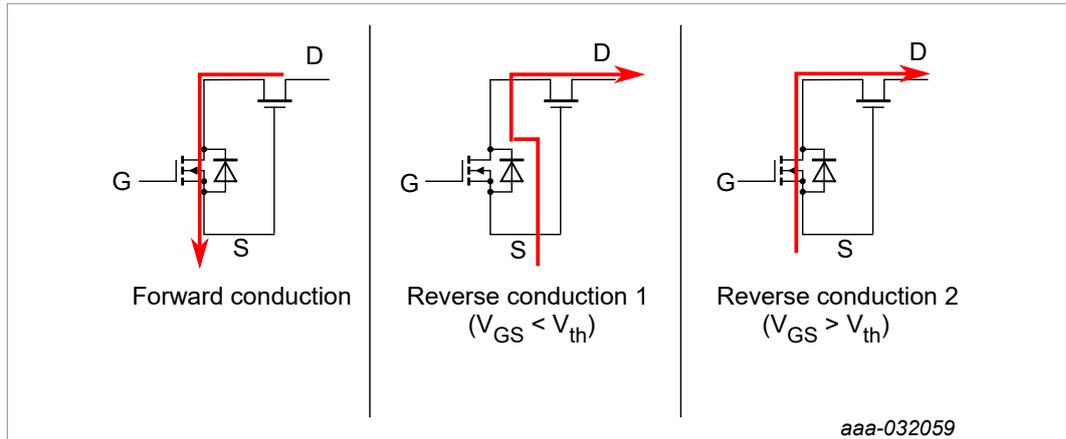


Fig. 4. GaN FET operation

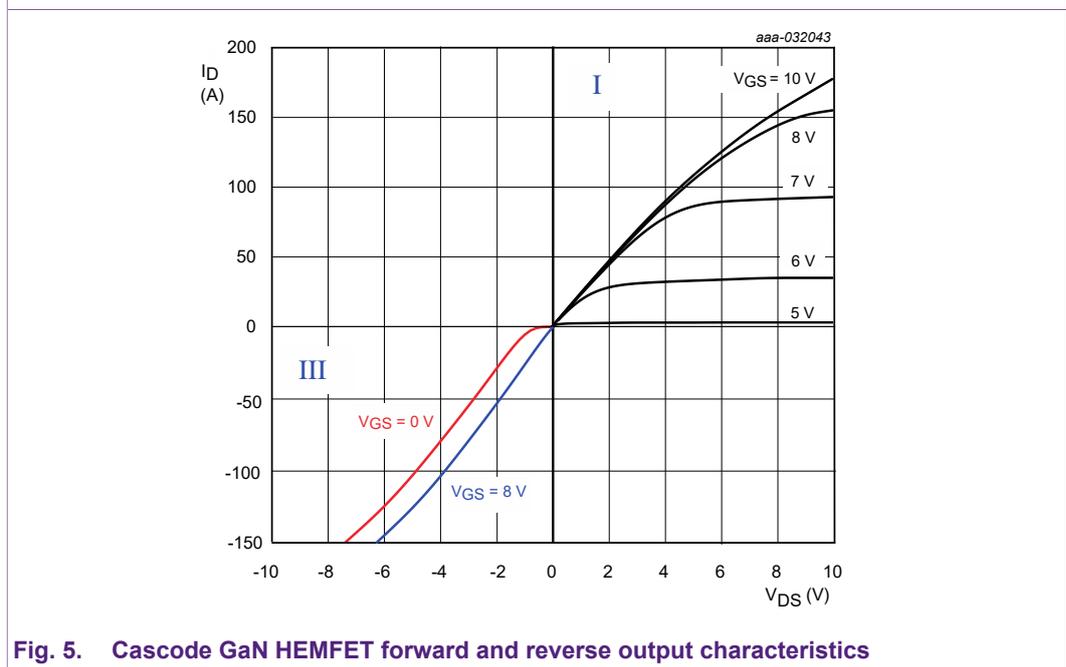


Fig. 5. Cascode GaN HEMFET forward and reverse output characteristics

Since power GaN transistors were introduced to the market, significant improvements in performance, reliability, cost, and availability have taken place. More capable GaN power transistors are becoming available to drive higher power to be compatible with the EV requirements while being well positioned for applications in data centres, telecom infrastructures and industrial.

3. Scalability and growth

Si wafers are widely available in different sizes. GaN on Si wafers allow us to use 150 mm, 200 mm metal organic chemical vapor deposition (MOCVD) reactors for epi growth and can be processed in mature silicon semiconductor fabs. There is a lot of Silicon fab capacity that can be utilised. Processing is similar to standard Si processing, which is not so complex. Tremendous growth potential is better addressed with power GaN technology on Si which is at the correct cost point.

4. Applications and performance

Whether it is AC-to-DC PFC stage, a DC-to-DC converter Fig. 6 or traction inverter Fig. 7 the basic building block for most topologies is a half-bridge (Fig. 9). Hence when GaN FETs are compared against Si FETs in a simple boost converter, then the GaN FET shows its superior performance due to the differences in material properties (Fig. 8). All of these applications can take advantage of these benefits and hence reduce losses. The advantages of power GAN FETs compared to Si IGBTs are clearly shown by light load performance, high temperature and high frequency operation where the Si IGBT losses are comparatively high.

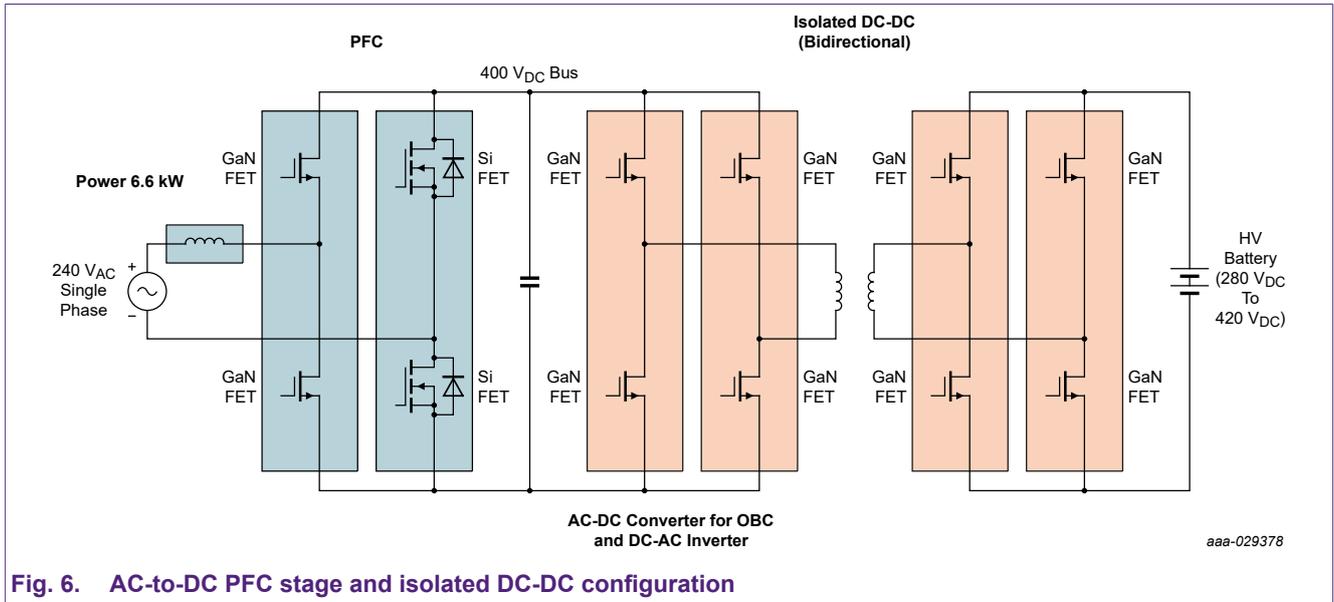


Fig. 6. AC-to-DC PFC stage and isolated DC-DC configuration

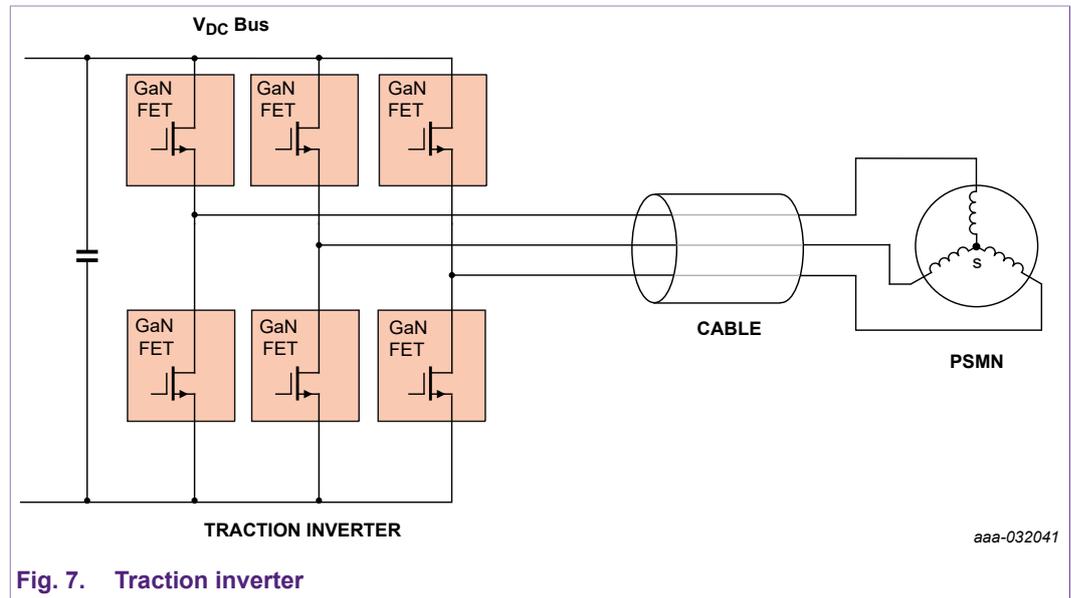


Fig. 7. Traction inverter

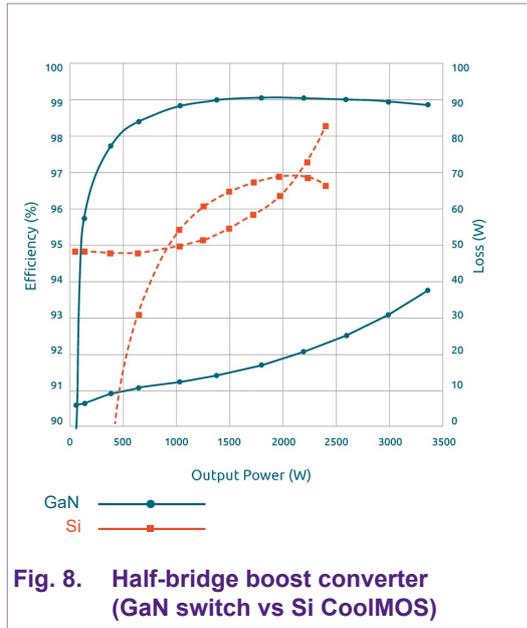


Fig. 8. Half-bridge boost converter (GaN switch vs Si CoolMOS)

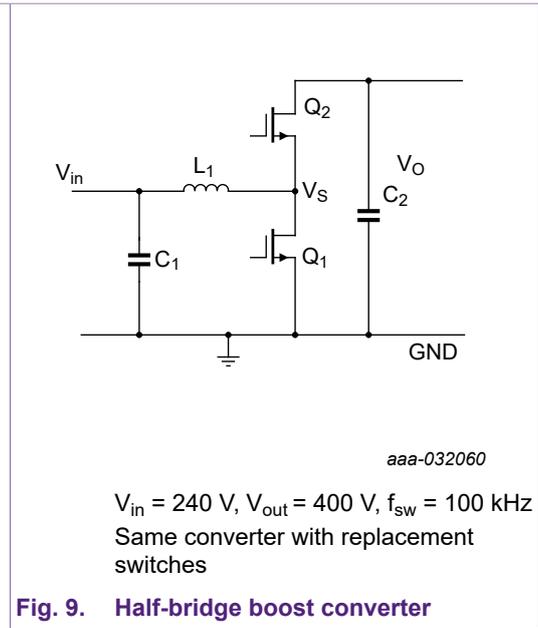


Fig. 9. Half-bridge boost converter

GaN FET losses are significantly lower due to the absence of reverse recovery losses and switching crossover losses. It is possible to achieve near ideal turn on and off losses with dV/dt of approximately 200 V/ns.

GaN switches are extremely fast and routinely used in radio-frequency amplifiers at gigahertz frequencies, although at much lower voltages but show the capability as both use the GaN HEMT structure. Since the GaN devices are very fast and can be used in applications with high dV/dt and high dI/dt , care must be taken to optimize the PCB layouts. To minimize parasitic inductance layout optimization is absolutely fundamental to Power GaN usage.

To maximize the performance of surface-mount packages that have very low inductance, high-current capability, then high-performance modules are essential and are being developed.

Using GaN FETs in a traction inverter requires the GaN FETs to be slowed down substantially to ensure that the dV/dt does not damage the motor winding insulation.

Existing low price motor technology requires that the dV/dt is limited to around 10 V/ns, which provides significant potential to improve the motor design and construction to enable an increase in operating frequency up to >40 kHz leading to improved power density and efficiency.

5. Quality and reliability:

Power GaN FET technology currently showing good quality and reliability as multiple vendors demonstrated Joint Electron Device Engineering Council (JEDEC) and Automotive Electronics Council (AEC) Q101 quality standards. To demonstrate the reliability of power GaN technology, these are minimums and must be fulfilled. For GaN, only the existing quality standards are not enough as the material is new and operates differently. Dynamic R_{DSon} or current collapse phenomena is well known for power GaN FETs and this method for testing is introduced and devices are verified. Material quality, trapping and appropriate de-trapping that is responsible for the dynamic R_{DSon} can be measured and given high-level confidence for its usage as the values getting better and are now around 10%. We need to continuously look at the different failure modes and take the devices to failure and understand the physics of failure.

Beyond AEC-Q101 qualifications, for validating the GaN FETs' reliability in actual operating conditions, several identical half-bridge circuits (with continuous current conduction mode) were prepared using one high and one low side GAN063-650WSA. These were operated continuously for 1000 hours as synchronous-boost converters with the conditions: $V_{in} = 200\text{ V}$, $V_{out} = 480\text{ V}$, $P_{out} = 800\text{ W}$, $T_j = 175\text{ °C}$ and frequency = 300 KHz. There is no indication of any degradation in the performance of any circuits for all samples for the whole duration of 1000 hours of test. Following the high temperature switching tests, all devices were tested for shifts in dynamic R_{DSon} , leakage current, and threshold voltage. All parameters were found to be stable, with any parametric shifts below the allowed levels.

Power GaN technology: the need for efficient power conversion

The device specification has 800 V transient voltage capability guaranteed by test to eliminate any concerns for over voltage spikes. Similarly many other over stresses like voltage and temperatures are used and different acceleration factors are defined for end of life and Failure in Time (FIT) rates estimated for the application situations. As the volume of products shipped increases, real field failure rates will be determined.

Power GaN technology is ready to take its place for efficient power conversion. We are beginning to see its adoption in the non-auto segments and soon it will be used in automotive applications which can take advantage of lower losses and higher power densities. Si technology is well established in the market but reaching its limit. Power GaN technology will be the norm in the future as fear of unknown is reduced going forward.

6. References and further reading:

[1] [AN90005](#) - Understanding Power GaN FET data sheet parameters

[2] [AN90006](#) - Circuit design and PCB layout recommendations for GaN FET half-bridges

7. Revision history

Table 2. Revision history

Revision number	Date	Description
2.0	2020-08-14	Fig. 3 corrected, minor editorial changes.
1.0	2020-07-28	Initial version

8. Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

List of Tables

Table 1. Material properties..... 3
Table 2. Revision history.....8

List of Figures

Fig. 1. GaN HEMT cross section.....	4
Fig. 2. GaN HEMT graphic symbol.....	4
Fig. 3. Q_{rr} , reverse recovery charges for GaN FET vs Si MOSFET.....	4
Fig. 4. GaN FET operation.....	5
Fig. 5. Cascode GaN HEMFET forward and reverse output characteristics.....	5
Fig. 6. AC-to-DC PFC stage and isolated DC-DC configuration.....	6
Fig. 7. Traction inverter.....	6
Fig. 8. Half-bridge boost converter (GaN switch vs Si CoolMOS).....	7
Fig. 9. Half-bridge boost converter.....	7

Contents

1. Introduction.....	2
2. Power GaN FET switches.....	3
3. Scalability and growth.....	5
4. Applications and performance.....	6
5. Quality and reliability:.....	7
6. References and further reading:.....	8
7. Revision history.....	8
8. Legal information.....	9

© Nexperia B.V. 2020. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 14 August 2020
