Avnet Zynq Mini-ITX Development Board
IBERT Design

Version 1.0
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1 Introduction

This document describes an IBERT design implemented and tested on the Avnet Zynq Mini-ITX development board.

2 Reference Design Requirements

This reference design will require the following software and hardware setups.

2.1 Software

The software requirements for this reference design are:
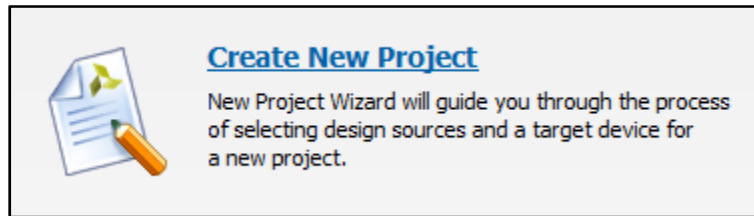- Xilinx Vivado 2013.4

2.2 Hardware

The hardware setup for this reference design is:
- Computer with 4 GB RAM and 1 GB virtual memory (recommended)
- Avnet Zynq Mini-ITX Development Board
- Power supply Module
- ATX power supply
- SFP module supporting up to 6.0Gbps data rate and optical cables or SFP loopback adapter
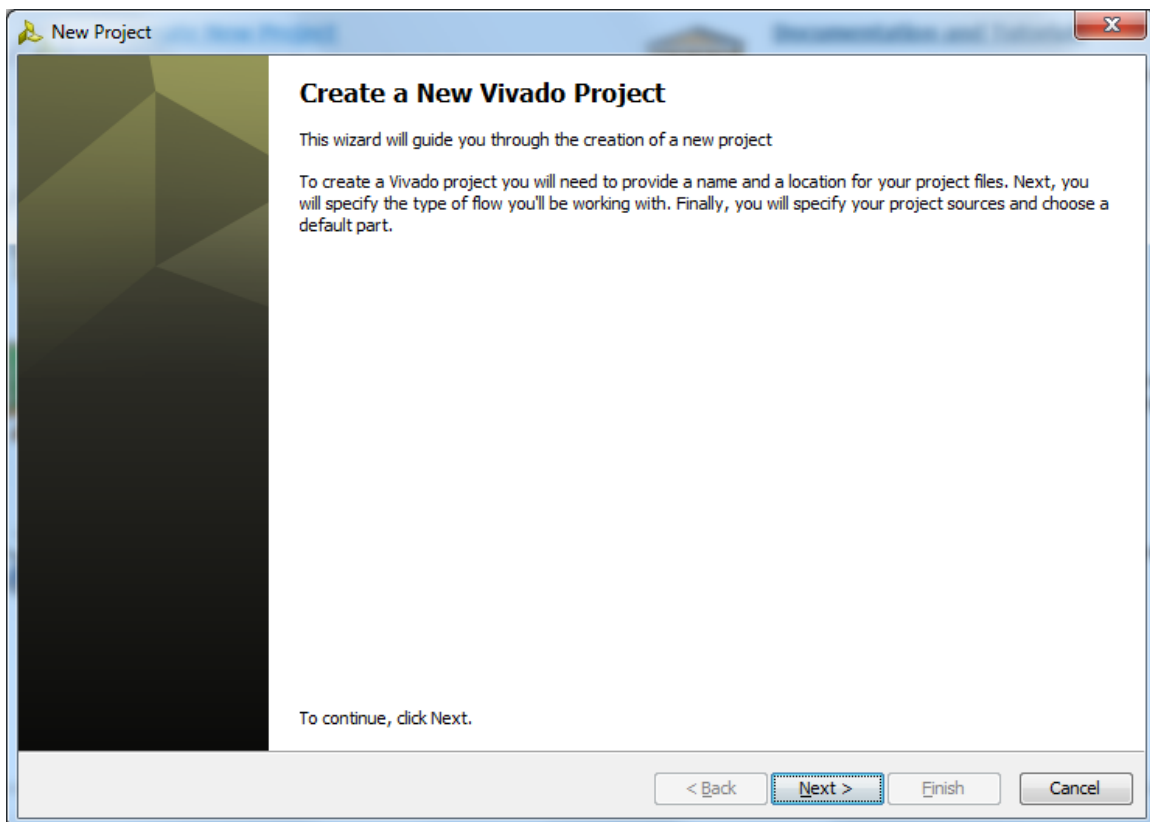- USB A-mini-B cable

3 Using the Xilinx Coregen Integrated Bit Error Ratio Tester (IBERT)

This reference design is developed to assist the users in using the Xilinx Vivado Coregen IBERT to test the Zynq-7000 GTX transceivers. The Coregen IBERT outputs a reference design that can be used to verify the operation of the GTX connected to the SFP module and the SMA connectors on the Avnet Zynq Mini-ITX development board.

1. Start Vivado 2013.4 via **Start > All Programs > Xilinx Design Tools > Vivado 2013.4 > Tools > Vivado 2013.4**.

2. Click on the **Create New Project** as shown in the following figure.
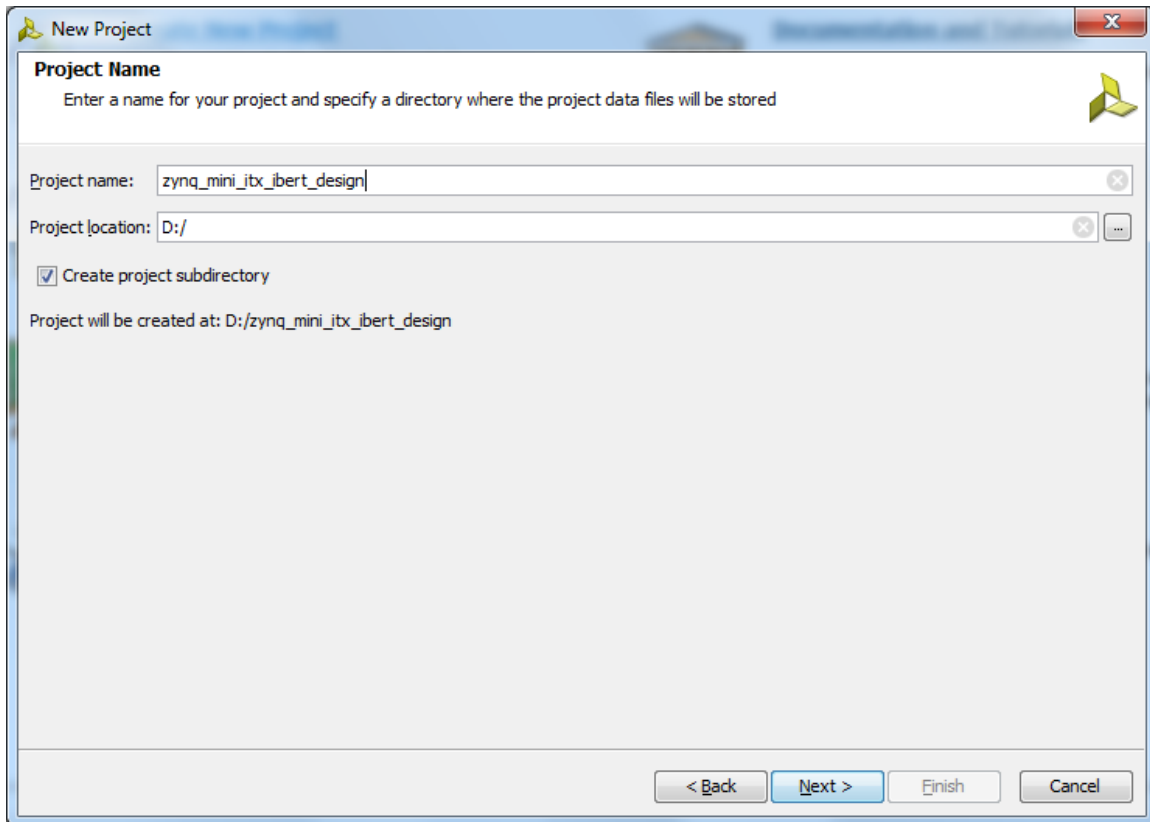

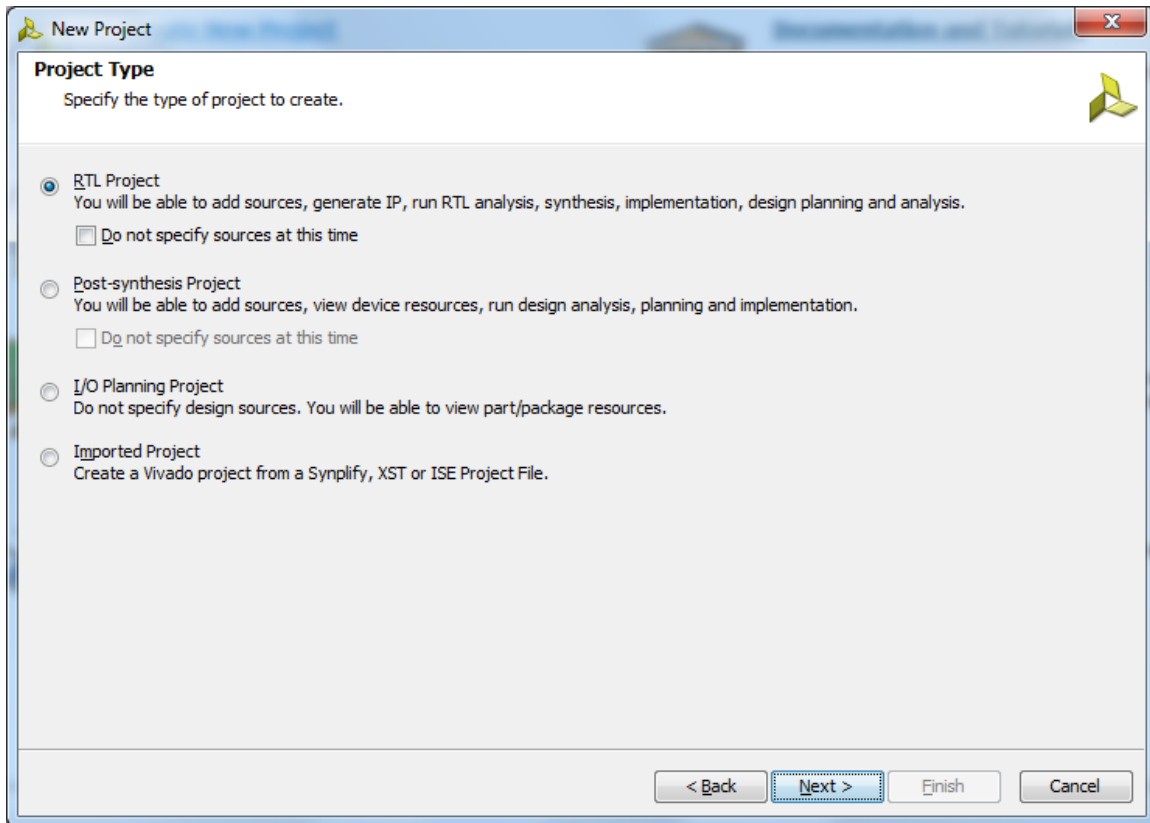3. In the following figure, click **Next** to continue.

4. Specify **zynq_mini_itx_ibert_design** as project name and make sure the **Create project subdirectory** box is checked as shown in the following figure. Click **Next** to continue

   Note: Project can be stored on any hard drive such as the D drive in this example, but keep your path as short as possible.

5. Specify the project type as shown in the following figure and click **Next** to continue.

6. Click **Next** in the next 3 dialog boxes to continue.

7. If you are using the Zynq Mini-ITX board XC7Z045 version, please set the device information as shown in the following figure, click on the **xc7z045ffg900-2** device to highlight it, and click **Next** to continue.

8. If you are using the Zynq Mini-ITX board XC7Z100 version, please set the device information as shown in the following figure, click on the **xc7z100ffg900-2** device to highlight it, and click **Next** to continue.

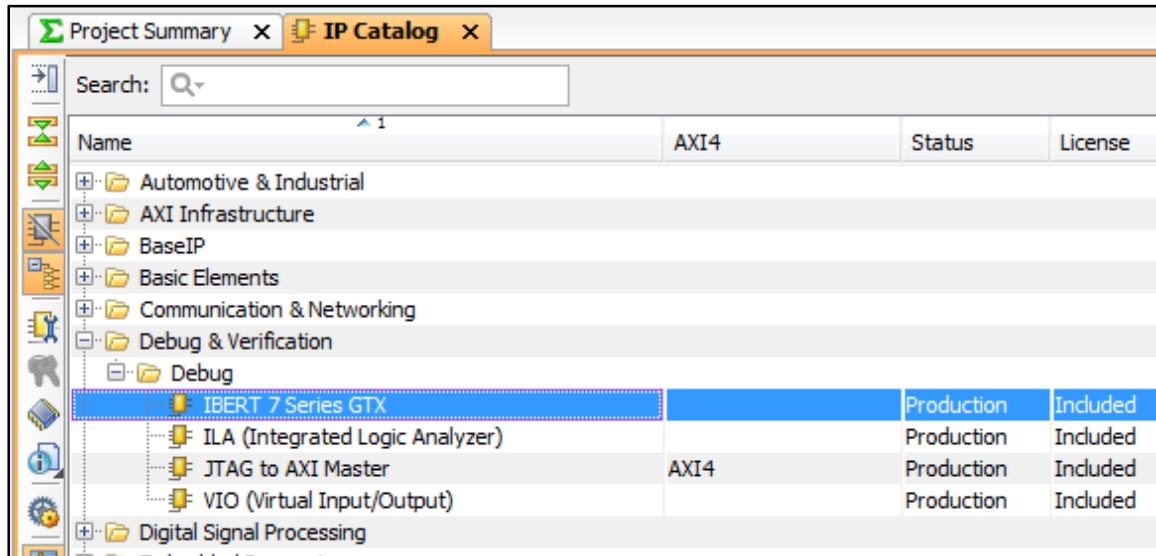| Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
xc7z045ffg900-2	900	362	218600	437200	545	900	16	0
xc7z100ffg900-2	900	362	277400	554800	755	2020	16	0

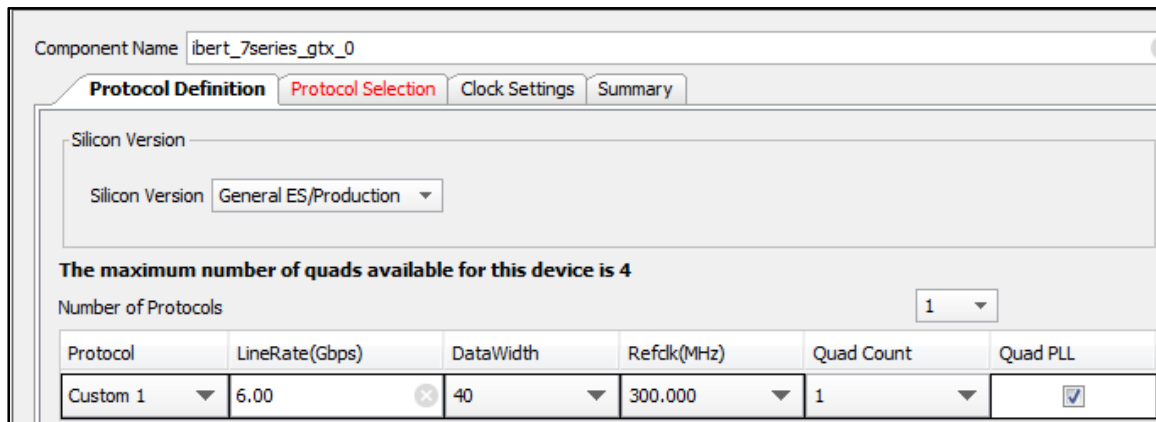9. In the following figure, click **Finish** to continue.

10. Click on the **IP Catalog** in the Vivado GUI as shown in the following figure. The **IP Catalog** will open.
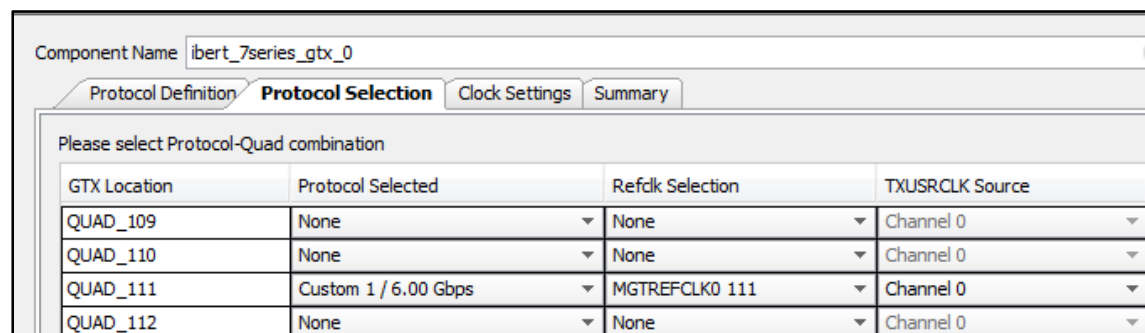
11. In the **IP Catalog** view, double-click on the **IBERT 7 Series GTX** as shown in the following figure.

12. Under the **Protocol Definition** tab, set the parameters as shown in the following figure.

13. Under the **Protocol Selection** tab, set the parameters as shown in the following figure.

14. Under the **Clock Settings** tab, set the parameters as shown in the following figure.

15. Click on the **Summary** to see the project settings as shown in the following figure and click **OK** to continue.

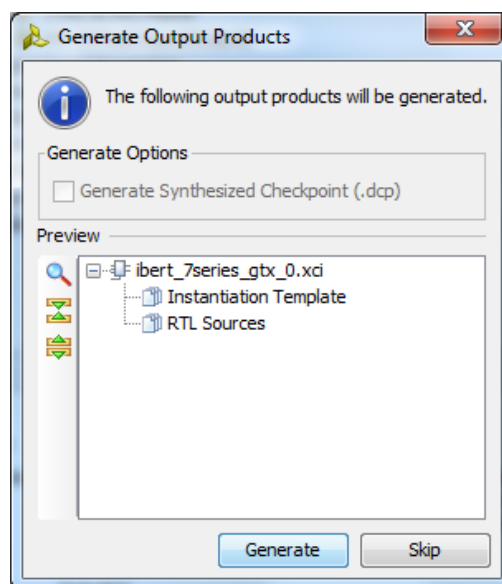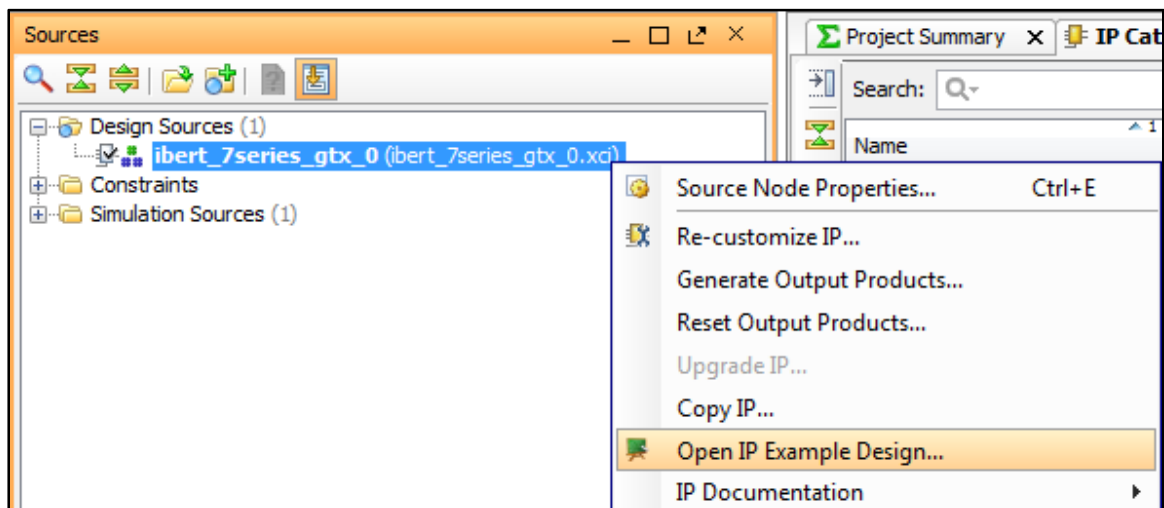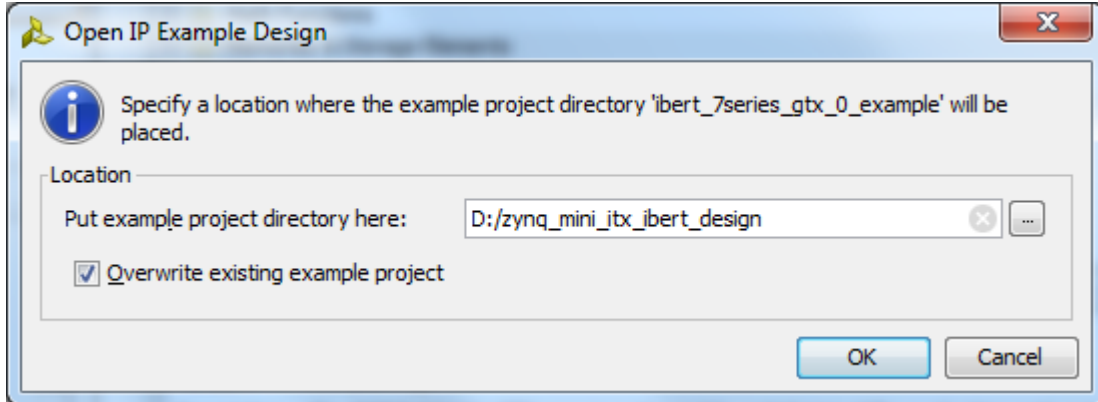16. When the following dialog box appears, click **Generate** to continue.

17. At this time, the **Sources** window should look as shown in the following figure.
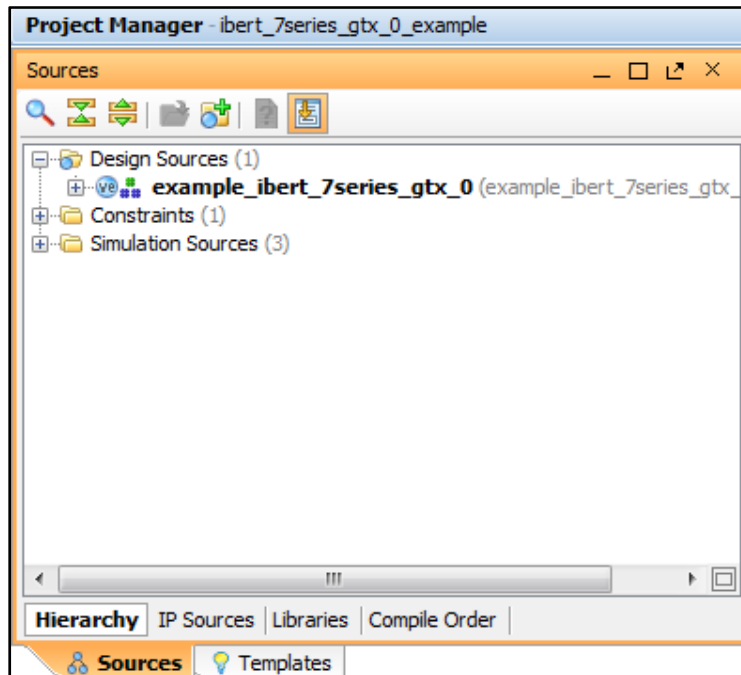

18. Right-click on the **ibert_7series_gtx_0.xci** and select **Open IP Example Design** as shown in the following figure. This action will start a new Vivado project to implement an IBERT example design using the IBERT core generated in the previous Vivado project.

19. When the following dialog box appears, click **OK** to continue.

20. The IBERT example project will open in a new session of the Vivado tool and you should see the following in the **Sources** window of the IBERT example design.
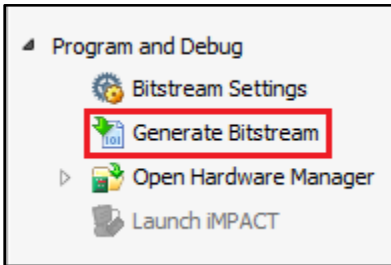

Note 1: The IBERT example design Vivado project is saved in the **zynq_mini_itx_ibert_design\ibert_7series_gtx_0_example** folder in case you need to reopen the project.
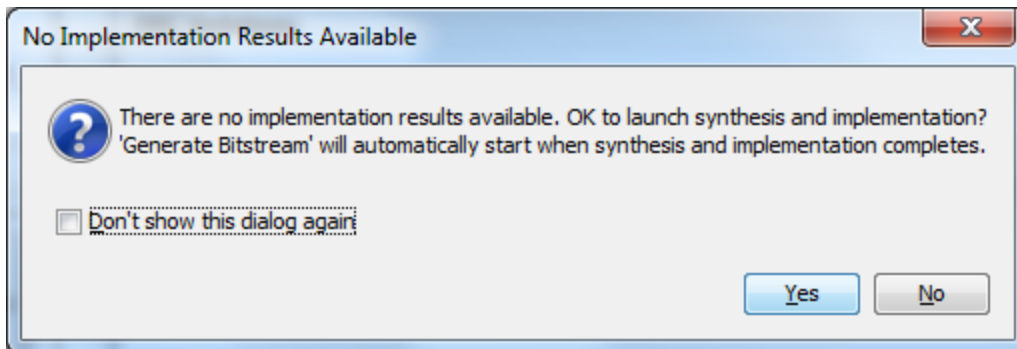
Note 2: If you are using a Windows PC and encounter Windows 260 character path limit issue when trying to rebuild the hardware platform in Vivado (the hardware platform is already built for you), please refer to the Xilinx Answer Record #52787 to resolve the issue.
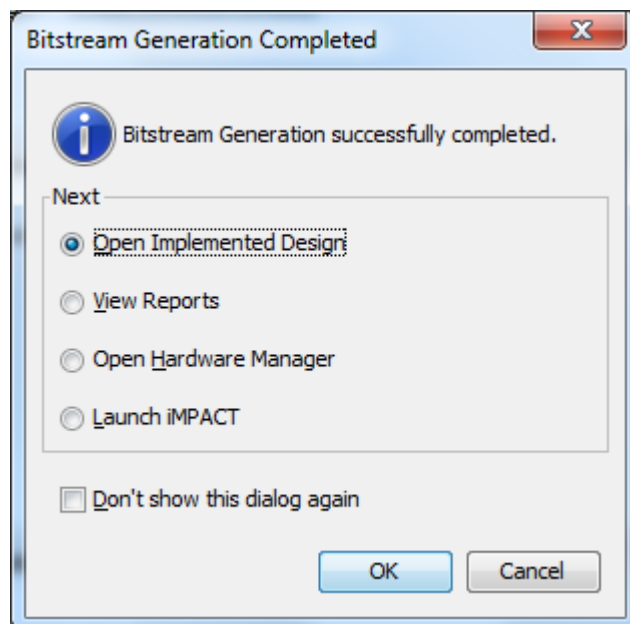
http://www.xilinx.com/support/answers/52787.htm

21. Click on **Generate Bitstream** to implement the design and generate a bitstream.

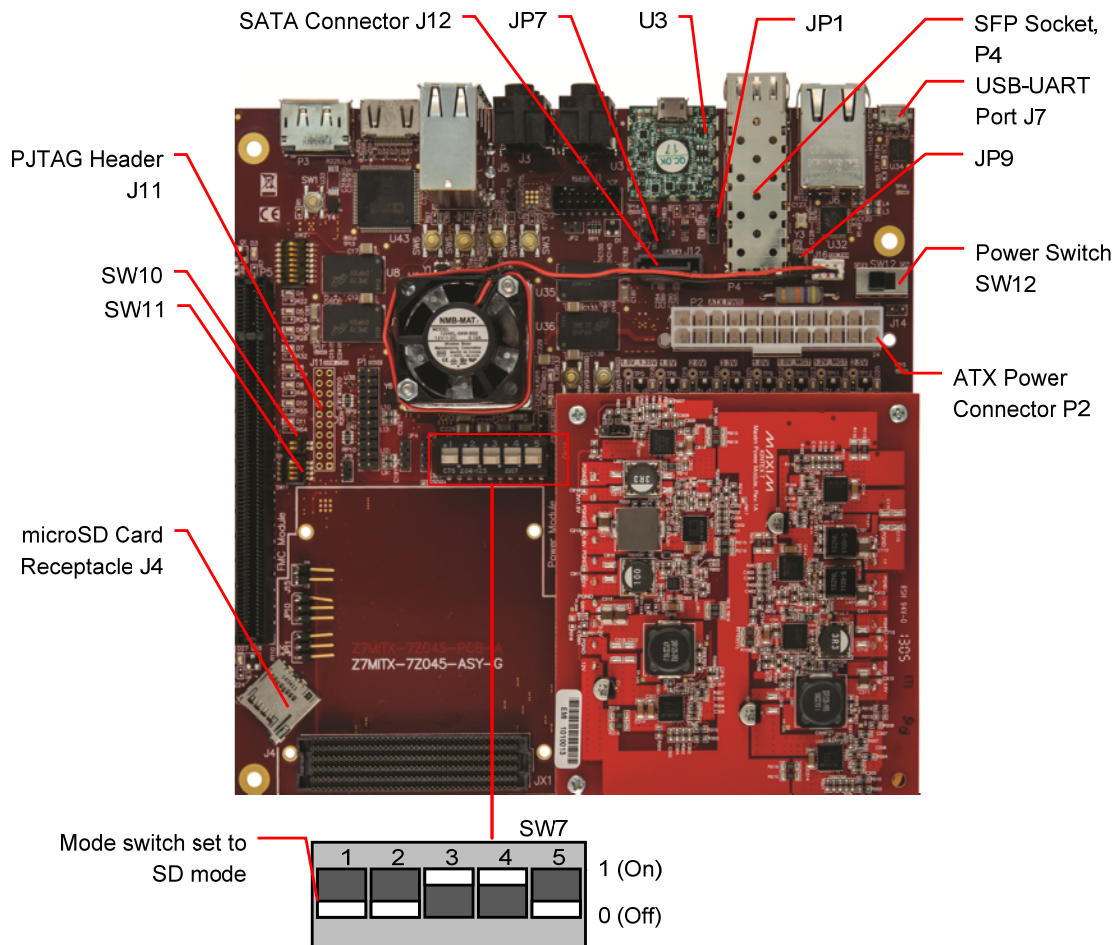22. When the following dialog box appears, click **Yes** to continue.

23. At the completion of the bitstream generation, when the following dialog box appears, click **Cancel** to continue.
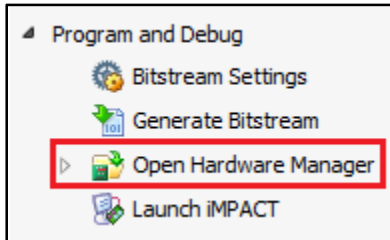
4 Setting up the Board

Please perform the following steps to setup the Zynq Mini Module Plus kit.

1. Install a jumper on JP1 pins 1-2.
2. Install a jumper on JP7 pins 3-4.
3. Install a jumper on JP9.
4. If not already installed, install the power module onto the Mini-ITX board via J8, J9, and J10 connectors.
5. Connect the ATX power supply to P2 connector.
6. Connect the USB A-min-B cable to the U3 (Digilent USB-JTAG SMT-2 module) USB port and the USB port of the PC (JTAG connection).
7. Set the boot mode switch (SW7, positions 1-5) to 00000.
8. Plug an SFP module into the SFP socket (P4) on the baseboard and use an optical cable to connect the SFP TX port to the SFP RX port or insert an SFP loopback plug into the SFP socket.
9. Set the SW11 DIP switch (positions 1-4) to OFF, ON, ON, and OFF.
10. Set the SW10 DIP switch (positions 1-2) to ON, and ON.
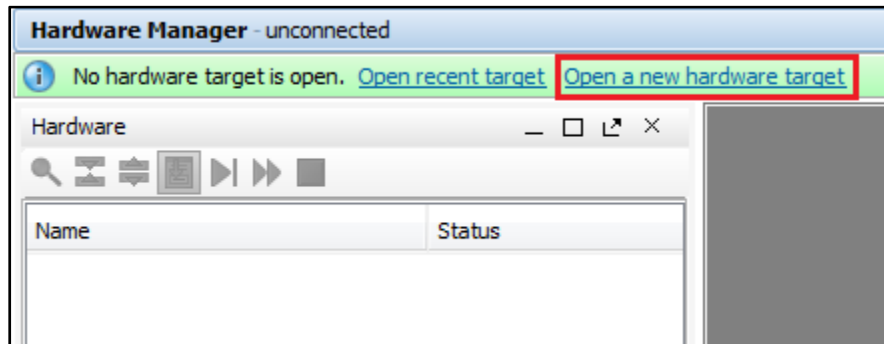11. Slide the SW12 power switch to the ON position.

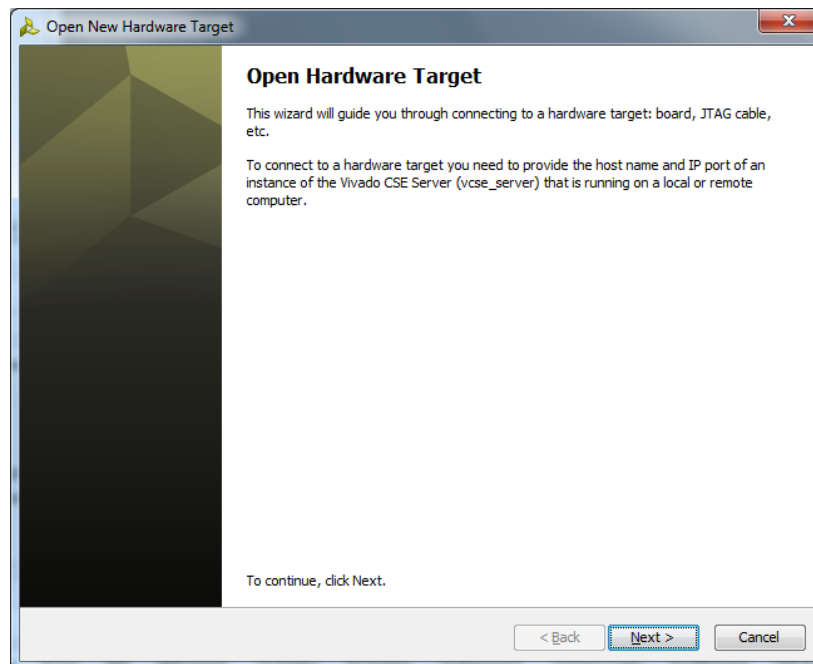## 5 Running the IBERT Design on the Mini-ITX Development Board

1. Upon successful completion of the bitstream generation, click on the **Open Hardware Manager** in the Vivado GUI as shown in the following figure.
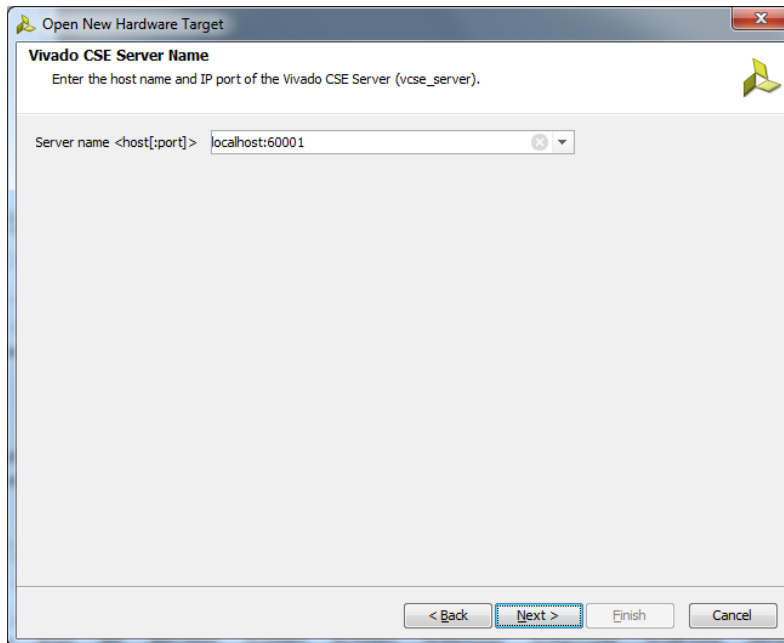

2. Click on the **Open a new hardware target** in the Vivado GUI as shown in the following figure.
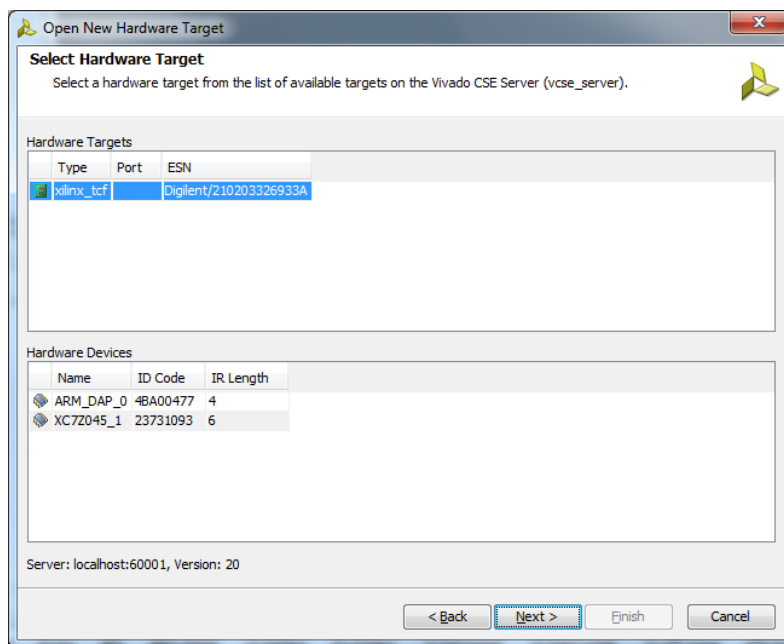

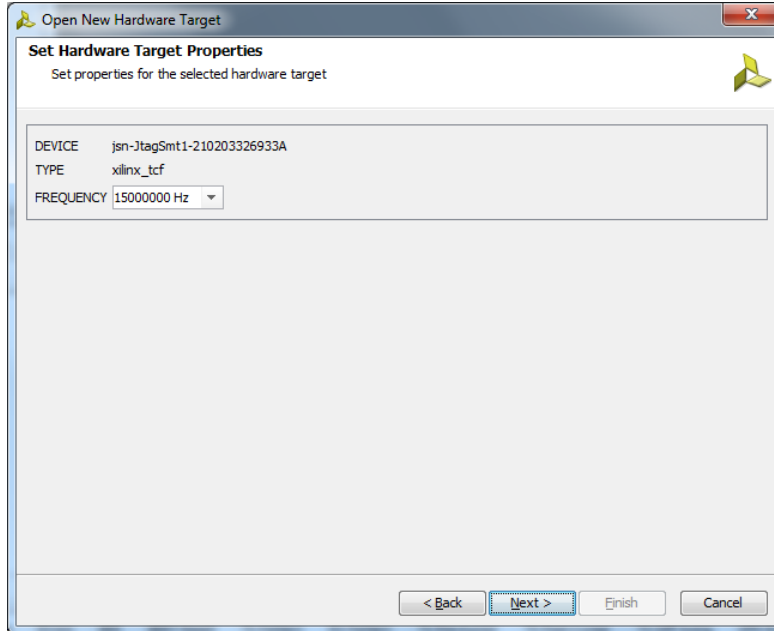3. Click **Next** to continue.
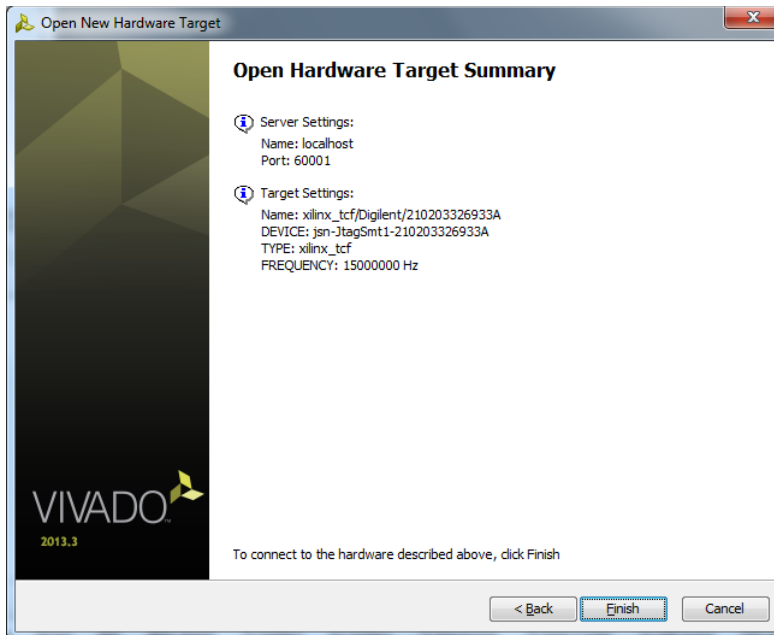
4. Click **Next** to continue.
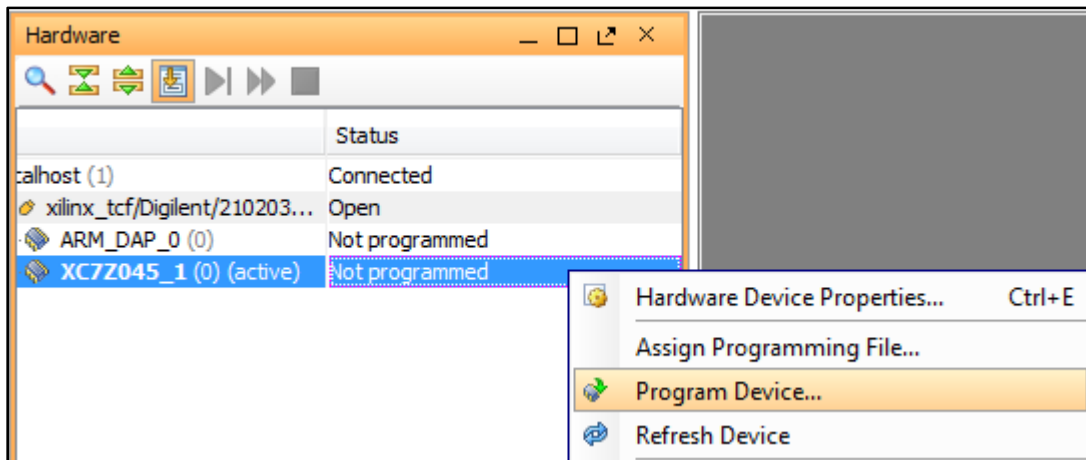

5. Click **Next** to continue.
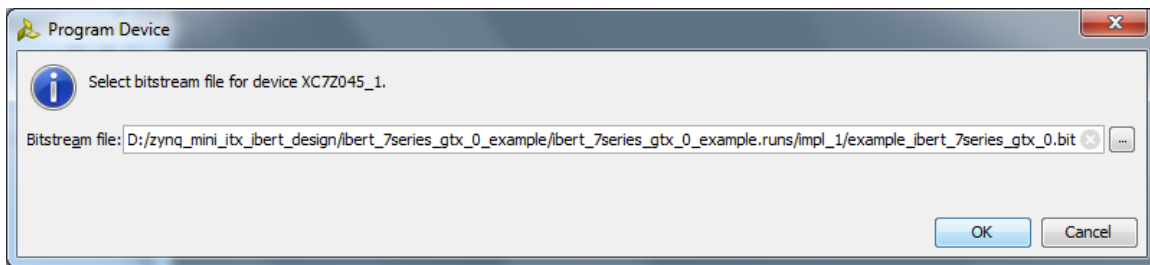
6. Click Next to continue.
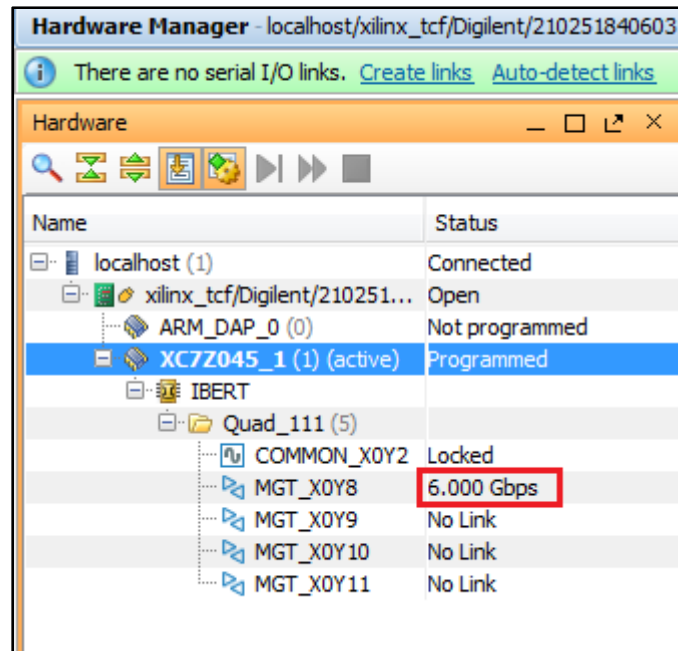

7. Click **Finish** to continue.

8. Right-click on the **XC7Z045_1** device and select **Program Device** as shown in the following figure (you would right click on the **XC7Z100_1** when using the Zynq Mini-ITX 7Z100 version.
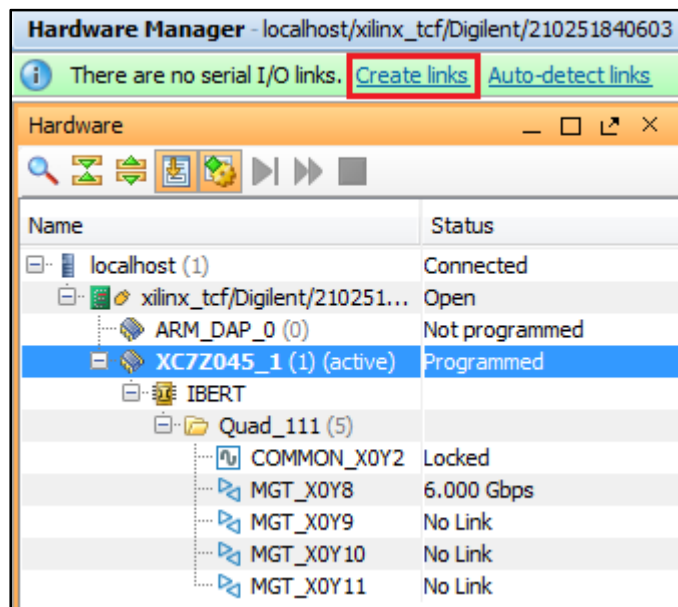

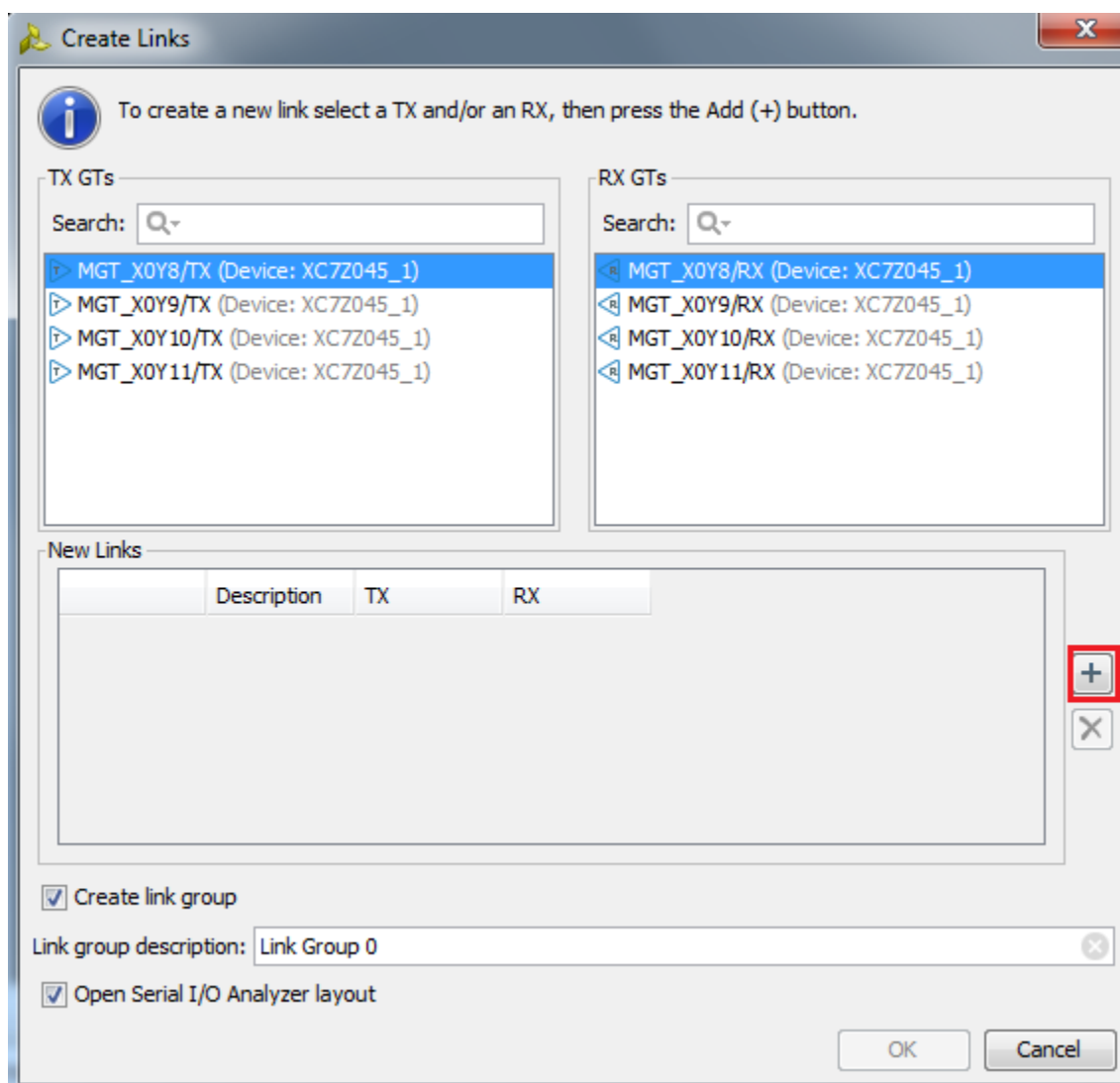9. When the following dialog box appears, click **OK** to continue.

10. The Vivado GUI should look as shown in the following figure. The MGT_X0Y8 is connected to the SFP socket on the Mini-ITX board. The MGT_X0Y9, MGT_X0Y10, and MGT_X0Y11 in the GTX Quad 111 are not used in this IBERT example design.
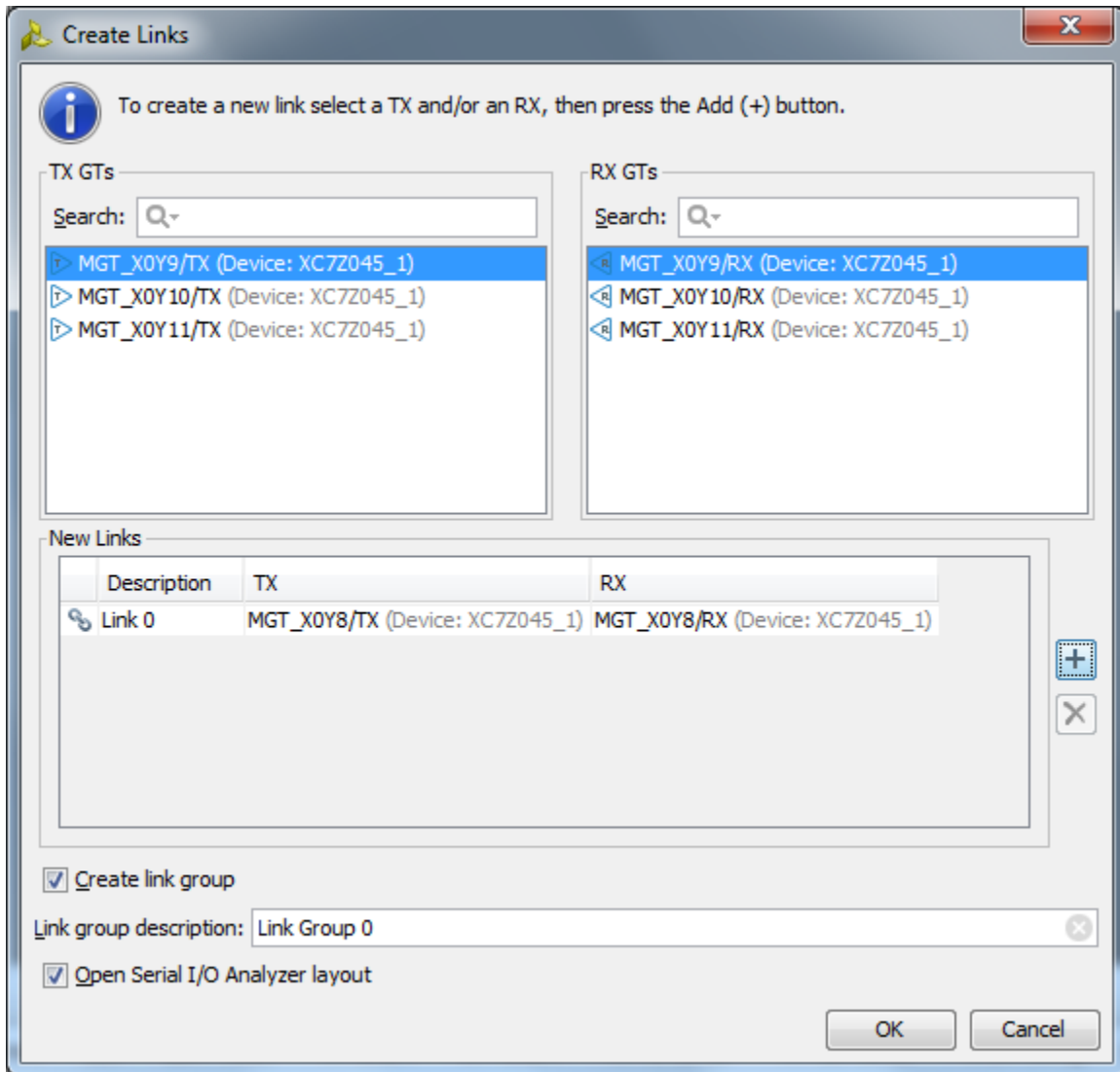

11. Click on **Create Links** as shown in the following figure.

12. Click on MGT_X0Y8/TX and MGT_X0Y8/RX to highlight them and then click on the + sign to add the MGT_X0Y8 to the new link set as shown in the following figure.

13. The **Create Links** dialog box should look as shown in the following figure.

14. You should see the following in the Vivado GUI. As seen, link0 and link1 are running at 6.0Gbps without any errors using PRBS 7-bit data pattern.

15. Set the **TX Pattern** and **RX Pattern** to **PRBS 31-bit** using the drop-down box to stress the links and then click on the **BERT Reset** to reset the Error counter as shown in the following figure.