SiC Simulations

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Abstract

*Last year's session explained how **onsemi**'s Physical and Scalable Spice simulation models are made and used to obtain datasheet values. In this session, we will focus more on results obtained only through simulation and how to use the results in some high−power conversion topologies.*

The first part of the session will explain to you:

- *How to access internal node voltages or the die voltages.*
- *How to use corner simulation models to study current sharing between MOSFETs in parallel.*
- *How to use the thermal interface with a Cauer network.*
- *How package parasitics can influence switching losses.*
- *How the half−bridge structure can also influence losses.*

The session second part will focus on topology simulations like:

- *Flying Capacitor Boost*
- *I−NPC and T−NPC cells*
- *6−Pack Boost Active Front End with complete D−Q control and 3rd Harmonic Injection*

Introduction

In the past, behaviors and models with elementary structures were the foundation of simulation. Equations used by those models are the ones we all learn at school, and they are primarily valid for devices used in simple integrated circuit technologies.

But, when it comes to power devices, those simple models usually cannot predict phenomena linked to the changes done to optimize the device. Today, most of the power device structures are not lateral but vertical. They use several doping layers to handle the large electric field. Gates move from Planar to Trench. More complex structures, like super junctions, have been introduced and dramatically changed MOSFET behaviors. Simple device structures available in basic spice models do not consider all those non−linearities.

Now, by introducing the Physical and Scalable modeling technique, **onsemi** moves simulation to the next level of accuracy.

Victory et al. have explained this modeling technique [1, 2, 3, 4, 5, 6] based on physical equations, process parameters, and layout parameters. It also considers all non−linearities introduced in our parts for modern power switching devices. Physical equations can capture temperature dependency and propagation effects in all various zones of modern power devices. We create a core model for dedicated technology (SiC MOSFET M3, IGBT FS4, etc.) — setting the dimension of the die through the layout parameters to obtain a particular device.

During last year's webinar session [8, 9, 10], we showed you how easy it was to get datasheet values with those new models. It is also clear that Physical & Scalable simulation models contain much more than datasheet values obtained with datasheet parameters or obtained in an almost ideal measurement environment. The models can simulate all values in all conditions within the specification limits. Parameters or curves not available in the datasheet are also captured in the Physical and Scalable simulation models — accessible through simulation. Most of the time, just running a straightforward simulation schematic is needed.

As an example of the power of Physical and Scalable models, let's compare output capacitor results obtained by simulating two super−junction MOSFET models (one behavioral and one Physical & Scalable). Those two super−junction MOSFETs have similar performances (650 V, around 18 mΩ on−resistance). First, we will superpose results with the measured data. For the simulation configuration details, please refer to [7] for the simulator library setup and [8, 9, 10] for the simulation schematic and simulation setup.

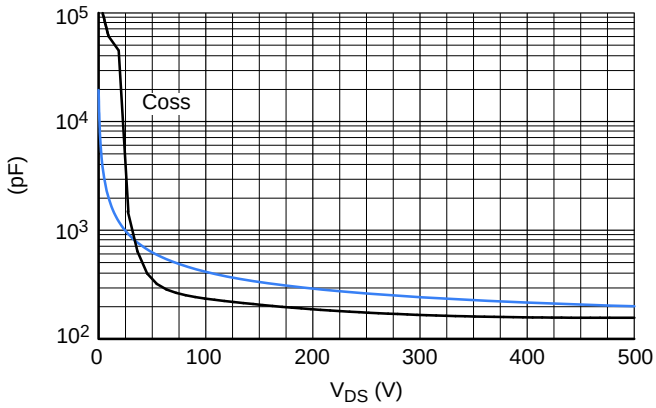

Figure 1. Behavioral Model Output Capacitor Simulation Results

In the previous and following graphs (Figures 1 and 2, respectively), the colored curve is obtained by simulation, while the superimposed black curve is the one given in the device specification. Figure 1 is from a competitor model because all **onsem**i super−junction MOSFET models are not behavioral but Physical & Scalable. The behavioral model cannot capture the nearly 3−decade drop in output capacitance inherent to all Super−Junction MOSFETs.

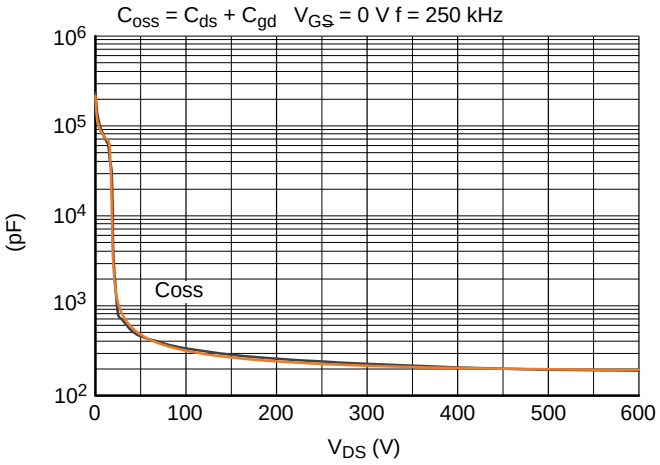

Figure 2. Physical & Scalable Model Output Capacitor Simulation Results

Second, to compare the same Silicon Super Junction MOSFET models used to obtain Figures 1 and 2, we plotted the Output Capacitor (or C_{OSS}) on the same log−log scale this time. This scale amplifies the differences but helps us to read simulation results for the maximum capacitor values at minimum blocking voltage and minimum capacitor values at maximum blocking voltage for both devices, as shown in Figure 3.

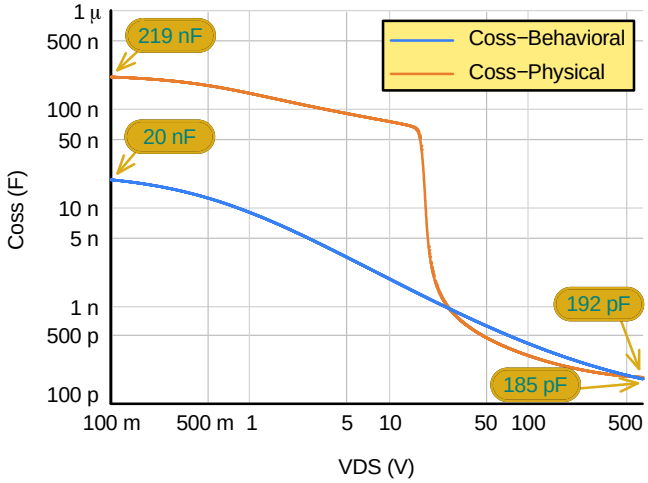

Figure 3. Output Capacitor Simulation Results Comparison Behavioral vs. Physical and Scalable

Let’s imagine we want to simulate a soft transition or zero−volt switching application using a Half− or Full−Bridge structure. During the transition, we will consider the inductor current constant, meaning the inductor is large enough.

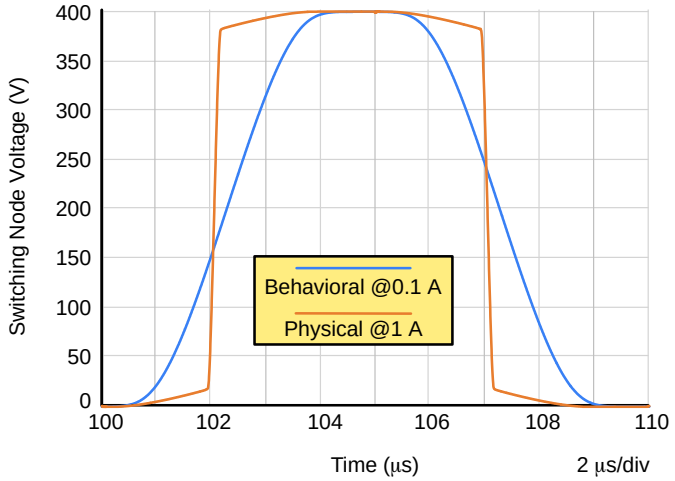

Figure 4. Output Capacitor Simulation Results Comparison Behavioral vs. Physical and Scalable

We tried to get almost the same transition time (Figure 4). Due to the decade difference in capacitor values at low voltage (see Figure 3), the currents needed to charge output capacitors and get a soft transition also have a decade difference in their values.

As shown in Figure 2, the output capacitor value (or C_{OSS}) given by the **onsemi** Physical and Scalable simulation model is accurate and actual. It means the current needed for the soft transition simulated using the **onsemi** Physical and Scalable simulation model in Figure 4 is also valid.

Using the behavioral simulation model, you will underestimate the energy needed for the resonant transition by a factor of 10 — a mistake or error that could require a complete redesign of the application's resonant tank and the system.

Now, you can simulate the Zero Voltage Switching transition with excellent accuracy using **onsemi** Physical and Scalable simulation models. You will get the actual energy needed for the transition because the simulation model captures all capacitor non−linearities over more than 3−decades of C_{OSS} variation.

Physical & Scalable Simulation Model Capabilities

REMARK: the Annex shows simulation−schematic details in a larger format than in the article text.

Access Internal Node Voltages with SIMetrix

The bonding and the package are between the die and the electrical or thermal contact point. The assembly influences the die performance with parasitic series inductance and resistance or electrical impedance and thermal impedance. Package pins plus bonding and metal mask can add up to 10 mΩ series resistance.

To quantify those influences, it is possible to access die internal nodes like Gate, Drain, and Source for a 3−pin MOSFET (See Figure 5).

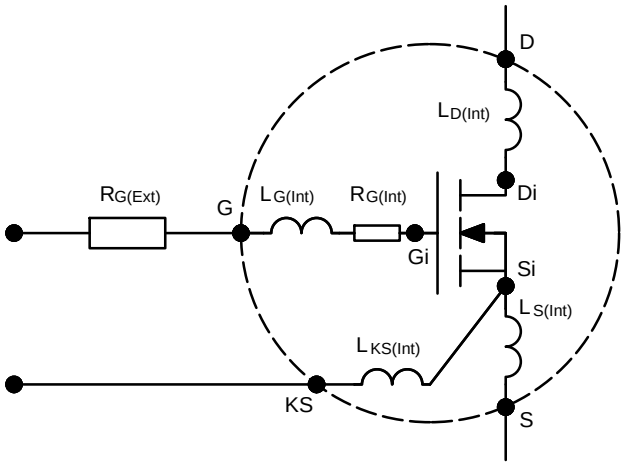

Figure 5. Internal Versus External Nodes

The gate is the most critical signal in hard and soft switching in very high−speed switching. It is essential to know when the MOSFET is really on and off. For example, it helps designers set the delay between high−side and low−side switching in a half−bridge structure.

To access internal nodes, look for the device and the available pin names. A pin is labeled with an ‘i’ for ‘internal’ at the end.

In **SIMetrix** [12], you have internal node voltages available by selecting this feature in the simulation option control panel. Then, names looking like ‘**Q*n*:*xy*:di**’ are, for example, the internal Drain node voltage. It is the voltage directly at the die level. We can now measure the actual Drain−to−Source voltage applies to the die without all parasitic that may increase or decrease the ringing.

Let’s take a half−bridge configuration with SiC MOSFET NTHL015N065SC1, vary the external gate resistor, and compare the Drain−to−Source voltage difference between die level and package level. This device uses a TO247 with three Leads.

In the following figures, we can compare turn−on and turn−off Drain−to−Source waveforms. At turn−on, ringing is lower, while at turn−off, it is the opposite (see Figures 6 and 7).

Light−colored curves are die−Drain to die−Source voltage, while dark−colored curves are package−Drain to package−Source pins voltage.

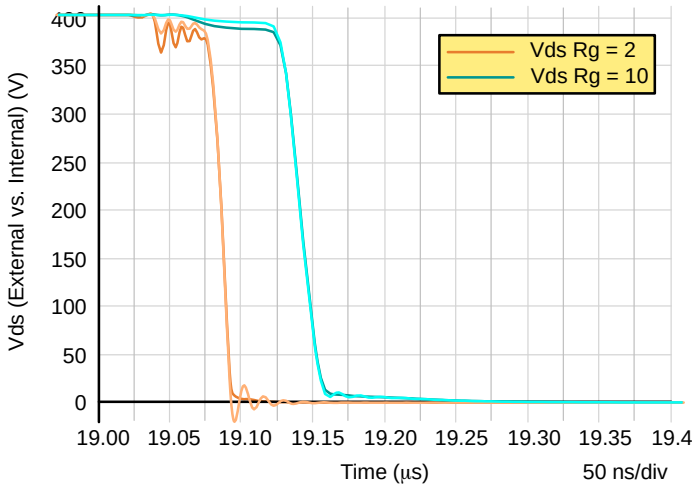

Figure 6. Drain−to−Source Voltage Difference at Turn−On between Internal and External

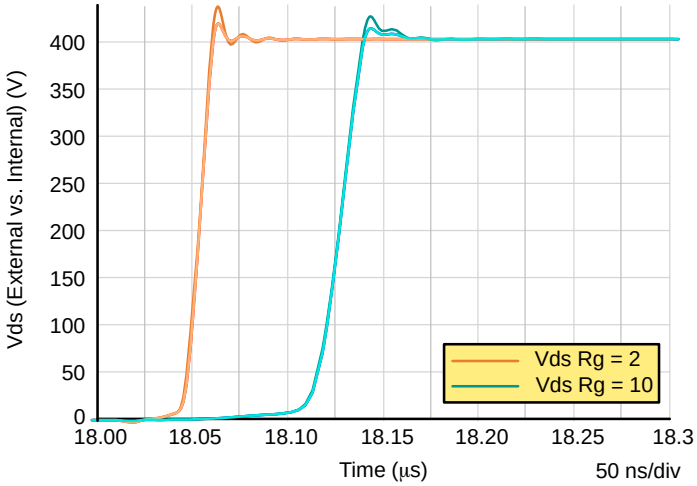

Figure 7. Drain−to−Source Voltage Difference at Turn−Off between Internal and External

As stated earlier, having access to the actual die gate signal gives you handy information. Let's take a half−bridge configuration with SiC MOSFET NTH4L015N065SC1, vary the external gate resistor, and compare the Gate−to−Source voltage difference between die level and package level (see Figures 8 and 9).

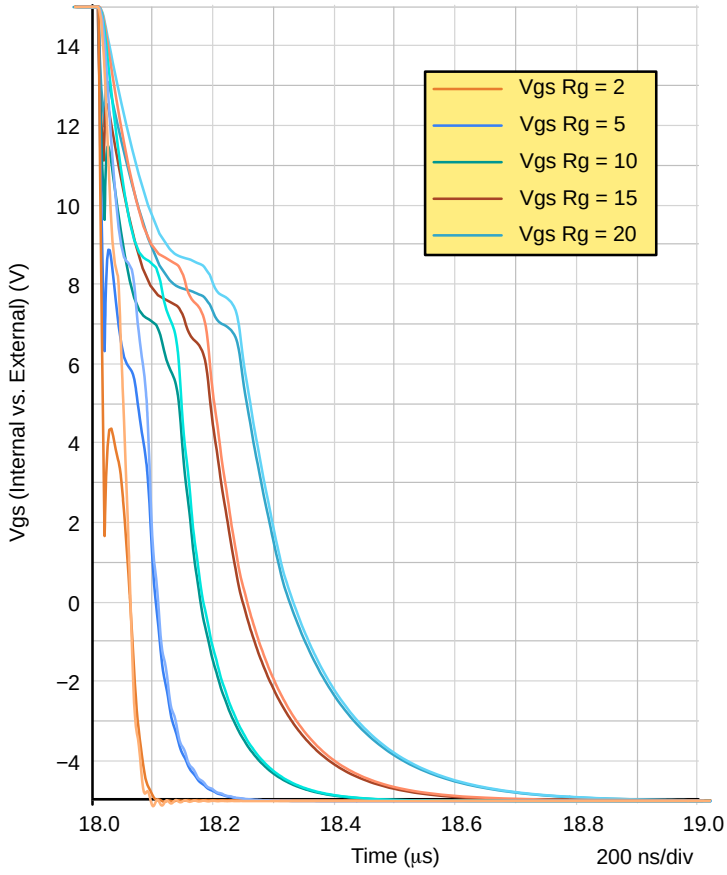

Figure 8. Gate−to−Source Voltage Difference between Internal and External as a Function of the External Gate Resistor

Light−colored curves are die−Gate voltage, while dark−colored curves are package−Gate pin voltage.

Let's see step by step what happens when the gate resistor changes. Above 10 Ω, the external and internal gate voltages cross the threshold (i.e., 2 V with **onsemi** SiC MOSFET) almost simultaneously. There is a delay in the range of 10 ns.

With 5 Ω and below, we can see voltage spikes and more and more oscillations during the turn−off on the external gate voltage only while the internal gate voltage is relatively smooth.

With 5 Ω or 2 Ω, a considerable delay (around 40 ns) is clearly visible at the threshold crossing between the two voltages (external and internal).

For 5 Ω, the turn−off time given by the external voltage is around 80 ns, while the internal turn−off time is approximately 120 ns, so 50% longer. For 2 Ω, it is even worse. The turn−off time given by the external voltage is about 40 ns while the internal turn−off time is 80 ns, so a 100% longer turn−off.

It depends on the ratio between external and internal gate impedances. In the previous example in Figure 8, the internal gate impedance is slightly below 1 Ω.

In Figure 9, we increase the internal gate impedance close to 5 Ω by changing the die design and gate runners, but with the same package, we can see a longer turn−off time in general, as expected. The gate network is also more damped, and less ringing is present on the external gate node voltage.

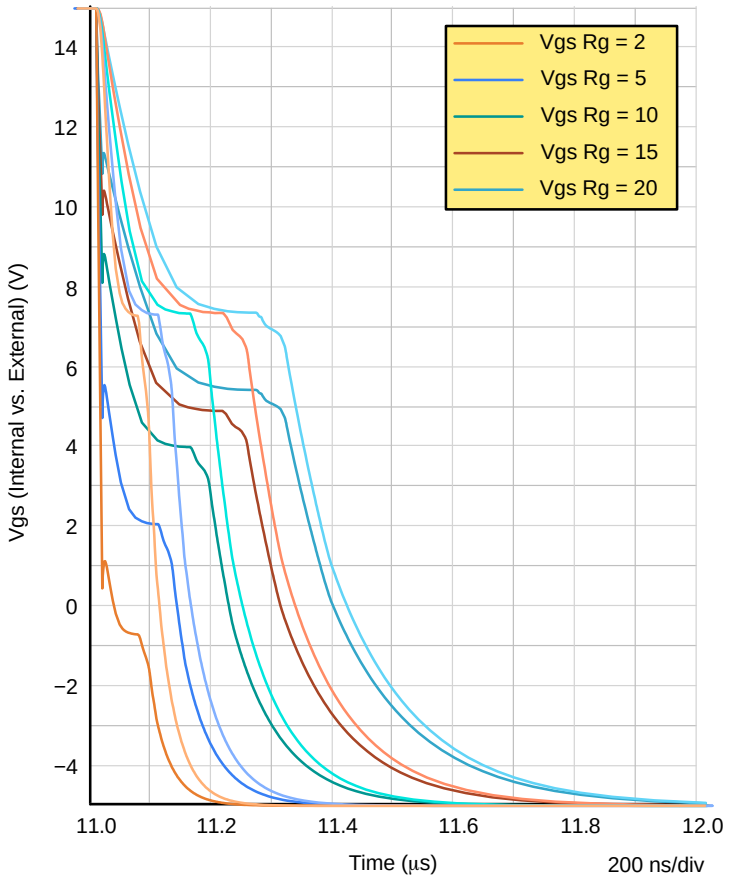

Figure 9. Gate−to−Source Voltage Difference between Internal and External with High Internal Gate Impedance

Figure 9 shows a longer delay between internal and external gate voltages when the external gate resistor is below 10 Ω. Some manufacturers use high internal gate impedance to decrease maximum Drain−to−Source dV/dt, EMI content, and limit failure due to gate oxide stress.

However, it also increases the risk of shoot−through when relying on external gate voltage waveforms to set the delay between switches in a half− or full−bridge configuration.

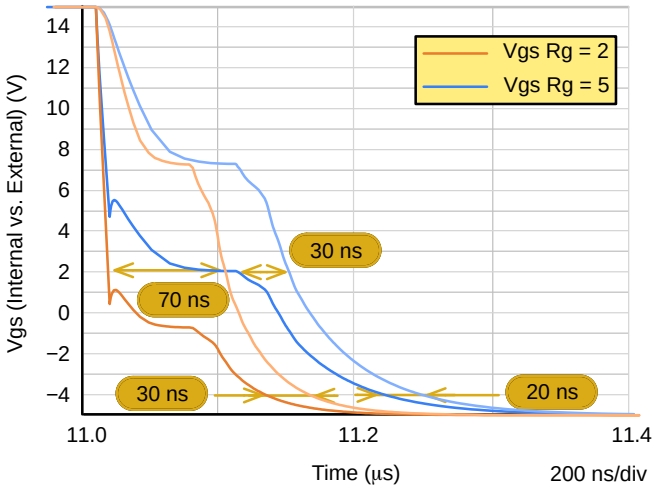

Figure 10. Gate−to−Source Voltages Delays

There is a big difference in the threshold crossing time for external resistors below 10 Ω, as shown in Figure 10. Even the zero crossing and turn−off threshold crossing can happen at a different time than the internal gate and the external gate signal. In the case of a half−bridge configuration where MOSFETs switch out of phase or in Q−$\overline{Q}$ configuration, we can measure a much lower turn−off delay on the external gate than the real turn−off time. And so, turning on the other side MOSFET too early and creating a big shoot−through.

Here also, having access to internal die voltage can be very helpful to set the proper delays to avoid cross−conduction between the High and Low sides.

Using Corner Models

Models available online are made and calibrated using nominal values from the fab. They give typical datasheet values.

But, in practice, parameter values follow a Gaussian distribution due to process variation in manufacturing.

For a particular technology, it is possible to create models with minimum and maximum values. We can then study paralleling when devices are not the same or see device reactions in the function of extreme case values.

To illustrate that capability, let us use a High Voltage Buck stage with three SiC MOSFETs operating in parallel (see Figure 11).

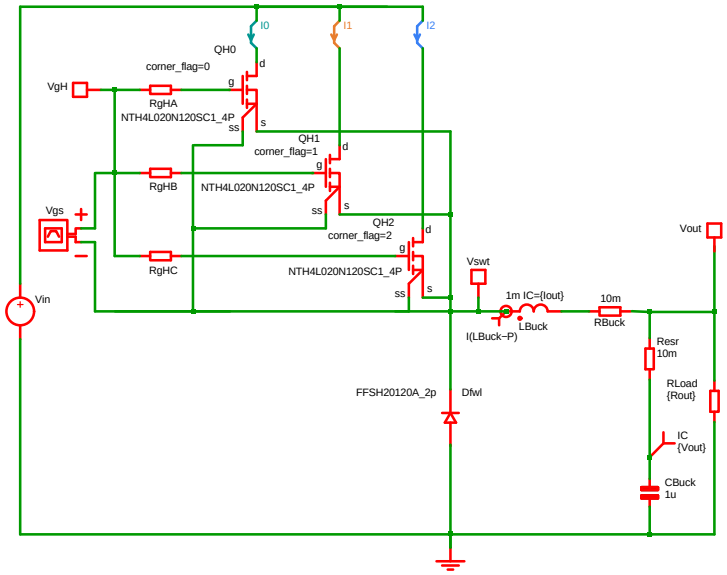

Figure 11. Buck Stage with Corner Models

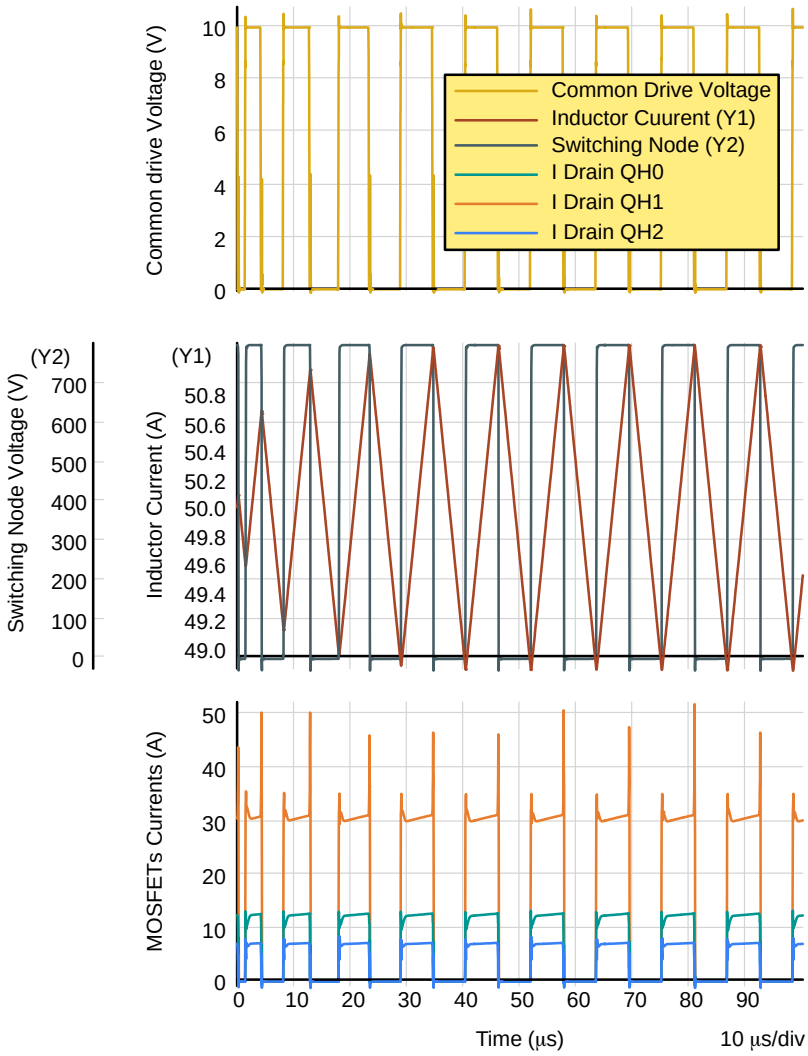

Figure 12. Buck Stage Waveforms with SiC MOSFET Corner Models

The results in Figure 12 show a very unbalanced current flowing in the SiC MOSFETs. The currents split into 30 A, 12 A, and 7 A in switches or SiC MOSFETs during the on−time — for 50 A average steady−state current in the inductor. The theoretical current−value that should flow in each MOSFET is around 17 A, and we have a +13/−10 A error. So, on the current balancing, it makes an error of +76% for QH1 (the lowest threshold MOSFET), an error of −29% for QH0 (the average threshold MOSFET), and an error of −59% for QH2 (the highest threshold MOSFET).

We can now also analyze turn−on and turn−off details with Figures 13 and 14.

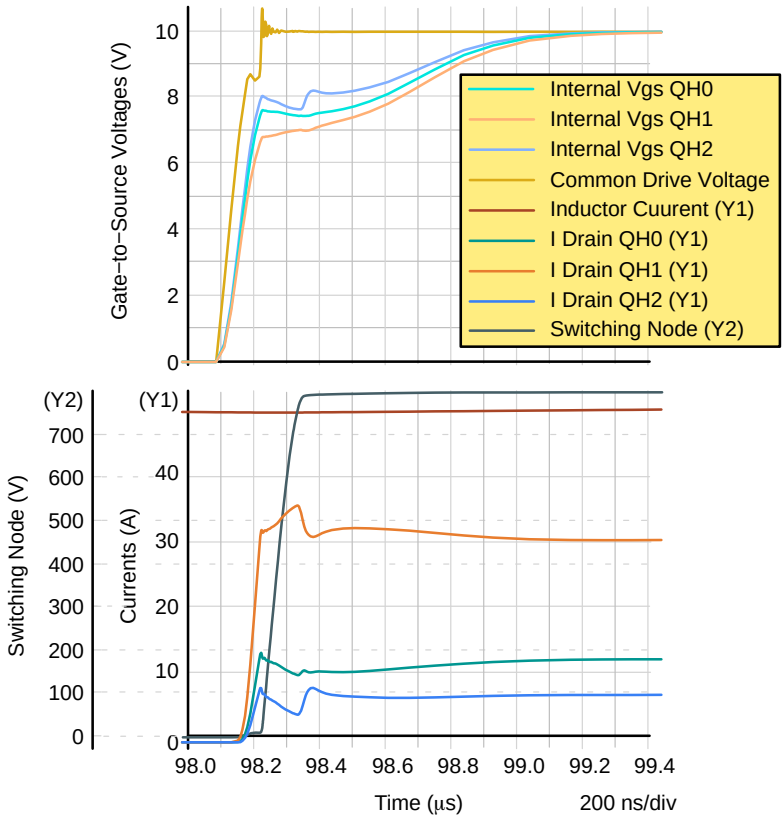

Figure 13. Turn−On Sequence Zoom

At turn−on, shown in Figure 13, a much higher current flows in the SiC MOSFET with the lowest threshold voltage. This single MOSFET sees a large part of the inductor current plus the reverse capacitive SiC Schottky diode current. Also, turn−on losses will not be equal in all SiC MOSFETs.

Similarly, during turn−off, almost all the current flows in the SiC MOSFET that has the lowest threshold voltage (See Figure 14).

We can also see the current starting to decrease first in the SiC MOSFET at the highest threshold voltage and then decreases in the average threshold voltage. But, before a complete turn−off of those two SiC MOSFETs, a resonance in the three−gate network makes those two SiC MOSFETs have a lousy turn−on due to their integral gate−to−Source voltages increasing a little bit. They conduct again but only a small part of the total current during the switching node voltage negative slope.

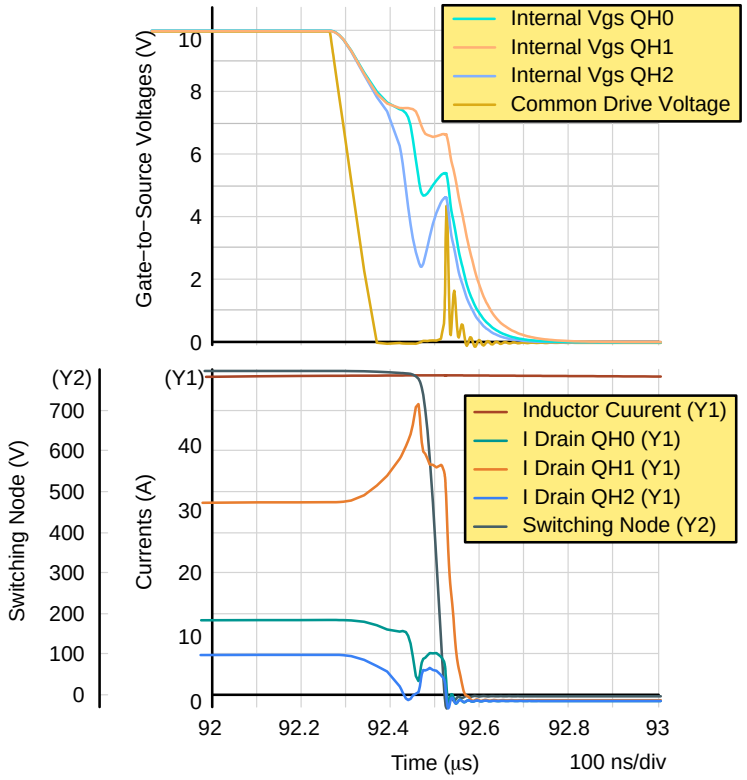

Figure 14. Turn−Off Sequence Zoom

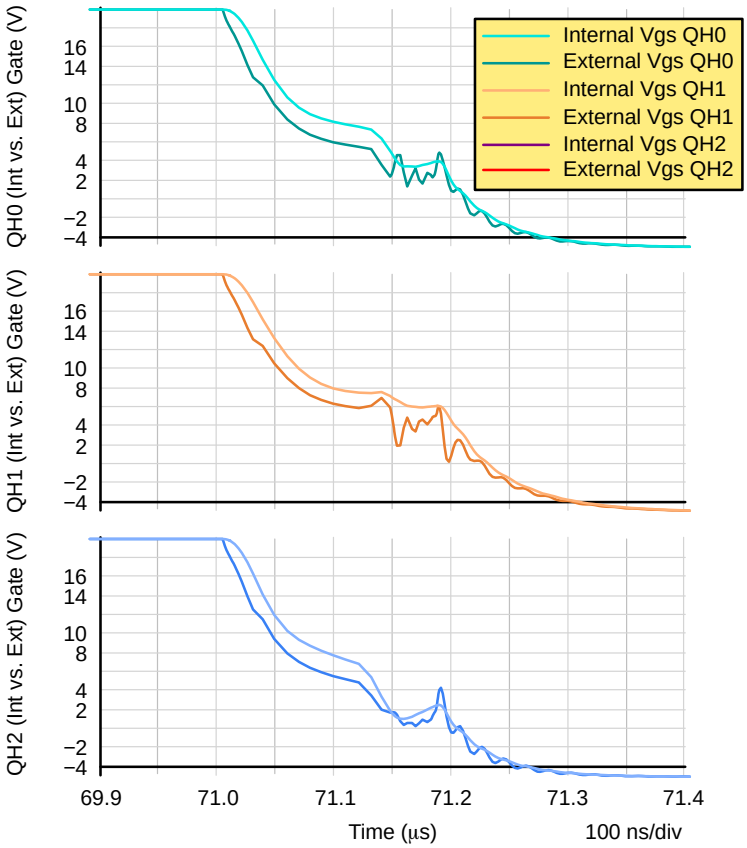

Figure 15. Turn−Off Sequence Zoom Internal vs. External Gate−to−Source Voltage

Here also, if we analyze the difference between the internal and external Gate−to−Source voltage, we obtain the results in Figure 15. We see gate network oscillations in the external Gate−to−Source voltages. There is also a significant spike in external Gate−to−Source voltages when the switching node voltage negative slope happens. This spike can also be seen on the common drive voltage in Figure 14 at 71.2 μs.

We can integrate the product of the Drain−to−Source voltage and the Drain current to obtain switching losses energies or conduction losses power depending on the integration period (turn−on, turn−off, and conduction time). We can also average the same product over a switching period to get the total losses in each SiC MOSFET.

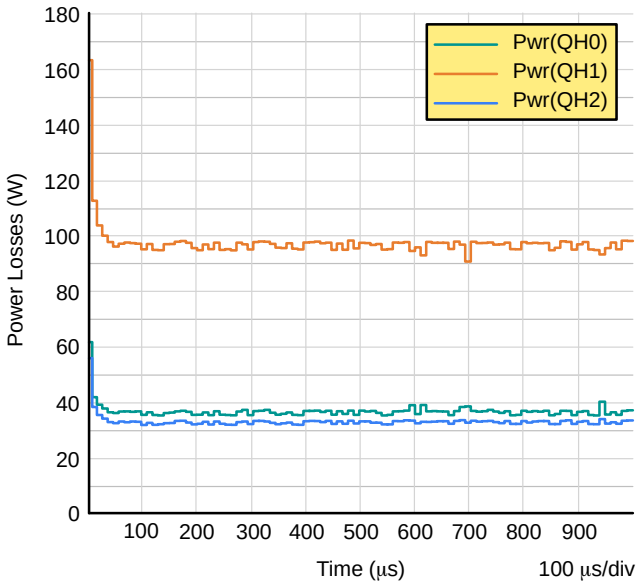

Figure 16. Total Power Losses in Each SiC MOSFET

As expected and demonstrated in Figure 16, the lowest threshold voltage SiC MOSFET has the highest number of total losses.

Looking closer, the lowest threshold, SiC MOSFET, shows slightly less than 100 W. The average threshold voltage one has between 38 W and 39 W, and the SiC MOSFET with the highest threshold has lost 36 W to 37 W.

The switching frequency is not very stable when we use a hysteresis control or self−oscillating feedback. This induces some simulation and calculation errors for each cycle. There are also errors due to simulation accuracy and simulation time step that varies randomly — translated into a kind of noise on the curves.

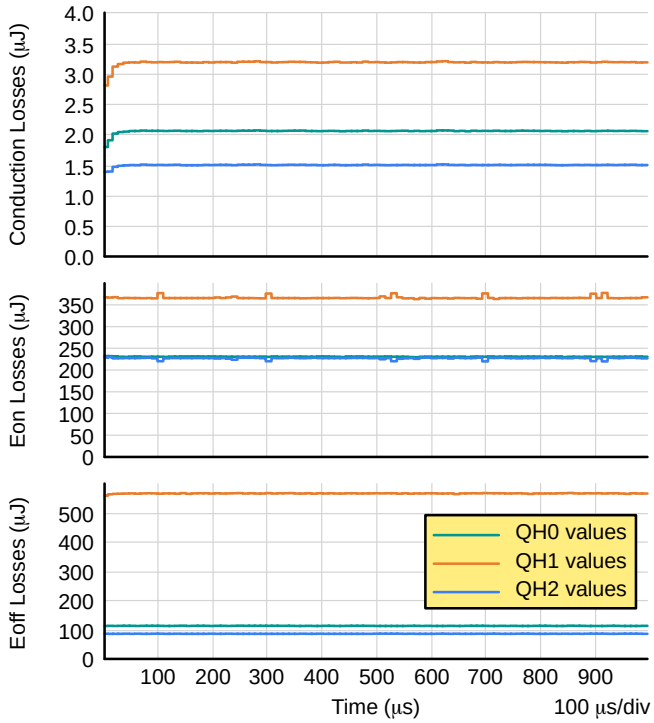

Figure 17. Turn−On, Turn−Off, and Conduction Losses Energies in Each SiC MOSFET

The conduction losses during each switching cycle (see Figure 17) align with the conduction current in each SiC MOSFET. No surprise here.

For turn−on energy, the lowest threshold SiC MOSFET has almost double turn−on energy of 400 μJ on average compared to the others with 250 μJ.

Turn−off energy is much higher in the lowest threshold voltage SiC MOSFET with more than 550 μJ. The average threshold voltage SiC MOSFET has 120 μJ turn−off energy, while the highest threshold voltage SiC MOSFET has only 90 μJ turn−off energy. The difference here is five times more in one MOSFET than the others.

Using Cauer Network To Simulate Thermal Behaviors

All simulation models are available with two (or more) extra nodes to provide information regarding thermal behaviors using the thermo−electrical equivalence. In this equivalence, for one node, Voltage represents the temperature, and the Current represents the power dissipated.

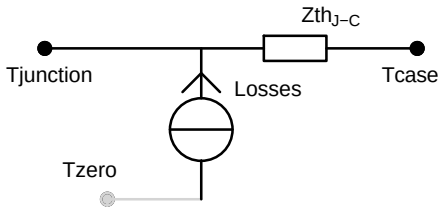

Figure 18. Internal Thermo−Electrical Structure

By connecting the Tcase pin to a fixed voltage source (representing the application's ambient or maximum case operating temperature), we can get the temperature difference between the Case and the Junction. We just need to measure the Tj pin voltage to get it. (See Figure 19)

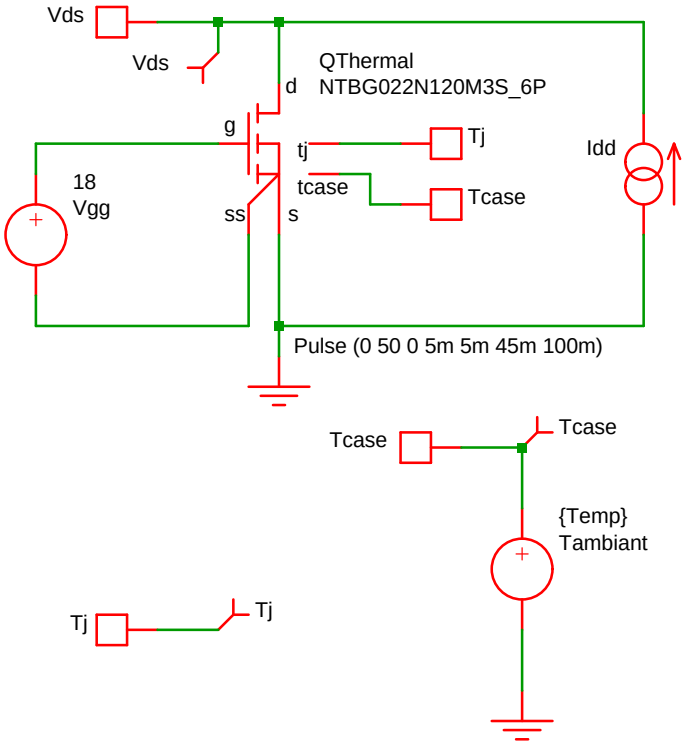

Figure 19. Electro−Thermal Simple Approach

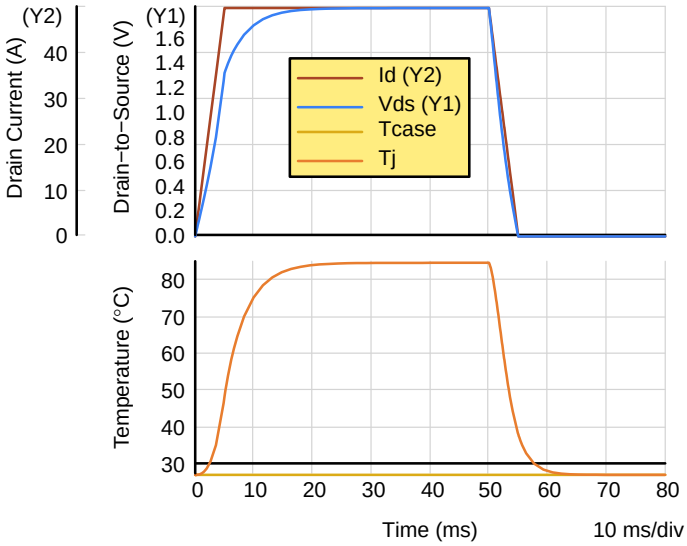

Figure 20. Junction−to−Case Temperature Difference

In the previous graph (Figure 20), we used a current pulse to heat the die. We can see the junction temperature increasing with time and power dissipated in the die. We also see the $R_{DS(on)}$ changing with temperature by looking at the Drain−to−Source voltage slow slope or exponential slope while the current is already at its maximum.

In the next exercise, we will use a D2Pack−7 lead SiC MOSFET mounted on a 1−inch square ground plane (used as a heatsink) on the Printed Circuit Board (PCB).

The most complicated part is to find the Cauer network (Figure 21) representing this PCB heatsink's dynamic performance. To obtain such a network at **onsemi**, we use a finite element simulation tool to model the assembly, extract the performance, and the equivalent Cauer network.

The following schematic gives the equivalent R−C network we will use.

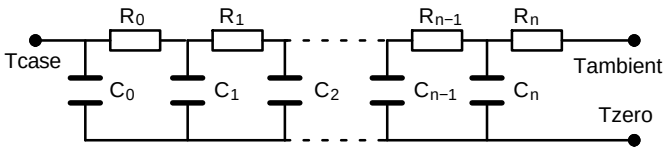

Figure 21. Cauer Network for a 1−Inch Square PCB

Table 1 provides the network values for a 1−inch square PCB.

Table 1. 1−INCH SQUARE PCB HEATSINK CAUER NETWORK VALUE

C0 = 0.00017	R0 = 0.00788	C5 = 0.01306	R5 = 1.78013
C1 = 0.00060	R1 = 0.02038	C6 = 0.04428	R6 = 4.56479
C2 = 0.00145	R2 = 0.07027	C7 = 0.54095	R7 = 6.75559
C3 = 0.00469	R3 = 0.10889	C8 = 1.79805	R8 = 14.31444
C4 = 0.00598	R4 = 0.28112	C9 = 2.30069	R9 = 10.56637

Then, we include this network in the simulation schematic and connect it to the extra "thermal" nodes, as shown in Figure 22.

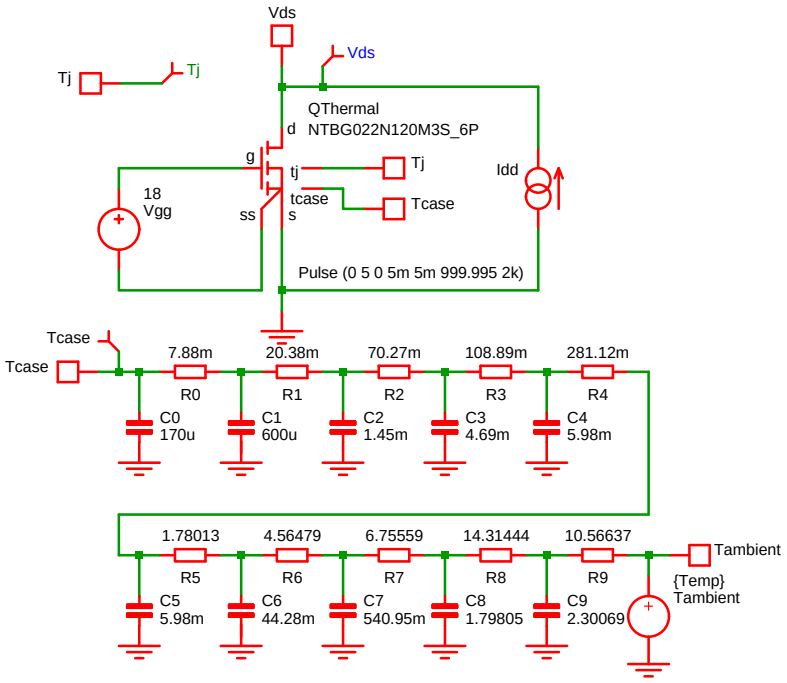

Figure 22. Simulation Schematic with Cauer Network

We can now run the simulation and see how the heat sink evacuates heat. We can also read the Case and Junction temperature but plot voltages on Junction and Case nodes available in the simulation model (See Figure 23).

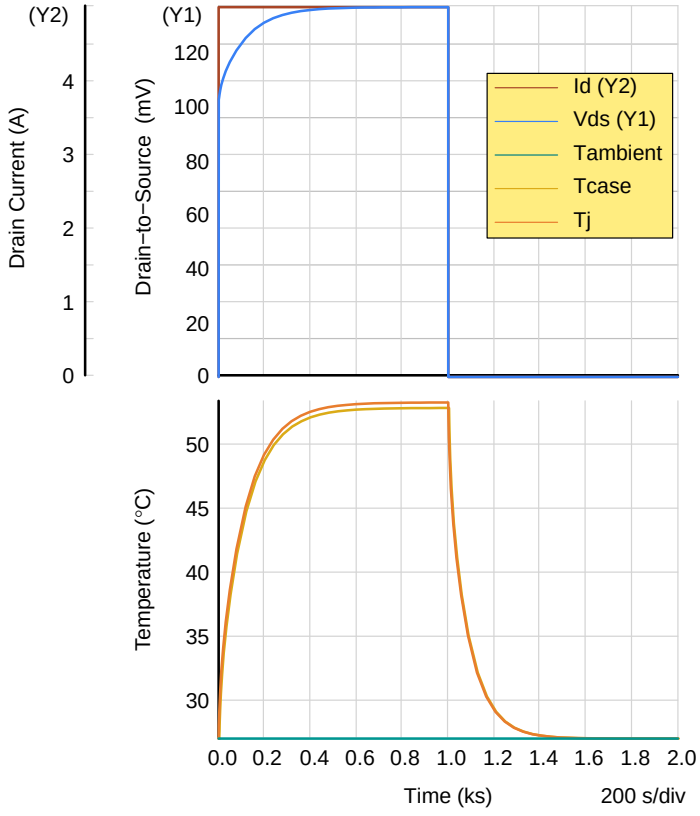

Figure 23. Thermo−Electrical Simulation Results

This is a concise example of what can be done with those extra thermo−electrical pins. If you want to go deeper on Electro−Thermal simulation in Spice, you can read Bénédicte Crosnier de Bellaistre's application note on this topic [11]. This application note covers many more examples and details on Thermo−Electrical simulations.

Evaluation of Gate−Drive−Voltage Level Influence on Switching Losses

In this section, we will take the same die and use this die in various packages. To evaluate the impact of the package parasitic, we will make a switching losses comparison.

The double pulse tester (in Figure 24) is well−known for the measurement of switching performance, and it allows the extraction of Turn−On and Turn−Off energy in a switching event. The current value stays nearly the same between the turn−off and the turn−on event as the freewheeling is almost on a short circuit.

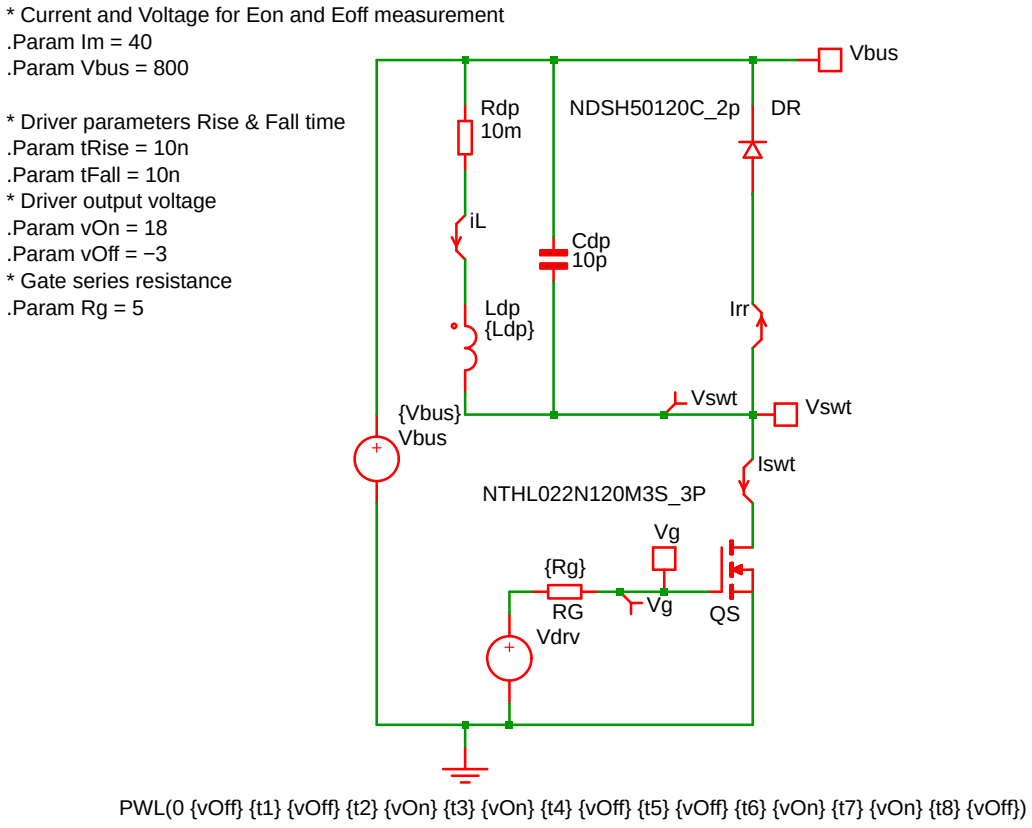

Figure 24. Double Pulse Tester Simulation Schematic

When we run this schematic, we obtain the following waveforms plotted in Figure 25.

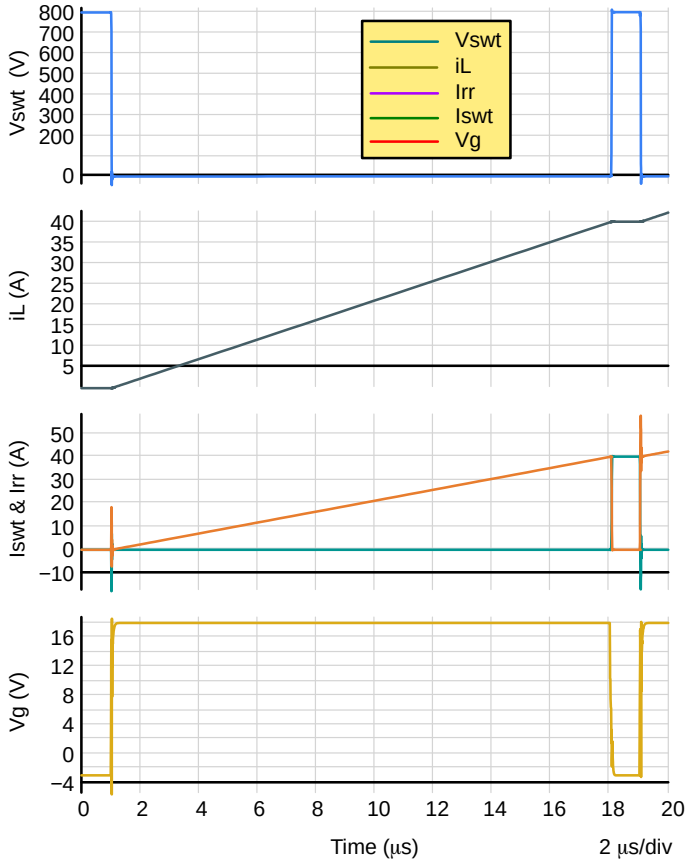

Figure 25. Double Test Waveforms

To measure the switching losses and all parameters (like Turn−On delay, Rise time, etc.), we use the following convention shown in Figure 26.

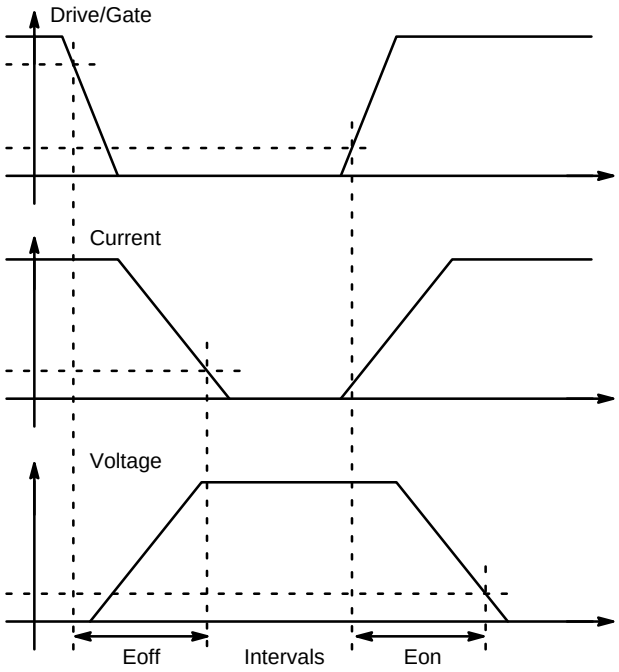

Figure 26. Turn−On and Turn−Off Energy Measurement

We can calculate the losses with some extra formulas directly on the schematic and use cursors to do the measurement. But, if you need to do this several times, the best is to create a simple script that does this for you.

We will look at several gate voltage Minimum and Maximum to see the impact on switching losses with the same setup.

We will not look at the $R_{DS(on)}$ changing with the gate voltage — covered in the datasheet with the on−region graphs.

We obtained the following values listed in the Table below with the new NTH4L022N120M3S (22 mΩ, 1200 V, M3S) MOSFET using a 5 Ω external gate resistor and an NDSH50120C (50 A, 1200 V, D3) diode. The bus voltage setting is 800 V, and the current in the inductor is 40 A. Table 2 shows the results below.

Table 2. TURN−ON AND TURN−OFF ENERGY FOR VARIOUS GATE DRIVE VOLTAGES

V_{GS} Low/Off	V_{GS} High/On	Turn−On	Turn−Off
0 V	12 V	687 μJ	168 μJ
−3 V	12 V	686 μJ	109 μJ
0 V	15 V	467 μJ	169 μJ
−3 V	15V	461 μJ	109 μJ
0 V	18 V	377 μJ	169 μJ
−3 V	18 V	369 μJ	109 μJ

As expected, increasing Gate voltage during turn−on reduces turn−on losses and has almost no impact on turn−off losses. Also expected, having negative Gate voltage during turn−off reduces turn−off losses and has a negligible effect on turn−on losses.

Evaluating Half−Bridge Structures Impact On Switching Losses

In this section, we will always take the same device as the low side switch, change the high side device, and see how this high side device influences the losses of the low side device. In practice, the double pulse tester measurements are done on the low side switch because it is easier to drive a low side switch and measure on the low side, and measuring on the high side will obtain the same results.

There are basically two types of SiC diodes: Schottky or P−N Junction. Schottky is available as discrete, while P−N is a body diode of SiC MOSFET (See Figure 27).

We will analyze switching losses with those two diode types.

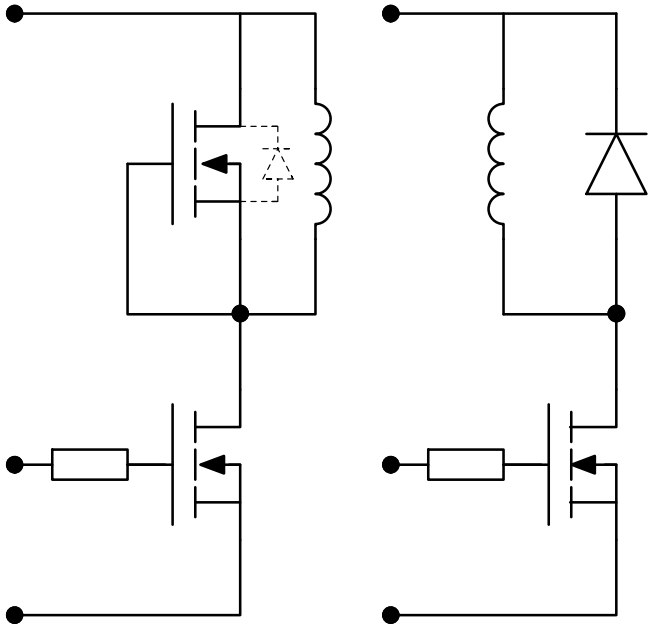

Figure 27. Half−Bridge and Quarter−Bridge Structures

We obtained the results in Table 3 using the new NTH4L022N120M3S (22 mΩ, 1200 V, M3S) and the same setup with a 5 Ω external gate resistor, a bus voltage is set to 800 V, and the current in the inductor set to 40 A. We used the same part for the Half−Bridge configuration for the freewheeling device, and the Quarter−Bridge configuration used the new NDSH50120C (50 A, 1200 V, D3).

Table 3. TURN−ON AND TURN−OFF ENERGY FOR SAME DIE SIZE (10 mΩ, 1200 V, M3S)

Structure	Quarter−Bridge	Half−Bridge
Turn−On	369 μJ	421 μJ
Turn−Off	109 μJ	117 μJ

As expected, using a SiC Schottky diode with much less capacitive and reverse current effects (or losses) than a P−N SiC body diode recovery effect (or losses), the SiC MOSFET switching losses are lower than using a standalone SiC diode.

Evaluating Package Influences on Switching Losses

We will look for losses for devices with the same $R_{DS(on)}$ in various packages. We will use the same conditions as before in a half−bridge configuration with the same device on the high side.

Table 4 shows the results.

Table 4. TURN−ON AND TURN−OFF ENERGY FOR SAME $R_{DS(on)}$ (22 mΩ, 1200 V, M3S) DEVICE

Package	TO247−3L	TO247−4L	D2Pak−7L
Turn−on	1115 μJ	421 μJ	483 μJ
Turn−off	257 μJ	119 μJ	111 μJ
Total	1372 μJ	540 μJ	594 μJ

TO247−4L is the best package for losses with low parasitic. But, as the D2Pak−7L has smaller parasitic (or leads + bounding) inductance than TO247−4L, especially on the drain side, those lower inductances cause the Drain current to increase faster, and the Drain−to−Source voltage drops slower during turn−on, so we get higher losses for D2Pak−7L.

The datasheet values are higher than the ones measured here because the actual test setup has more parasitics than this simple simulation schematic. As we have seen in [8, 9, 10] on the Boost stage example, all extra parasitics can influence losses during turn−on and/or turn−off.

Topologies Analysis with Physical & Scalable Simulation Models

Flying Capacitor Boost

In Figure 28, Flying Capacitor Boost (FCB) is a topology used in solar applications. As panel output voltage increases with power, nominal voltages above 1000 V are used, and the 1200 V device rating is not enough to offer a safe margin in those cases. Stack topologies often overcome this when higher voltage rating devices are unavailable or less efficient. FCB is one of them. It has the advantage of single input and output voltages — no need for split−bus voltages with complex or extra balancing loop to control the middle point voltage.

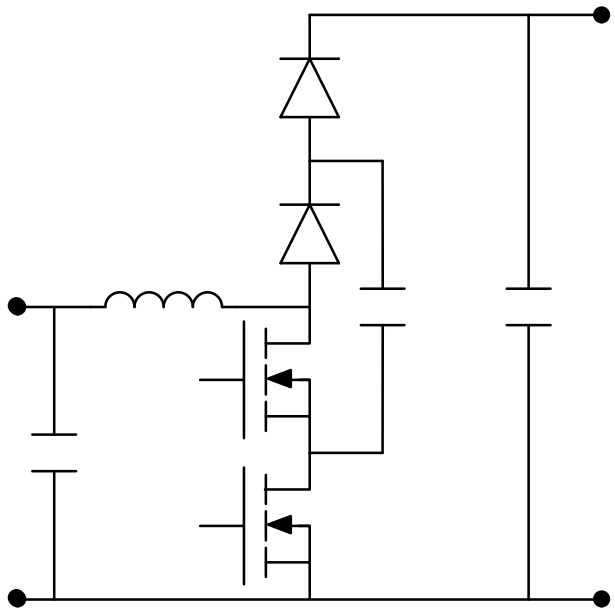

Figure 28. Flying Capacitor Boost Schematic

After reaching a steady state, we can analyze several parameters at this operating point using the results in Figures 29 to 31.

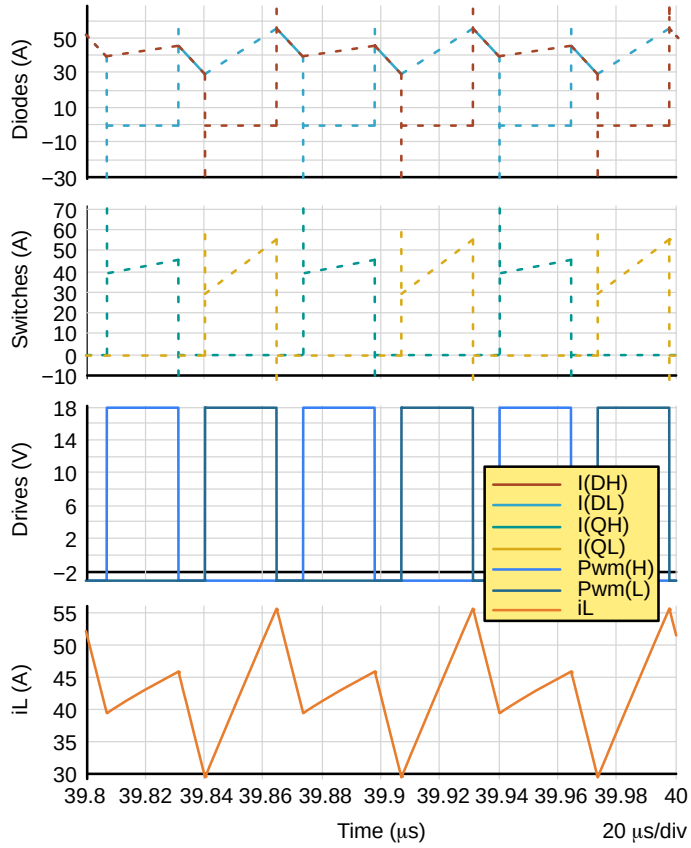

Figure 29. Flying Capacitor Boost Switches Current Waveforms

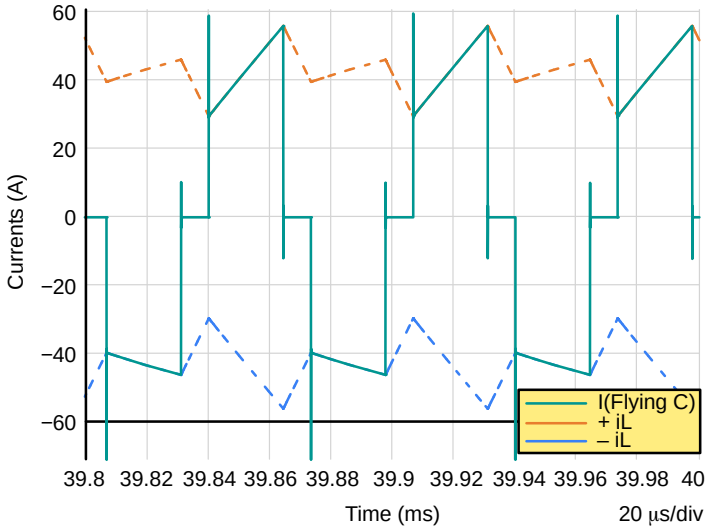

Figure 30. Flying Capacitor Boost Capacitor Current Waveform

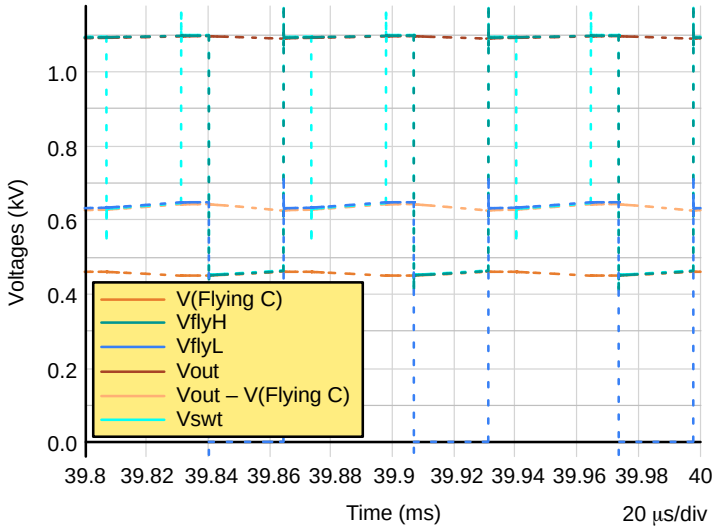

Figure 31. Flying Capacitor Boost Capacitor Voltages Waveforms

We can zoom on MOSFETs and Diodes turn−on and turn−off.

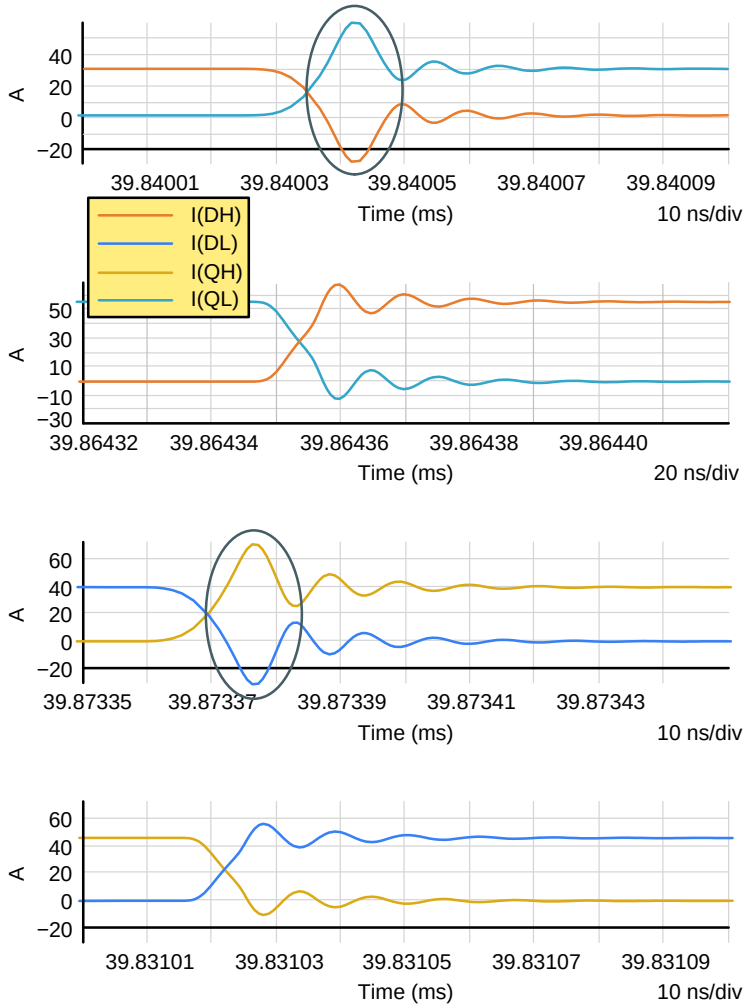

Figure 32. Flying Capacitor Boost Switches Turn−On and Off Current Waveforms Zoom

Figure 33 shows a significant current spike at turn−on for QL and QH. This capacitive energy stored in the SiC Diode Schottky barrier looks like a reverse recovery. We use 2.5 Ω external gate resistors, giving very high dV/dt and di/dt at QL and QH turn−on and turn−off. By increasing the external gate resistor, we will limit these phenomena but increase turn−on duration (and turn−off duration if there is the same resistor for turn−on and turn−off, as in this simulation schematic) and turn−on losses (and turn−off losses). It is always a compromise.

It is straightforward to get the average power losses in a device using the thermal−electrical equivalence with thermo−electrical simulation models. As we know, in this equivalence, the current represents power (and Voltage represents temperature). So, measuring the current out of the TCase pin will give us the power flow. The internal Cauer network modeling the device's thermal impedance, acting as a "very" low pass filter, filters this power flow. So, simulating on a "long time" scale (around milli−second, most of the time) gives us the average power losses in each active component if we make a DC−DC power stage.

Let's see what we get here with this Flying Capacitor Boost.

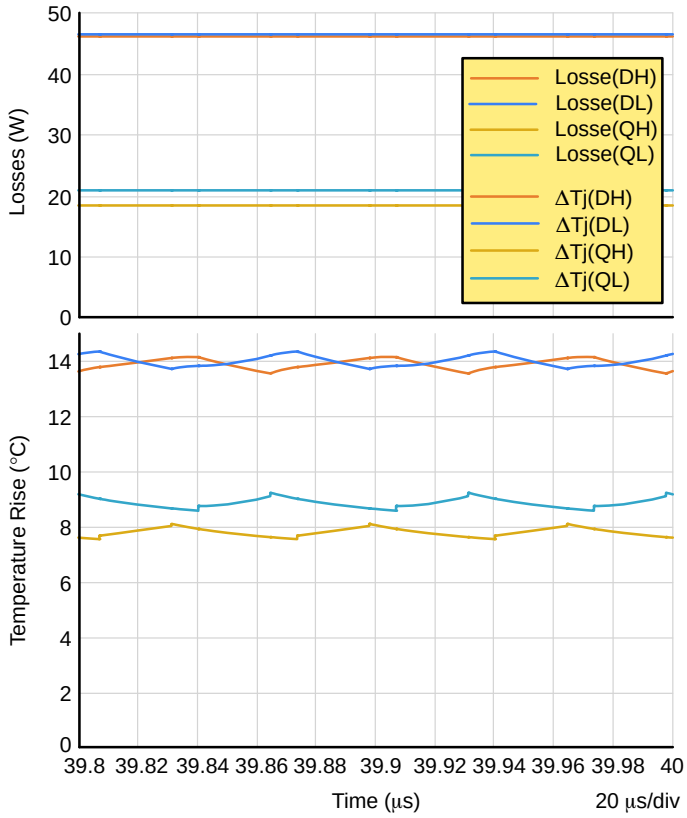

Figure 33. Losses Measurement Using "TCase" Pin Current/Power Flow and Junction Temperature Rise

The ΔTj curves show sudden increases at turn−on and turn−off. The losses and ΔTj are not the same for all active devices because the Flying Capacitor voltage value is not equal to half the output voltage value. This is also why the inductor current doesn't have the saw tooth shape (Figure 33).

We run the schematic with various external gate resistor values (Rg = 2.5 Ω; 5 Ω; 10 Ω). Figure 34 and Table 5 show the impact on the current spike during the MOSFET turn−on.

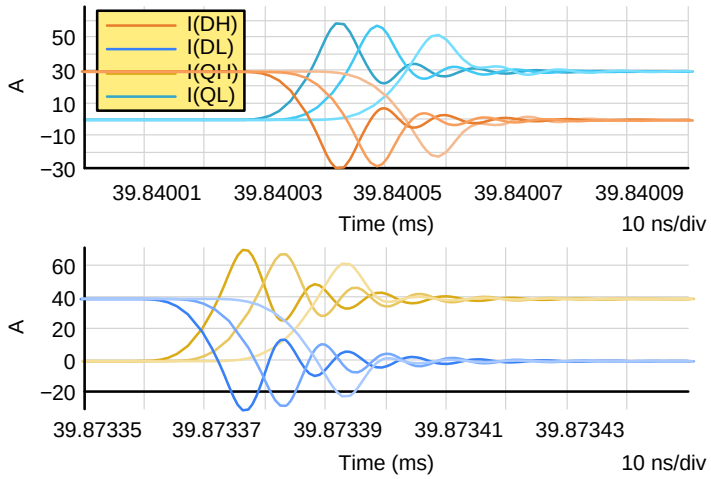

Figure 34. Flying Capacitor Boost MOSFETs Turn−On Current Waveforms Zoom vs. External Gate Resistor

Dark color curves are for Rg = 2.5 Ω; Medium−light color curves are for Rg = 5 Ω; Light color curves are for Rg = 10 Ω.

Table 5. CURRENT SPIKE PEAK VALUES FOR VARIOUS EXTERNAL GATE RESISTORS

External Gate Resistor	Negative Peak I(DH)	Negative Peak I(DL)
Rg = 2.5 Ω	−29.3 A	−30.6 A
Rg = 5 Ω	−27.8 A	−28.4 A
Rg = 10 Ω	−22.3 A	−22.3 A

Figure 35 shows the impact on losses and junction temperature rise when using Rg = 10 Ω.

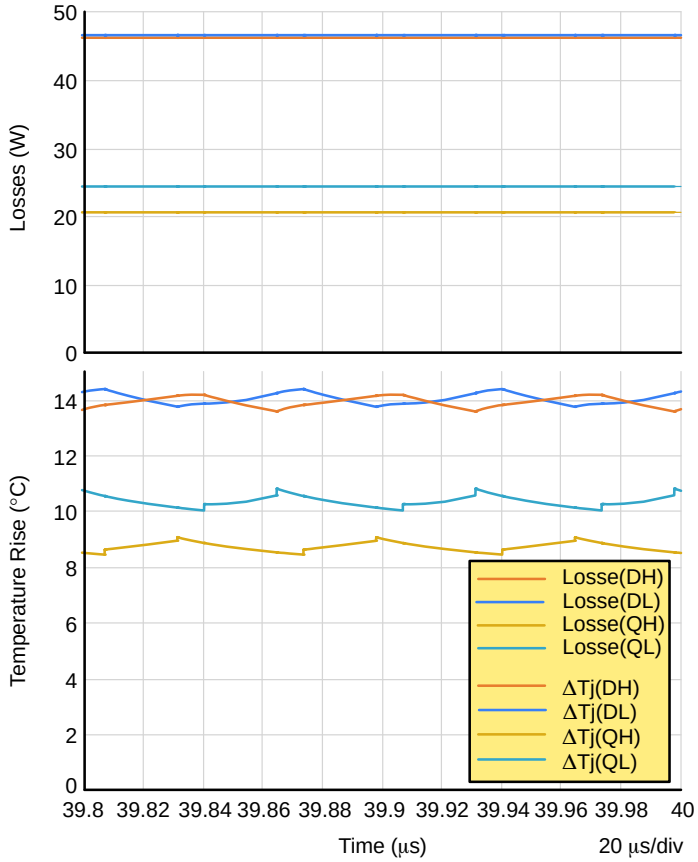

Figure 35. Losses and Junction Temperature Rise with High External Gate Resistor

For losses and Junction temperature rise in Figure 35 obtained with Rg = 10 Ω, we used the same scale as in Figure 33 for Rg = 2.5 Ω. We can compare the impact of the lower diode negative spike and longer switching time on losses and Junction temperature rise. As the capacitive energy stored in the diode dissipates in the MOSFET, diodes are not affected by the external gate change effects. We have the same losses and Junction temperature rise in both situations. But, as expected, the longer commutation durations with Rg = 10 Ω increase the losses and Junction temperature rise in both MOSFETs. The difference is around 1°C for the temperature and 2 to 3 W for losses.

I−type vs. T−type Neutral Point Clamp

Many applications in energy infrastructure use these two types (or three, considering A−NPC) of switching cells widely, as shown in Figure 36.

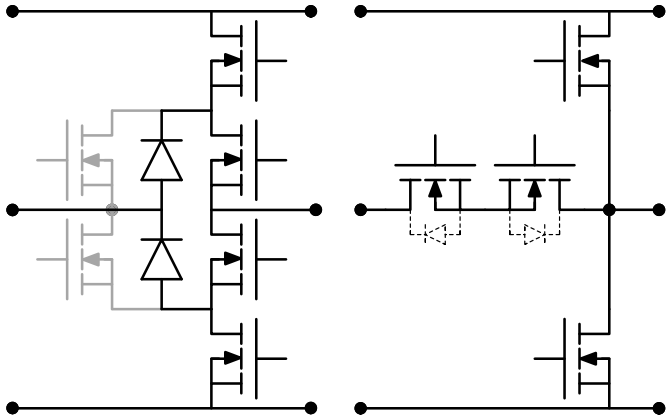

Figure 36. I−NPC (A−NPC in Grey) and T−NPC Cells

Using simulation, we can compare them and extract performance parameters at various operating points.

Here, we will compare these three structures in a Buck stage (for an inverter application) operating from 400 V down to 200 V with 20 A. To make the simulation faster, we will run the cells in DC−DC, so only the high−side switches are operating. We will use a self−oscillating control to avoid feedback loop stability issues and operate near the 100 kHz switching frequency. This way, we reach an almost stable point in 2 cycles. Then, the simulation runs to get to thermal equilibrium, taking much longer because thermal impedance is a very low time constant.

For the T−NPC, we can have two Gate drive strategies: first, using the MOSFET body diode for freewheeling in the Neutral Clamp branch and, second, drive this freewheeling MOSFET with the complementary switching signal used for the main switch (SR T−NPC in Table 6). We will try various structures with various Diode and MOSFET generations.

Our 650 V SiC MOSFET second generation (M2) is not designed to operate at such a high switching frequency, while our third generation (M3S) is adequate. So, we expect higher losses with 650 V M2 than with 1200 V M3S.

Table 6. TURN−ON AND TURN−OFF ENERGY FOR VARIOUS NEUTRAL POINT CLAMP SETUPS

Topology	I−NPC	I−NPC	I−NPC	A−NPC	A−NPC	T−NPC	SR T−NPC	SR T−NPC
QsH	M2 32.6 W	M2 18.7 W	M3S 7.8 W	M2 36.3 W	M3S 7.7 W	M3S 8.6 W	M3S 6.5 W	M3S 8.6 W
QdH/DH	D1 11.5 W	D2 10.9 W	D2 10.9 W	M2 18.1 W	M3S 18.8 W	M3S 50.4 W	M2 61.4 W	M3S 26.2 W
QmH	M2 4.4 W	M2 4.3 W	M2 4.3 W	M2 4.4 W	M3S 6.2 W	M3S 3.0 W	M2 2.2 W	M3S 3.1 W
Total	48.5 W	33.9 W	23.0 W	58.8 W	32.7 W	62 W	70.1 W	37.9 W

If we analyze the results in Table 6, A−NPC with recovery losses but lower−voltage drop than a Schottky doesn’t bring better efficiency. I−NPC remains the best option between the two. This trade−off also depends on the switching frequency, which is 90 kHz, and at a lower switching frequency, A−NPC could be the best choice.

T−NPC without driving the neutral clamp device during off−time yields awful results even if we use M3S devices due to the P−N junction body diode of the SiC MOSFET. But, if we drive the SiC MOSFET like a Synchronous Rectifier (SR T−NPC), we get good efficiency with M3S while M2 is worse due to the bad high−frequency performances. SR T−NPC cell structure is popular and widely adopted in new designs because it has good performance and requires only four devices compared to I−NPC or A−NPC, which requires six devices.

6−Pack Boost Active Front End

In Fast DC Charging, the 6−Pack Boost (Figure 37) is often used as an Active Front End or Power Factor Corrector when the power flow is bidirectional.

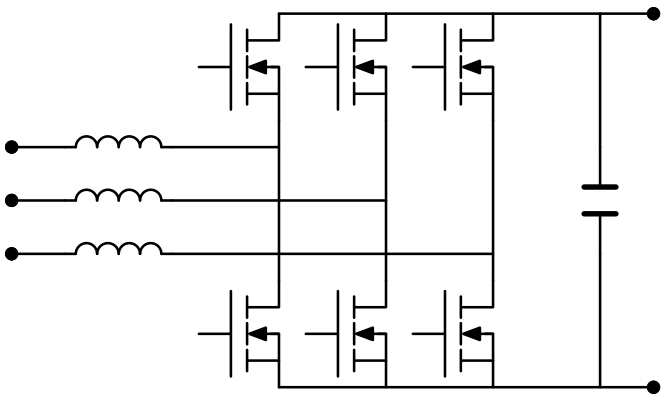

Figure 37. 6−Pack Boost Power Stage

The control involves D−Q transforms. The Third harmonic injection to reduce bus voltage or modulation index can be included or activated to analyze the influence on overall losses. We have also implemented a Feed−Forward action to minimize feedback effort to predict the operating duty cycle depending on the input voltage and the theoretical output value (Figures 41 and 42). So, the control loop only compensates for dynamic effects (like temperature, dispersions, delays, etc.) and the mismatch between theoretical and instantaneous output voltage. We used the Sinewave Pulse Width Modulation (SPWM) to generate each duty cycle. It is not the most efficient method, but it is straightforward to implement. A simple dual ramp sawtooth signal is necessary to make a symmetrical dual−edge modulation for all switches with simple comparators.

As the topology is bidirectional, no discontinuous mode facilitates the compensator design. We have used one PI compensator for the outer output voltage control loop. For the two inner current loops, we also applied a PI compensator for the Direct and the Quadratic contents. Figure 40 shows feedback errors and normalized control variables, which are the same with or without the 3rd harmonic.

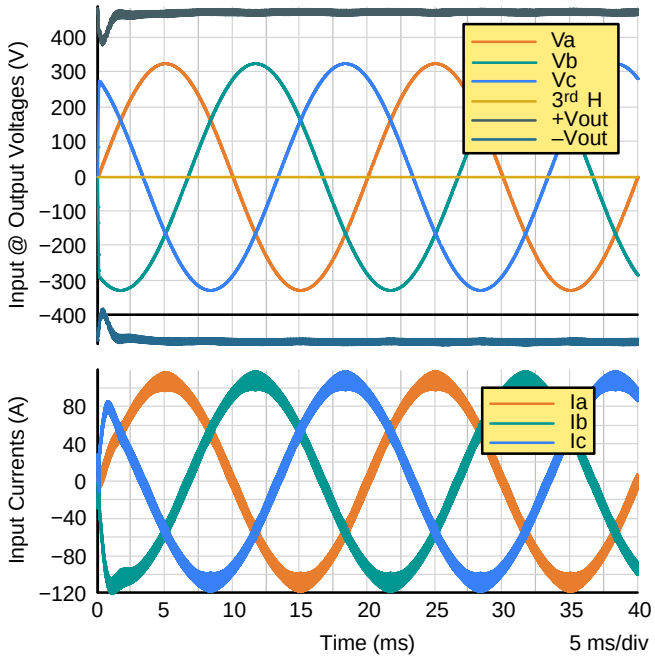

Figure 38. Input and Output Waveforms WITHOUT 3rd Harmonic Injection

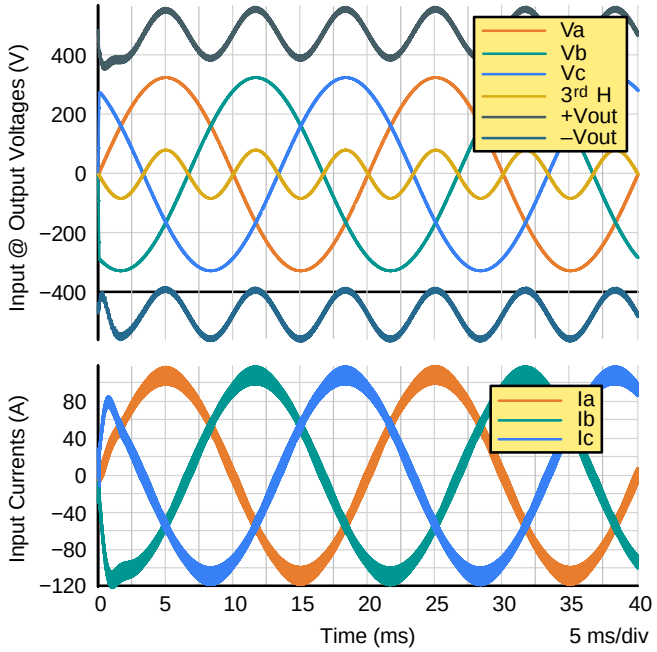

Figure 39. Input and Output Waveforms WITH 3rd Harmonic Injection

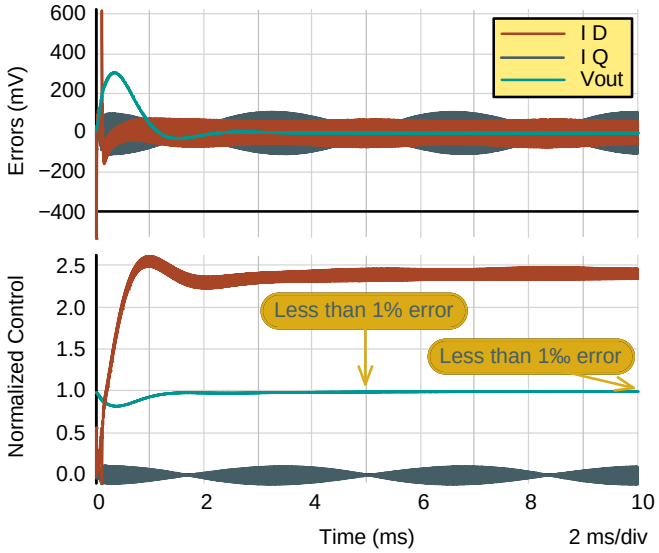

Figure 40. Control variables and Error Variables. Control and Error Are Not Affected by 3rd Harmonic

We will use the average European grid voltage values (230 VAC, 50 Hz) for the example here. The output voltage is 950 VDC, and the output power is 52 kW (Figures 38 and 39).

We have included some parasitic components with realistic values taken from the component datasheets for the boost inductor and the output capacitor. For the SiC MOSFET, each location uses the new 22 mΩ 1200 V M3S TO247−4L (NTH4L022N120M3S). If we use several devices in parallel, we can encapsulate them in a subcircuit to facilitate the re−use of the schematic. This also gives us the flexibility to change the switches' configuration at once and faster if we want

to try 1, 2, or more in parallel for various output powers and find the optimum configuration. For example, the schematic shown in the Annex uses three devices in parallel.

The objective here is to study the switching performances of the Silicon Carbide MOSFET and extract system losses. We will do this analysis with and without 3rd harmonic injection.

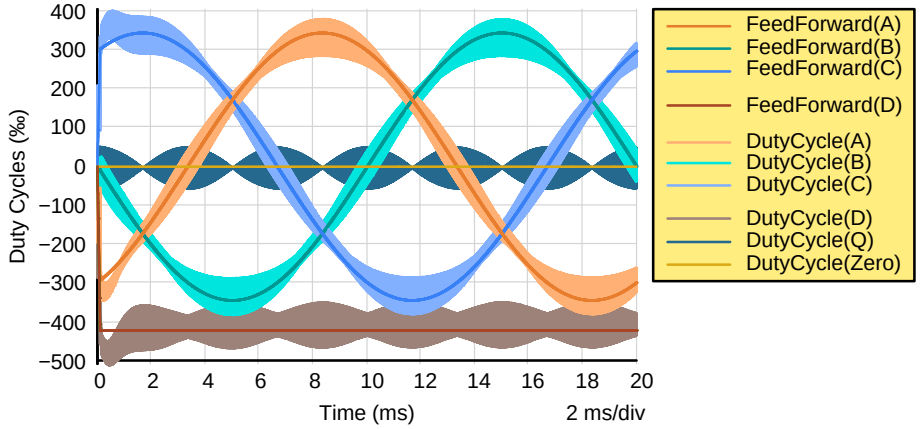

Figure 41. Feed Forwards and Duty Cycles WITHOUT 3rd Harmonic Injection

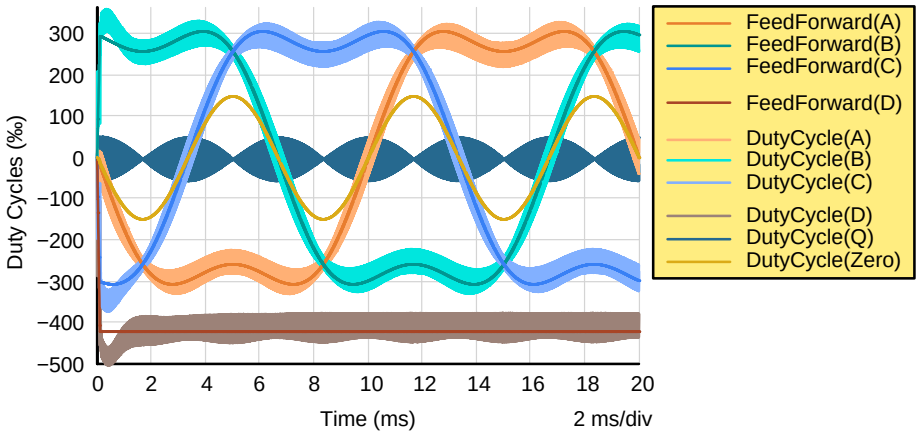

Figure 42. Feed Forwards and Duty Cycles WITH 3rd Harmonic Injection

To avoid overloading the simulator with losses calculation, we will use a script to perform these calculations at the end and display the results as text and curves.

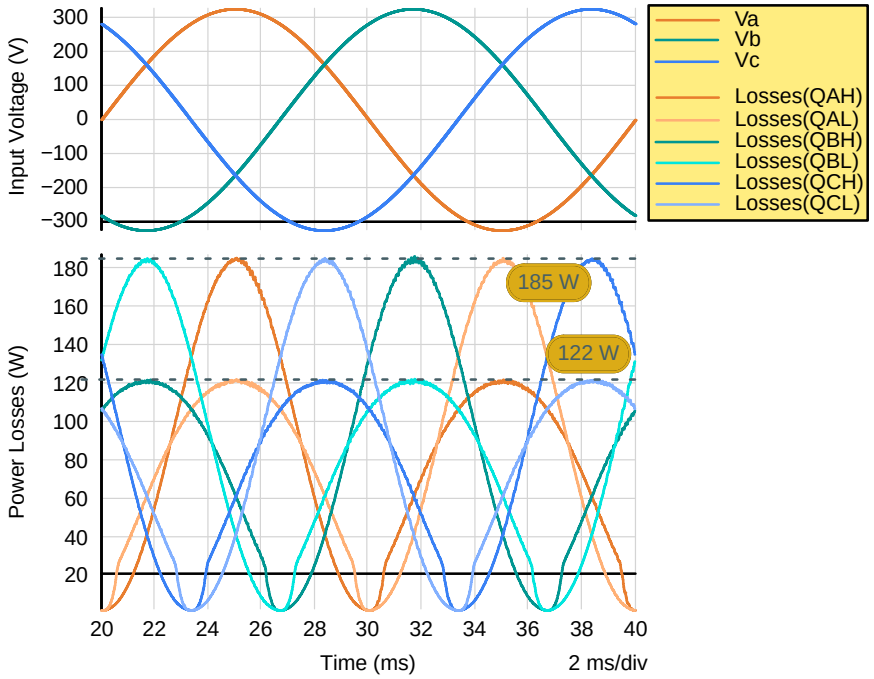

Figure 43. Losses without Third Harmonic Injection Over On Grid Period

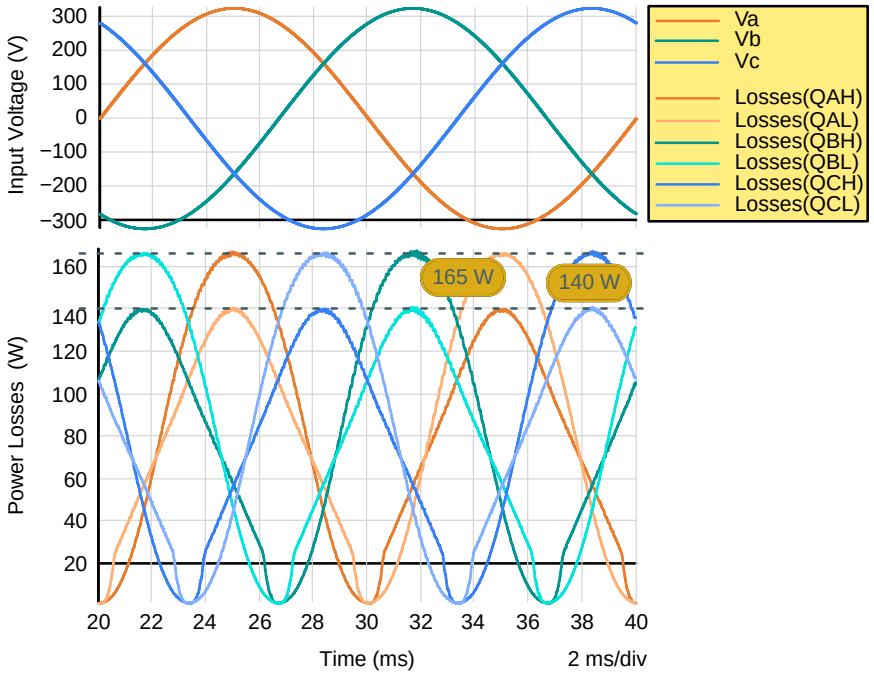

Figure 44. Losses with Third Harmonic Injection Over On Grid Period

Analyzing Figures 43 and 44, we can conclude: that using the third harmonic balances the losses more between the high side and low side switches in each half sine wave cycle. Without the third harmonic injection, the two peaks for each half−cycle are around 122 W and 185 W, while the third harmonic injection peaks are around 140 W and 165 W.

The average results over a grid period given by the script are in the following Table 7.

Table 7. AVERAGE LOSSES OVER A GRID CYCLE

Device	Without 3rd H	With 3rd H
QAH	83.56 W	83.69 W
QAL	83.55 W	83.69 W
QBH	83.55 W	83.68 W
QBL	83.53 W	83.68 W
QCH	83.55 W	83.68 W
QCL	83.54 W	83.69 W
Total	501.29 W	502.11 W

If we consider some errors due to numerical accuracy over a long simulation period, we can say total losses are the same with or without a third harmonic injection. This is a well know statement, and simulation using the Physical and Scalable model confirms this statement.

Conclusion

In the examples shown in the first part, we explained how to access the internal die inside the package, including direct at the die level — very helpful to evaluate stress on the die and remove package parasitic influences. We also demonstrate how to use Cauer networks, where the application note [11] will give you much more details.

Additionally, in this first part of the paper, we have shown how the package and the structure can influence losses in double pulse testing or measurement.

The second part of the paper focused on actual power stage analyses. We explored how those stages operate under actual conditions for various structures (I−NPC, T−NPC, FCB, 6−Pack). We also explored the switching performances. We closed the loop on the 6−Pack Boost Active Front End with D−Q transform, PI compensators, and Sine wave Pulse Width Modulation

Simulation can be beneficial in analyzing various device behaviors and systems performances.

Acknowledgment

I greatly appreciate the assistance provided by Mr. John Warner from SIMetrix in creating all scripts used in this paper.

I want to thank Bénédicte Crosnier de Bellaistre and Jonathan Harper for their help in the session regarding Cauer network and NPC+FCB topologies, respectively.

I am also immensely grateful to James Victory and his entire team for their tremendous support anytime I submitted simulation issues I have found over the last five years. They did a great job creating those models and solving all problems surrounding them. Simulation models are much more robust, and it is difficult to find an issue. My simulations now run from the first time unless I did something wrong.

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Annex: Simulation Schematics

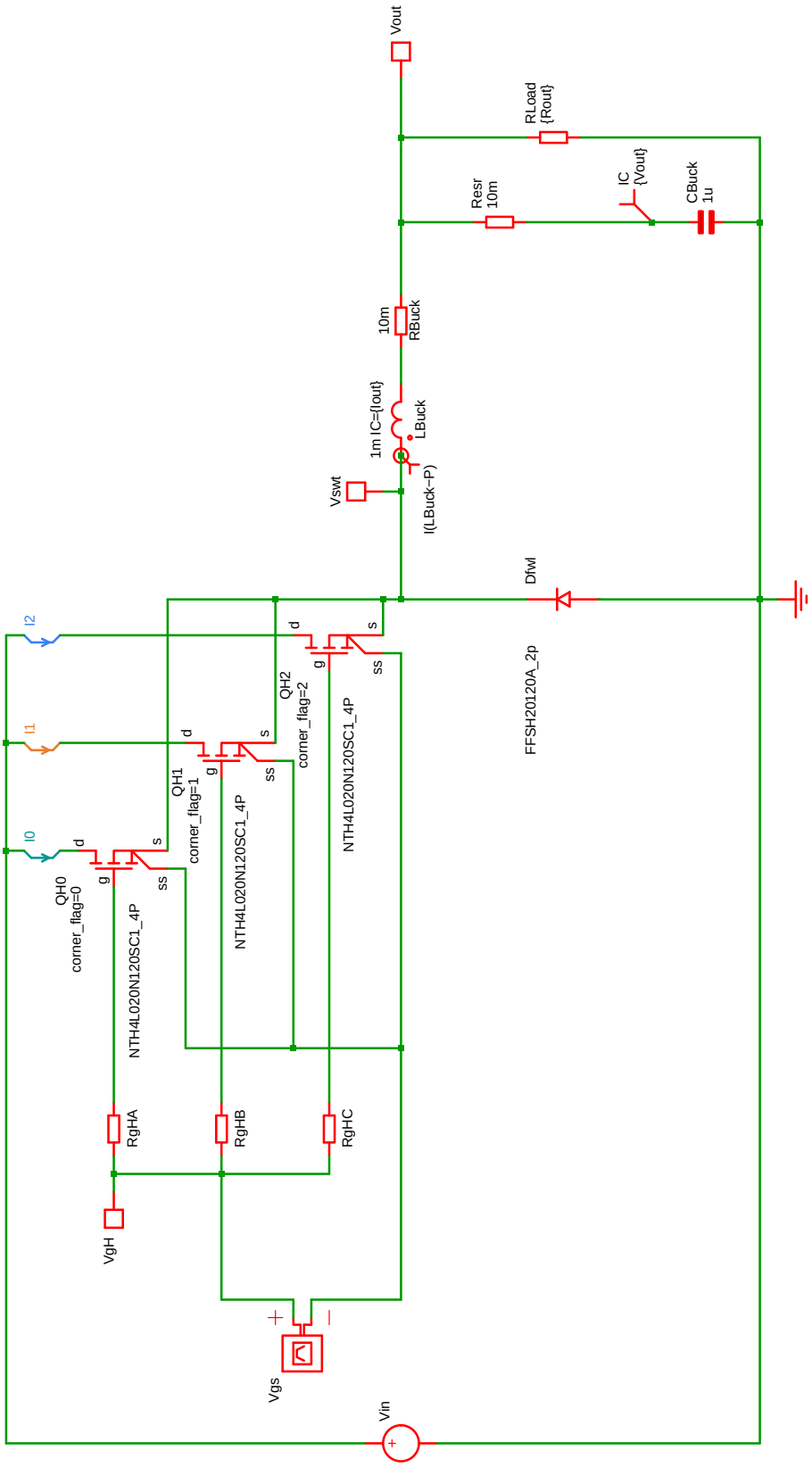
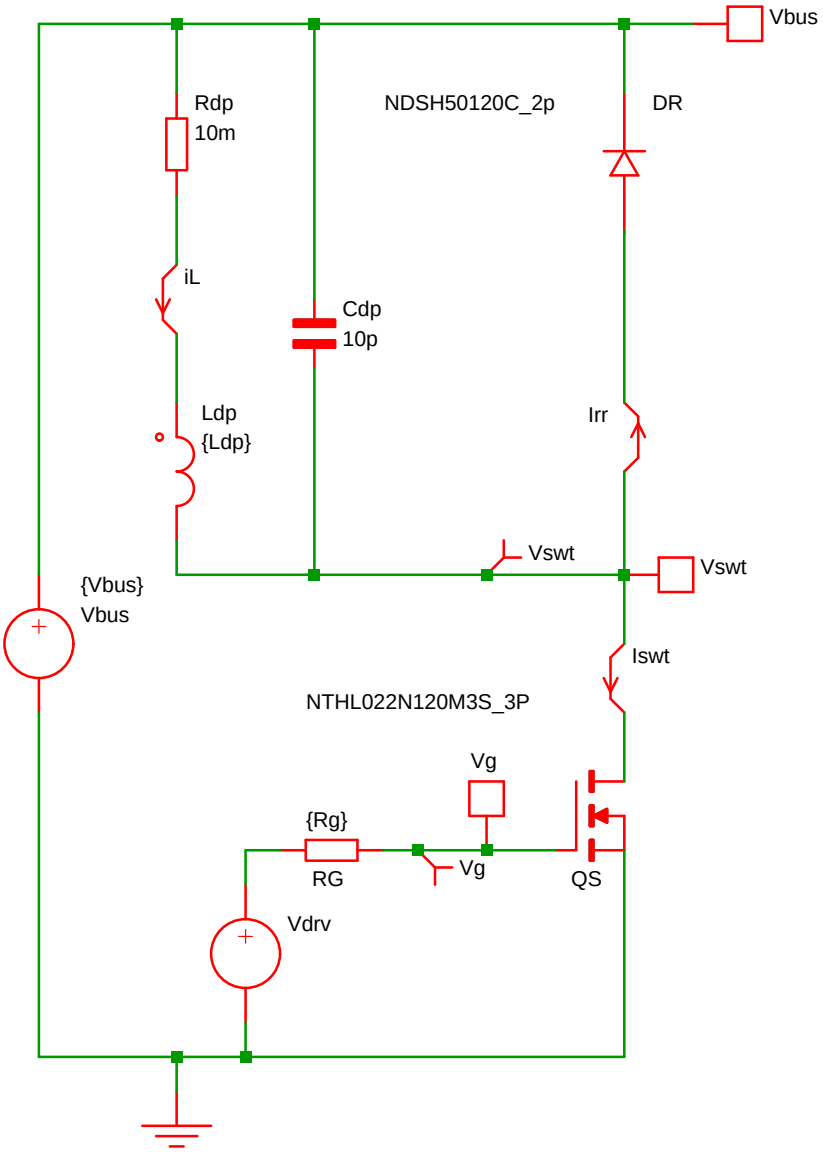


Figure 45. Buck Stage for Corner Effects Analysis

* Current and Voltage for Eon and Eoff measurement
.Param Im = 40
.Param Vbus = 800

* Driver parameters Rise & Fall time
.Param tRise = 10 n
.Param tFall = 10 n
* Driver output voltage
.Param vOn = 18
.Param vOff = −3
* Gate series resistance
.Param Rg = 5



PWL(0 {vOff} {t1} {vOff} {t2} {vOn} {t3} {vOn} {t4} {vOff} {t5} {vOff} {t6} {vOn} {t7} {vOn} {t8} {vOff})

Figure 46. Double Pulse Tester

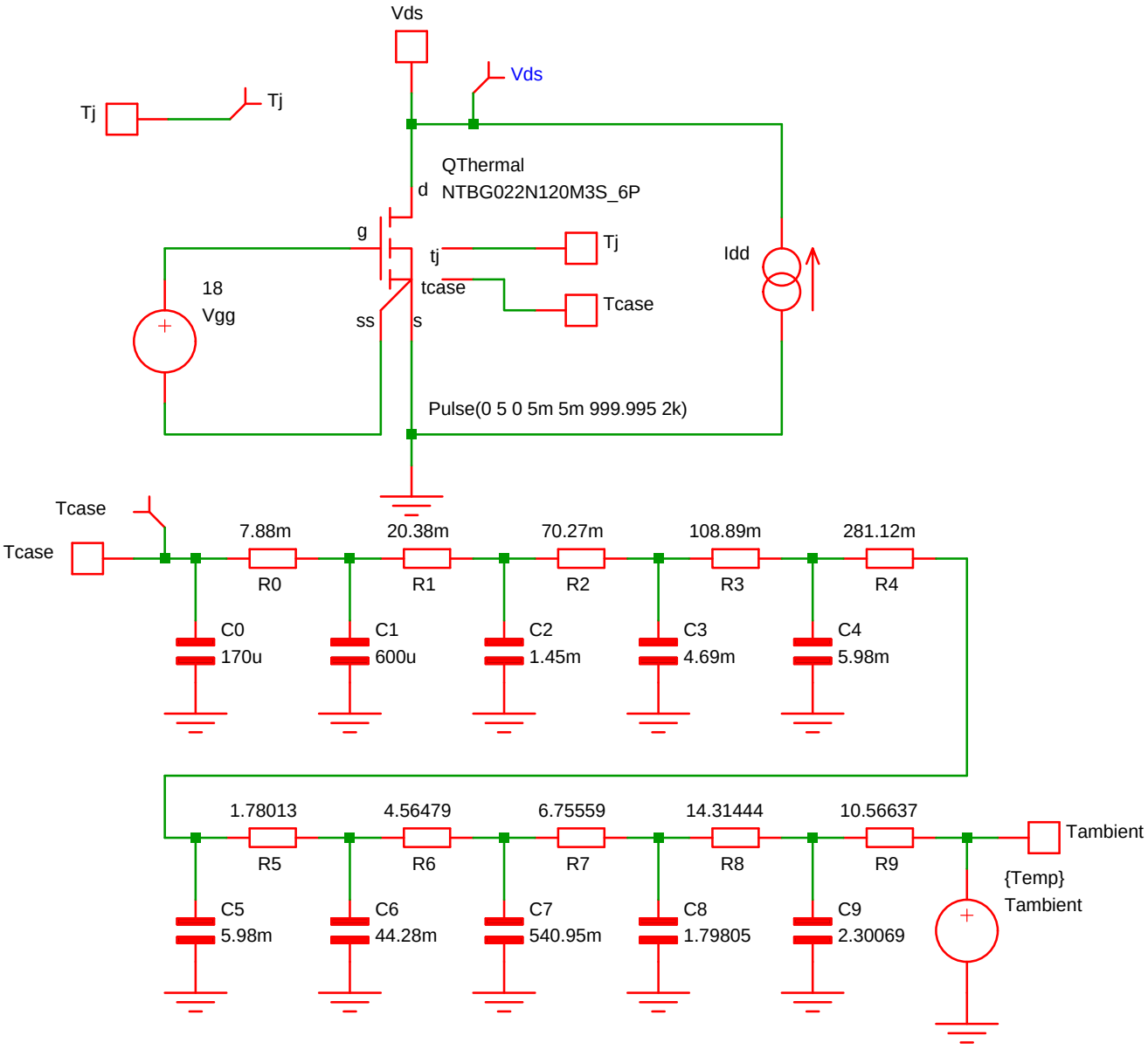


Figure 47. Cauer Network Example

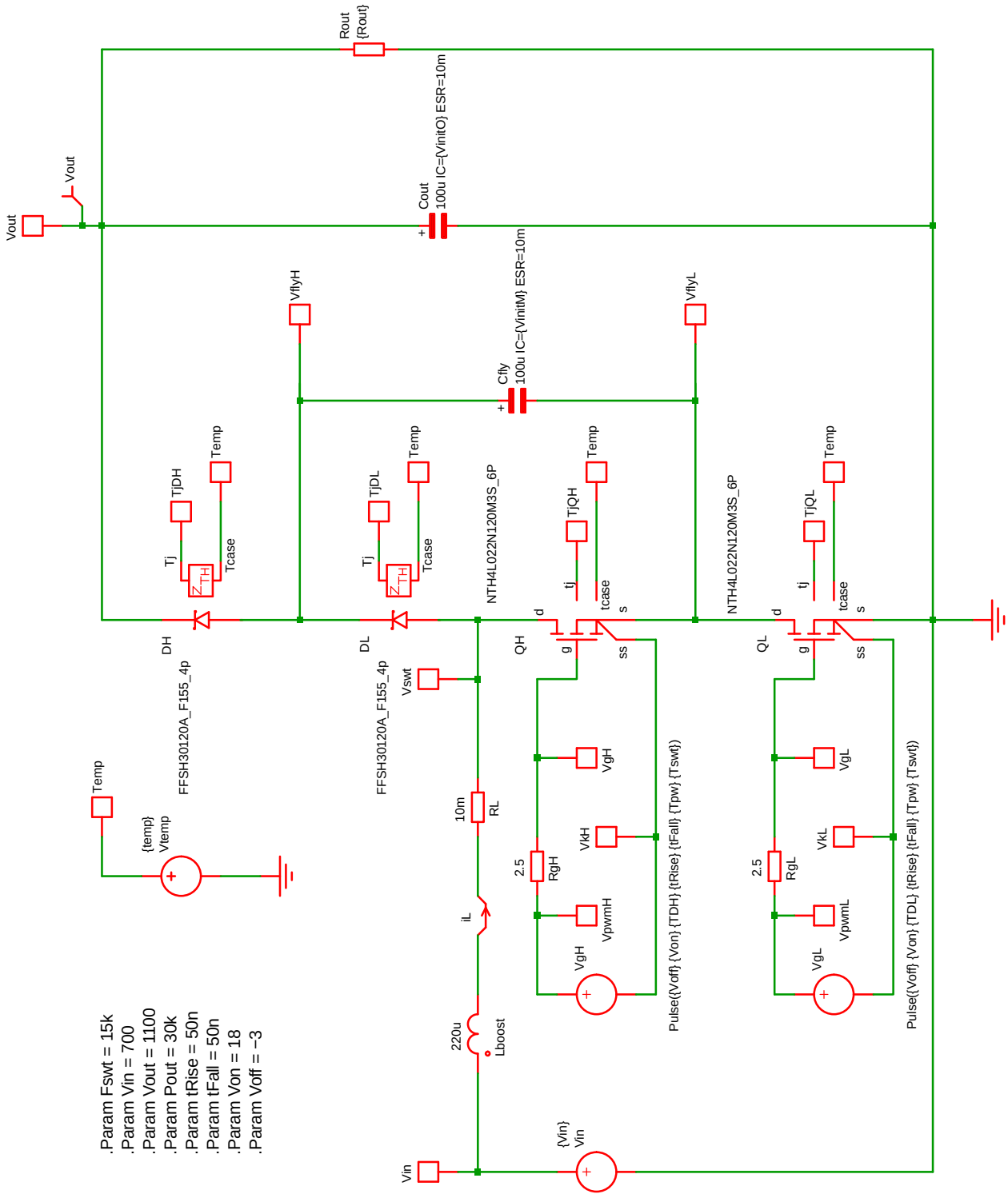


Figure 48. Flying Capacitor Boost (FCB)

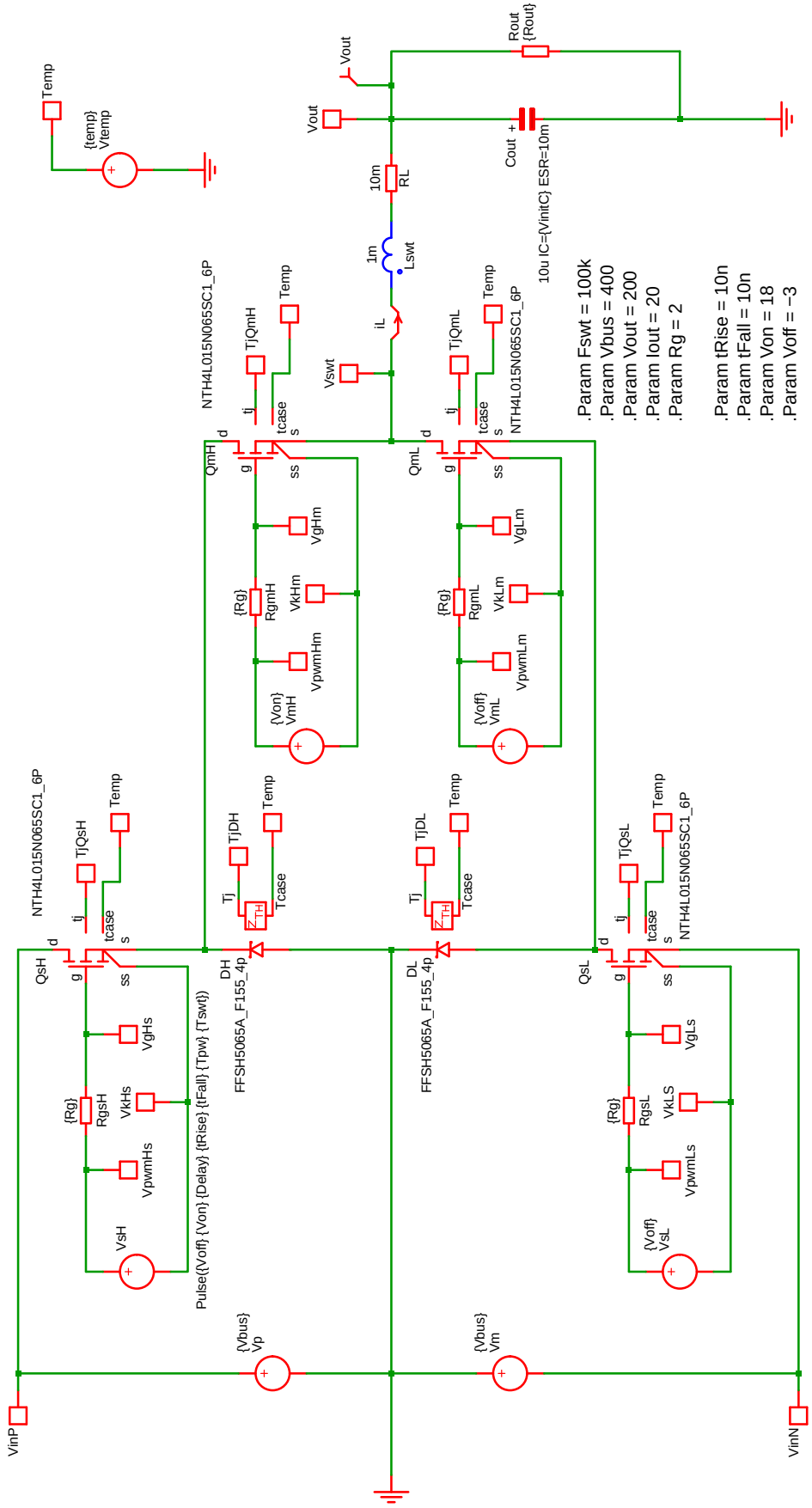


Figure 49. I−NPC Buck

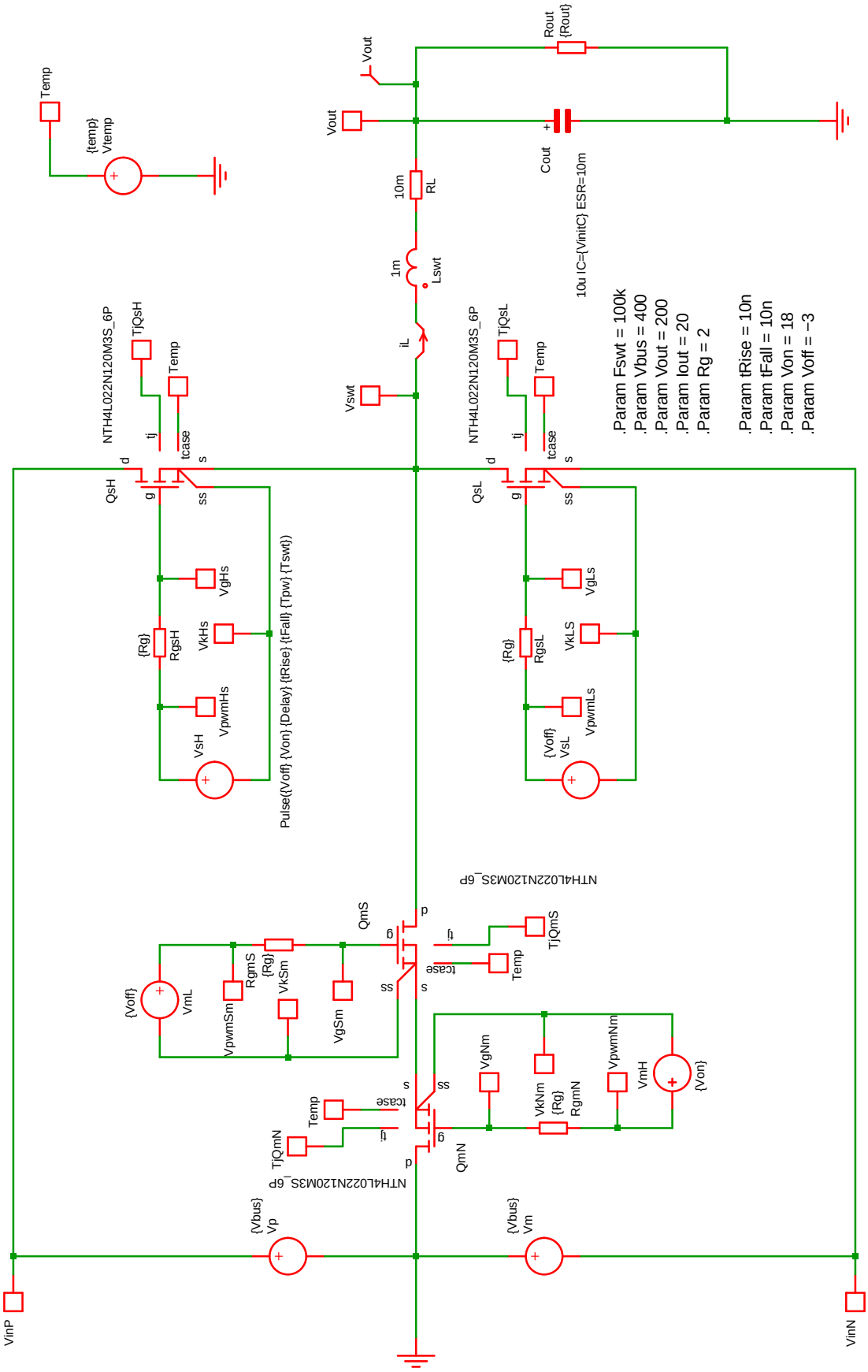


Figure 50. T−NPC Buck

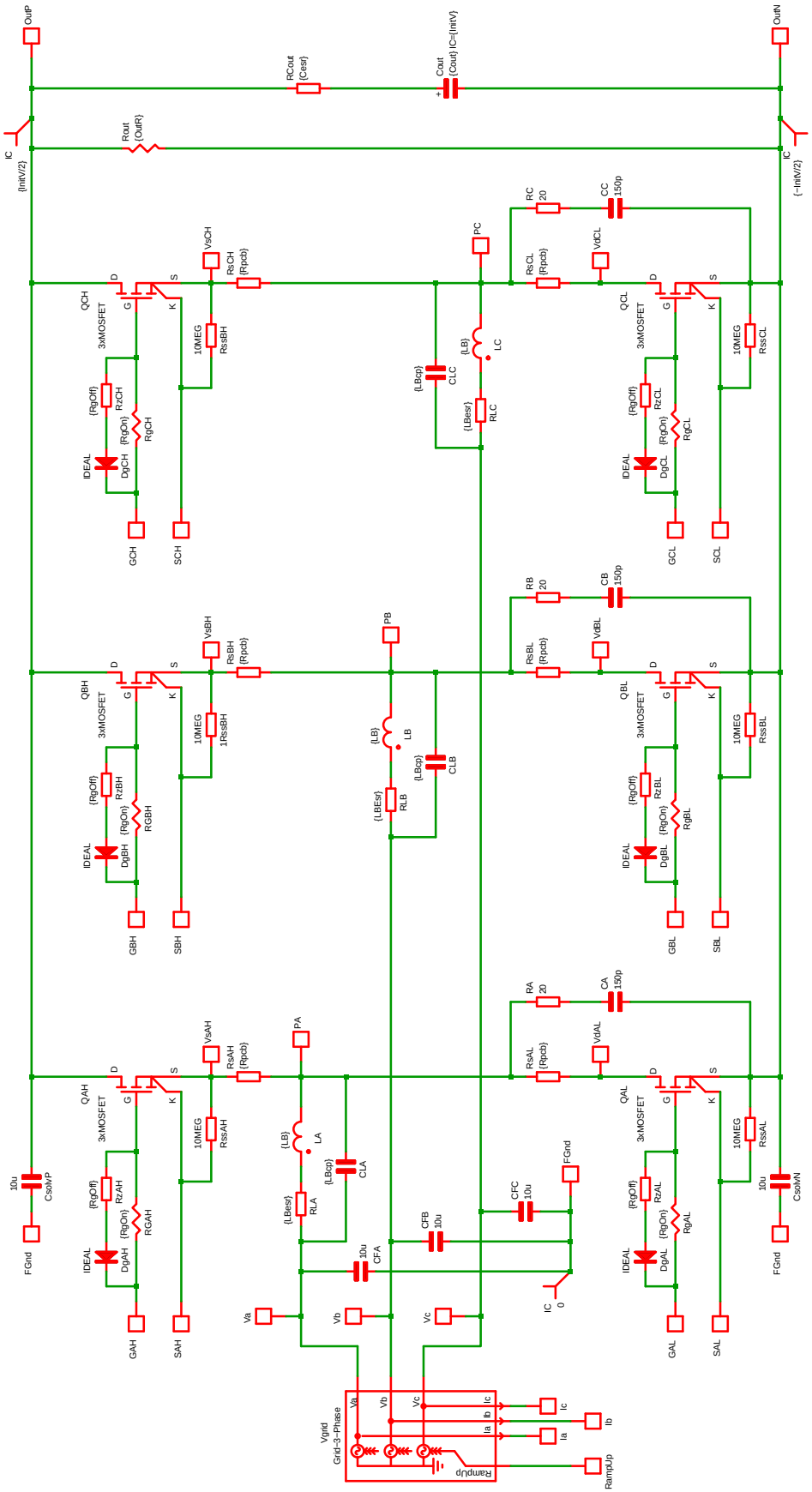


Figure 51. 6−Pack Boost Power Stage

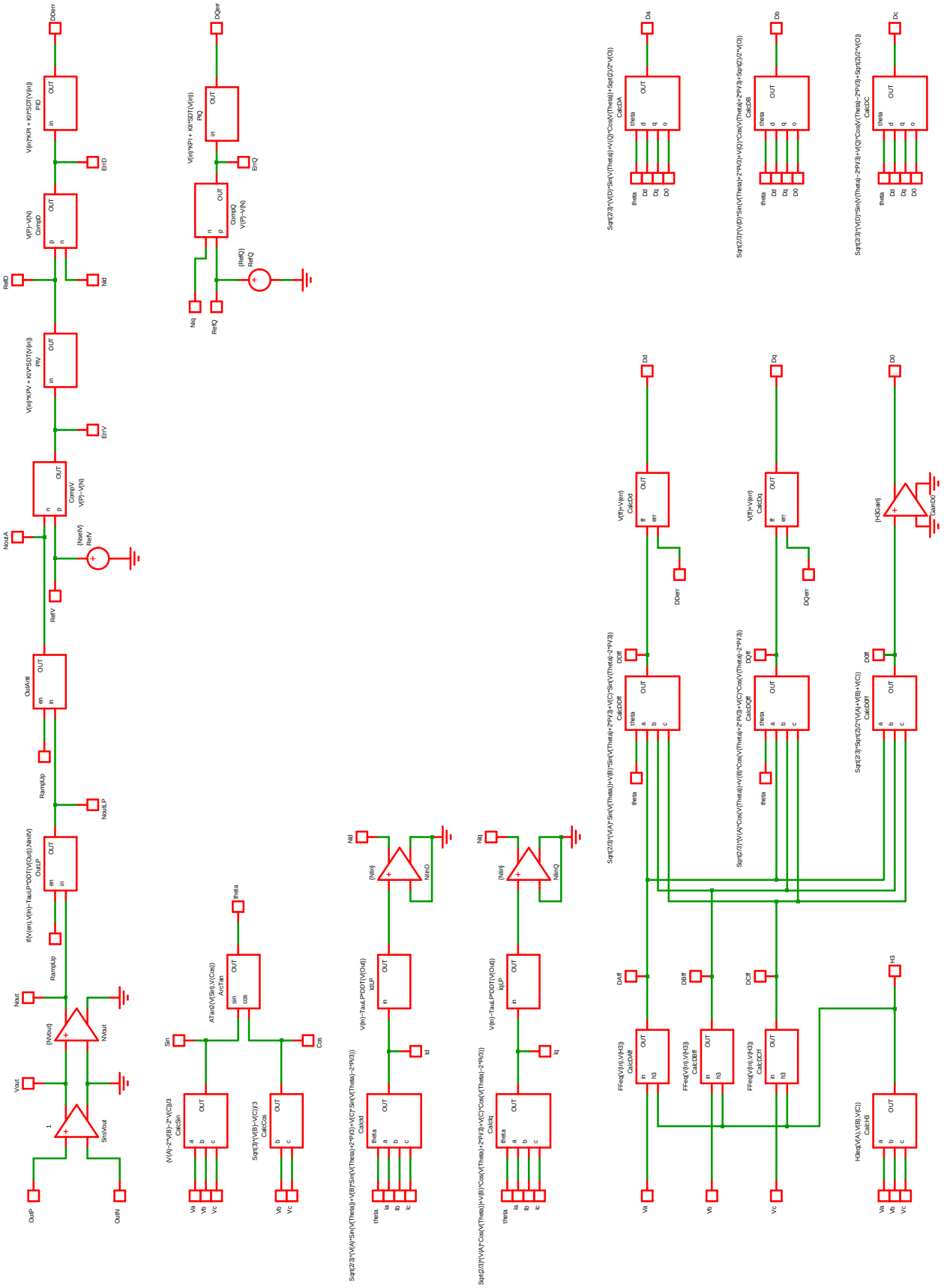


Figure 52. 6−Pack Boost Control SubCircuit

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