RENESAS
BIG IDEAS FOR EVERY SPACE

RENESAS RZ

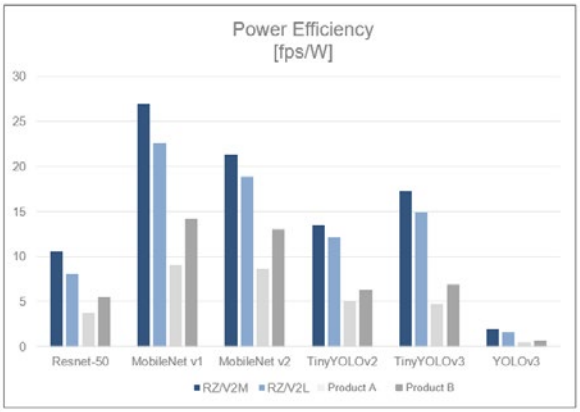
Highly Power-Efficient Embedded AI MPUs for Vision AI

RENESAS RZ/V SERIES

The Renesas RZ/V series of microprocessors (MPUs) for vision AI incorporate Renesas' exclusive DRP-AI dedicated AI accelerator delivering excellent AI inference performance and low power consumption. The RZ/V series consists of two products. The RZ/V2L with simple ISP, 3D graphics engine and highly versatile peripheral functions which is suitable for a wide range of applications. The RZ/V2M features a high-performance image signal processor (ISP) with 4K/30fps support.

Features

- The DRP-AI, dedicated AI inference hardware, utilizes dynamically reconfigurable technology exclusive to Renesas to deliver design flexibility, fast AI processing, and very high power efficiency.
- Combination of hardware (DRP-AI) and software (DRP-AI translator tool) results in high power efficiency.
- DRP-AI translator tool provides the capability to expand to more complex AI models without requiring hardware change.
- Deliver excellent inference performance and power efficiency, irrespective of complexity and size of the AI model (right figure).



Applications

- Security cameras
- POS systems
- Intercom systems
- Smart cameras
- Robot vacuum cleaners
- Smart appliances

Advantages

- No heat sink or cooling fan is needed, enabling reduced product size & BOM costs.
- RZ/V2L enables building of a vision AI system using an inexpensive camera module without an ISP.
- RZ/V2M provides "Tuned ISP" for growing list of sensors to use highest quality images without needing labor intensive ISP parameter tuning.

RZ/V2L Block Diagram

: Features

RZ/V2L Block Diagram

System
- Arm® Debugger (CoreSight)
- Arm® TrustZone®
- 16 × DMAC
- Interrupt Controller
- PLL/SSCG
- Standby (Sleep/Software/Module)

Timers
- 1 × 32bit MTU3
- 8 × 16bit MTU3
- 8 × 32bit PWM
- 3 × WDT

Audio
- 4 × SSI (I²S)
- 1 × SRC

CPU
- Arm® Cortex®-A55 1.2GHz: NEON, VFP; L1 I$: 32KB w/Parity; L1 D$: 32KB w/ECC; L2$: 0KB
- Arm® Cortex®-A55 1.2GHz: NEON, VFP; L1 I$: 32KB w/Parity; L1 D$: 32KB w/ECC; L2$: 0KB
- L3$: 256KB w/ECC
- Arm® Cortex®-M33 200MHz

AI Accelerator
- DRP-AI

Memory
- RAM 128KB w/ECC

Video & Graphics
- 3D GPU Arm® Mali™-G31
- H.264 Enc/Dec 1920 × 1080 @30fps
- Camera In (MIPI-CSI2 4lane, Parallel)
- Display Out (MIPI-DSI 4lane, Parallel)
- Image Scaling Unit

Security (Option)
- Secure Boot
- Device Unique ID
- Crypto Engine
- JTAG Disable
- TRNG
- OTP 4Kbit

Interfaces
- 1 × DDR3L/DDR4-1600 16bit (In line ECC)
- 1 × SPI Multi I/O (8bit DDR)
- 1 × SDHI(UHS-I)/MMC
- 1 × SDHI(UHS-I)
- 1 × USB2.0 Host
- 1 × USB2.0 Host / Function
- 2 × 100/1000Mbps Ether MAC
- 4 × I²C
- 2 × SCI 8/9bit
- 5 × SCIF(UART)
- 3 × RSPI
- 2 × CAN
- GPIO

Analog
- 8 × 12bit ADC

RZ/V2M Block Diagram

: Features

RZ/V2M Block Diagram

System
- JTAG Debug (Coresight)
- 16 × DMAC
- Interrupt Controller
- Power control
- Temperature sensor

Timers
- 32 × Timer
- 16 × PWM
- 2 × WDT

Image Sensor I/F
- MIPI CSI-2 (2 × 4Lanes)

Display I/F
- 1 × HDMI + PHY

Audio I/F
- 1 × I2S

CPU
- Arm® Cortex®-A53: 1GHz: NEON, FPU, L1 I$: 32KB, L1 D$: 32KB
- Arm® Cortex®-A53: 1GHz: NEON, FPU, L1 I$: 32KB, L1 D$: 32KB
- L2$: 512KB

Memories
- 200KB RAM
- 1MB RAM

Sensing and Analyzing
- DRP-AI
- General Processing Accelerator
- Multi-target detection (Face, Person's body)

Video and Graphics
- ISP
- 2D Graphics engine
- H.264/265 Multi Codec
- JPEG Codec

Security
- Security IP

FCBGA: 15 × 15mm², 841-pins, 0.5mm pitch

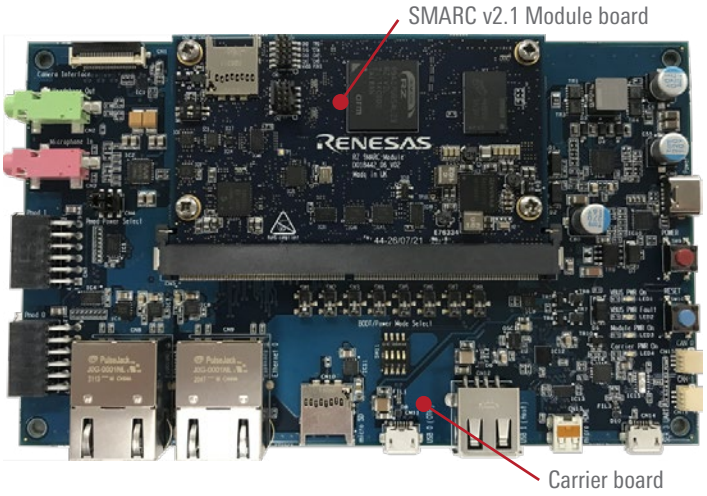
Communication I/F
- 2 × SD
- 1 × PCIe2.0 (1Lane)
- 1 × Gbit Ethernet MAC
- 1 × USB3.1 SuperSpeed (Host/Function)
- 4 × IIC
- 6 × CSI
- 2 × UART
- 1 × Motor Control (for Lens)
- 1 × Environment Sensor I/F
- GPIO

Memory I/F
- 1 × LPDDR4-3200 32-bit
- 1 × eMMC

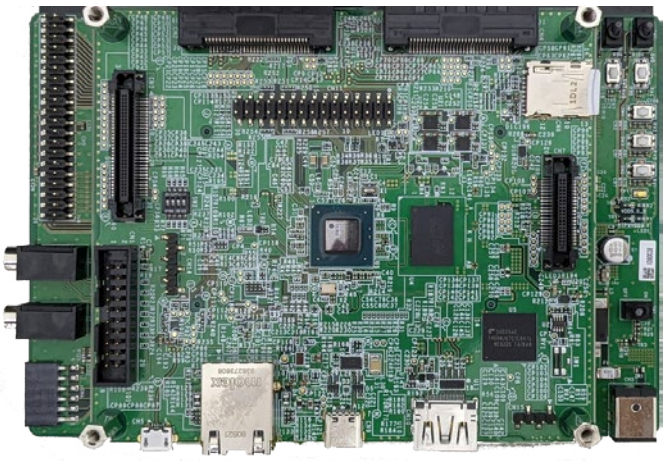
Analog
- 20 × ADC (12-bit)

Note: Refer to the hardware manual of the MPU for usage conditions of each function.

RZ/V2L Evaluation Board Kit (EVK)



RZ/V2M Evaluation Board Kit (EVK)



Ordering Information

Product Group	RZ/V2L		RZ/V2M
Part Number	R9A07G054L24GBG	R9A07G054L23GBG	R9A09G011GBG
AI accelerator	DRP-AI	DRP-AI	DRP-AI
ISP function	Simple ISP by DRP Library	Simple ISP by DRP Library	Tuned ISP by H/W
Main CPU	Cortex-A55 x2	Cortex-A55 x2	Cortex-A53 x2
Sub CPU	Cortex-M33 x1	Cortex-M33 x1	-
Graphics	3D (Arm Mali-G31)	3D (Arm Mali-G31)	2D
Video Codec	H.264	H.264	H.265/H.264 Multi codec
Display Interface	1x MIPI DSI or 1x Digital Parallel output	1x MIPI DSI or 1x Digital Parallel output	1x MIPI DSI
Camera Interface	1x MIPICSI-2 or 1x Digital Parallel input	1x MIPICSI-2 or 1x Digital Parallel input	2x MIPI CSI-2
Gigabit Ethernet	2ch	2ch	1ch
Package	LFBGA	LFBGA	FCBGA
Pin Count	551pin	456pin	841pin
Package Information	21mm x 21mm, 0.8mm pitch	15mm x 15mm, 0.5mm pitch	15mm x 15mm, 0.5mm pitch

■ Visit the following links to learn more about the RZ/V2L and RZ/V2M.
https://www.renesas.com/rzv2l
https://www.renesas.com/rzv2m

■ Visit the following link to learn more about the RZ/V2L Evaluation Kit.
https://www.renesas.com/rzv2l-evaluation-kit

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