Application note

PCB design guidelines for the BlueNRG-LP device

Introduction

The device members of the BlueNRG family are very low power Bluetooth® Low Energy (BLE) devices compliant with Bluetooth specifications.

The BlueNRG-LP is an ultra-low-power Bluetooth low energy (BLE) 2.4 GHz RF transceiver with a Cortex-M0+ microcontroller compliant with Bluetooth specification v5.2. The BlueNRG-LP is suitable to implement applications compliant with Bluetooth Low Energy SIG specifications.

Bluetooth Low Energy technology operates in the same spectrum range (2400 - 2483.5 MHz, ISM band) as classical Bluetooth technology, but uses a different set of channels. Bluetooth Low Energy technology has 40 channels (37 data channels + 3 advertising channels) of 2 MHz band. Two modulation schemes are defined. The mandatory modulation scheme (1 Msym/s) uses a shaped, binary FM to minimize the transceiver complexity. The symbol rate is 1 Msym/s. An optional modulation scheme (2 Msym/s) is similar but uses a symbol rate of 2 Msym/s. The maximum transmit power is 10 mW (10 dBm).

Further details are given in volume 6 part A of the Bluetooth Core specification v5.2.

The BlueNRG-LP device is provided in three different packages:

1. QFN48
2. WLCSP49
3. QFN32

ST provides all necessary source files (reference designs) for users that want to speed up their development.

This application note aims to accompany the reference designs of the application boards and provide detailed information regarding the design decisions adopted within STMicroelectronics designs. In addition, it details the design guidelines to develop a generic radio frequency application using a BlueNRG-LP device.

The RF performance and the critical maximum peak voltage, spurious and harmonic emission, receiver matching strongly depend on the PCB layout as well as the selection of the matching network components.

For the optimal performance, STMicroelectronics recommends the use of the PCB layout design hints described in the following sections. Furthermore, STMicroelectronics strongly suggests to use the BOM defined in the reference design, BOM that guarantees, with a good PCB design, the correct RF performance.

For further information, visit the STMicroelectronics web site www.st.com.

1 Reference schematics

Different application boards have been developed to show the BlueNRG-LP device functionality. The schematics of the different application boards are reported in the following images and refer to the three different packages.

1. QFN48
2. WLCSP49
3. QFN32

All the layout guidelines described in the following sections have to be applied to all these application boards.

Figure 1. BlueNRG-LP QFN48 application board schematic

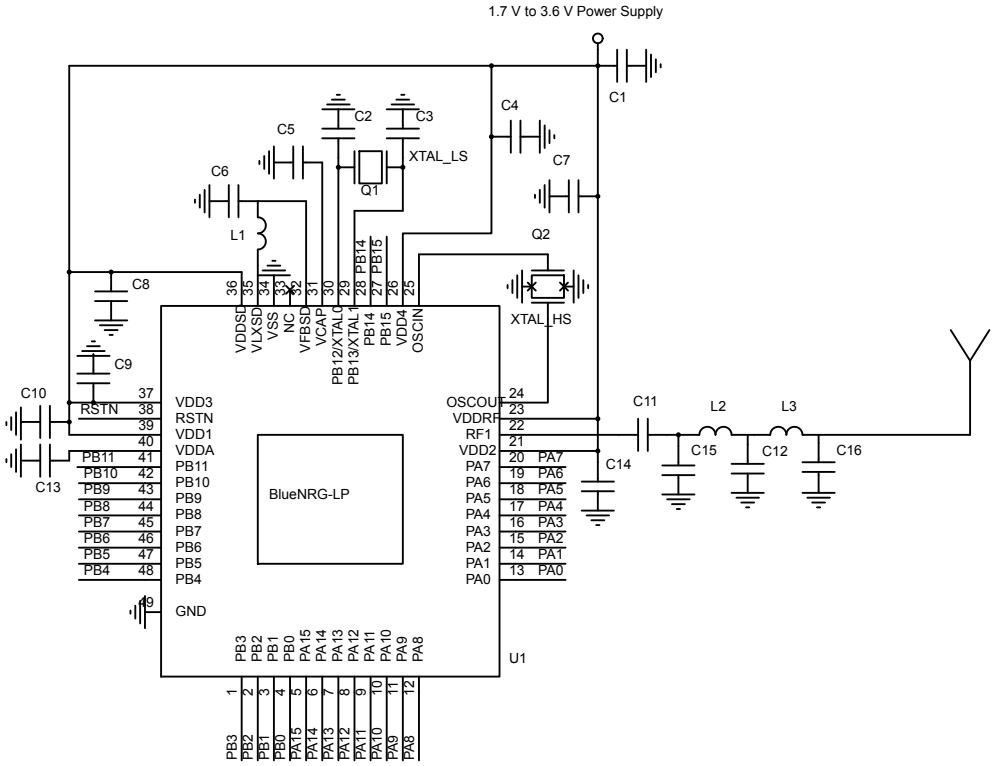


Figure 2. BlueNRG-LP WLCSP49 application board schematic

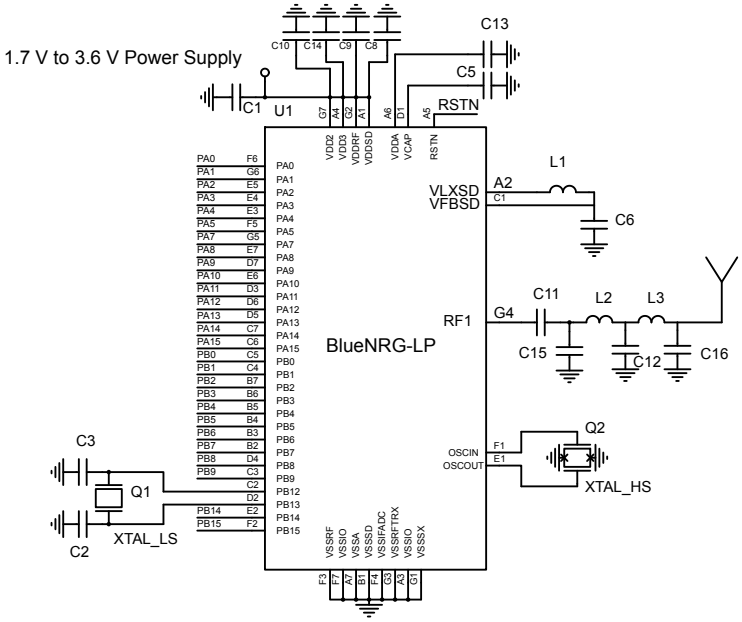


Figure 3. BlueNRG-LP QFN32 application board schematic

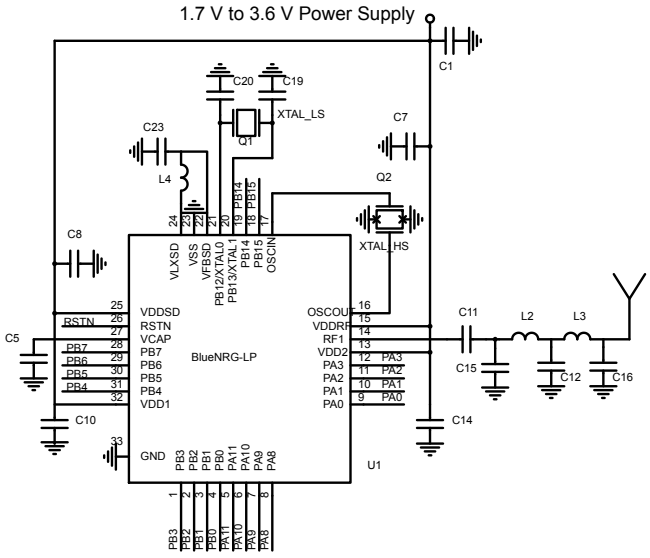


Table 1. The BlueNRG-LP application board external component description

Component	Description
C1	Decoupling capacitor
C2	32 kHz crystal loading capacitor
C3	32 kHz crystal loading capacitor
C4	Decoupling capacitor
C5	Decoupling capacitor for digital regulator
C6	DC-DC converter output capacitor

Component	Description
C7	Decoupling capacitor
C8	Decoupling capacitor
C9	DC-DC converter output inductor
C10	Decoupling capacitor
C11	Decoupling capacitor
C12	RF matching capacitor
C13	Decoupling capacitor
C14	Decoupling capacitor
C15	RF matching capacitor
C16	RF matching capacitor
L1	DC-DC converter output inductor
L2	RF matching inductor
L3	RF matching inductor
Q1	Low speed crystal
Q2	High speed crystal
U1	BlueNRG-LP
U2	Low/band pass filter

2 Two or more layer application board

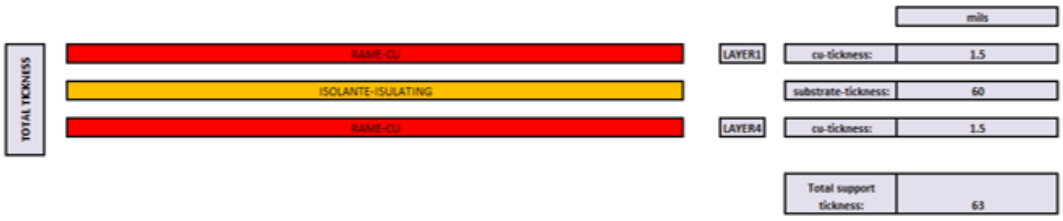
Different approaches can be taken when an application board is designed:

1. Two layer solution
2. More layer solution

2.1 Two layer solution

When it is possible to route all the tracks on two layers and a cheaper solution is requested, a two layer application board can be designed.

Figure 4. Two layer application board stack-up



The suggested thickness of the board is about 63 mils (800 µm).

The two layer board has to be distributed as follows:

1. TOP layer: used for RF signal and routing
2. BOTTOM layer: used for grounding under the RF zones and for routing in the other part

The two layer solution is indicated for the QFN package.

2.2 More layer solution

When it is not possible to route all the tracks on two layers and/or a cheaper solution is not requested, a more layer application board can be designed. This is the case, for example, for the WLCSP package where a four or more layer solution is suggested. See Figure 5. Four layer application board stack-up.

Figure 5. Four layer application board stack-up

The suggested thickness of the board is about 63 mils (800 µm).

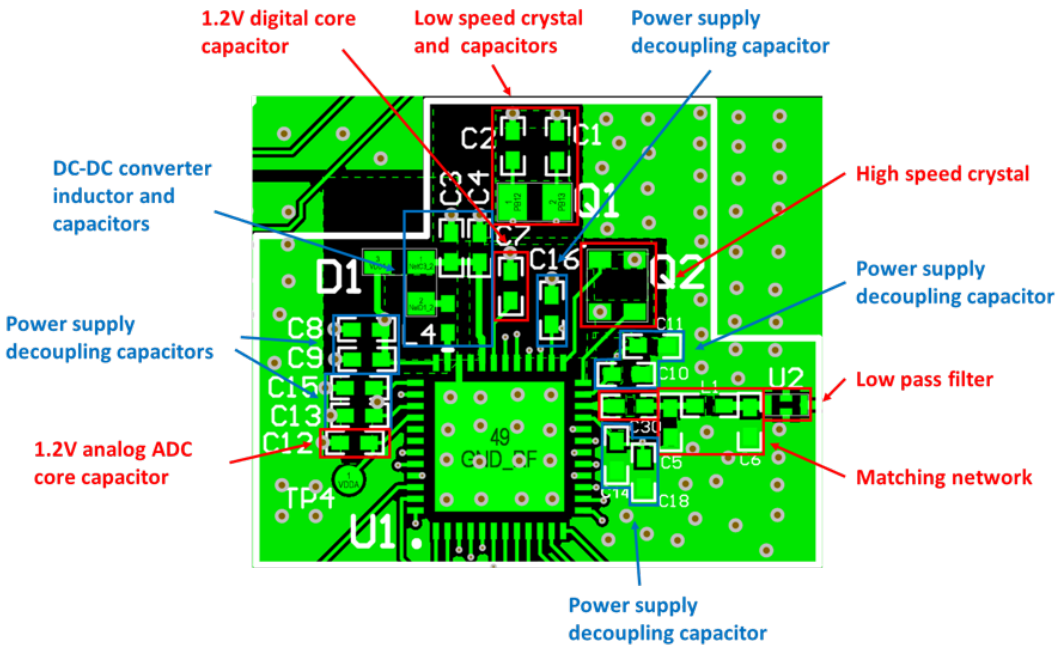
The four/more layer board has to be distributed as follows:

1. TOP layer: used mainly for RF signal and routing
2. GROUND layer: used for grounding under the RF zones
3. INNER and BOTTOM layers: used to route the low frequency tracks

3 QFN package layout recommendations

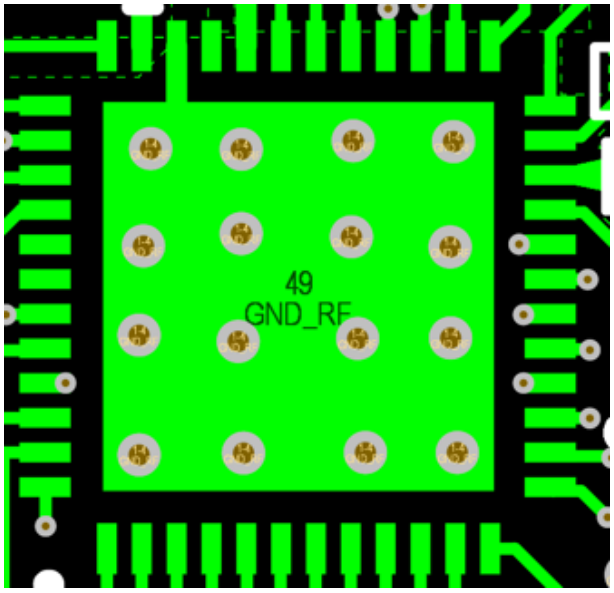
The application board top layer layout using the BlueNRG-LP QFN48 is shown in the Figure 6. BlueNRG-LP QFN48 application board top layer.

Figure 6. BlueNRG-LP QFN48 application board top layer



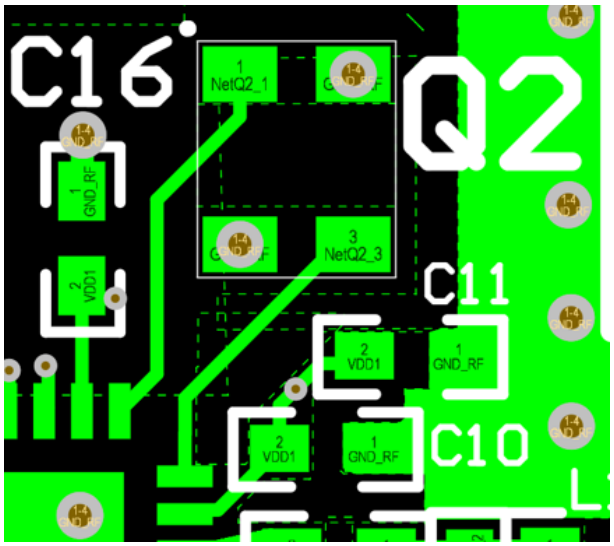
It is very important to connect very well the ground of the exposed pad of the QFN48 and QFN32 to the ground of the application board. Therefore a lot of vias are necessary to be sure that the parasitic inductor introduced from each via is negligible.

Figure 7. QFN48 vias on the exposed pad



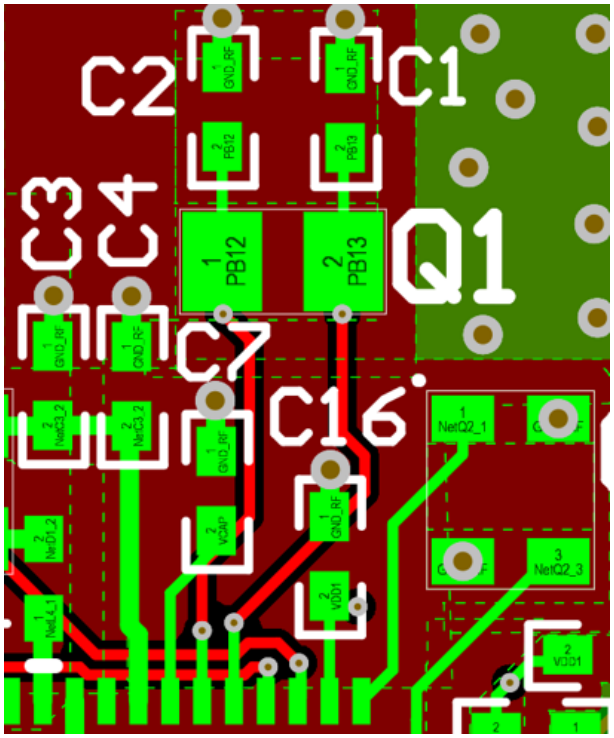
The high speed crystal (Q2) is connected directly to the BlueNRG-LP without external load capacitors. Two loading capacitors are tunable through a 6-bit word. This is mainly in order to enable fine XTAL frequency tuning. This tuning network is made by a fixed capacitor + 6 binary weighted switchable ones. The effective range of loading capacitors are programmable through an internal register. The programmable register and the capacitor range are reported in the BlueNRG-LP datasheet.

Figure 8. QFN48 high speed crystal zone



The low speed crystal is connected directly to the BlueNRG-LP with external load capacitors. The tracks that connect the low speed crystal to the BlueNRG-LP are put in a lower layer, the bottom layer, to reduce the coupling with the RF signal.

Figure 9. QFN48 low speed crystal zone



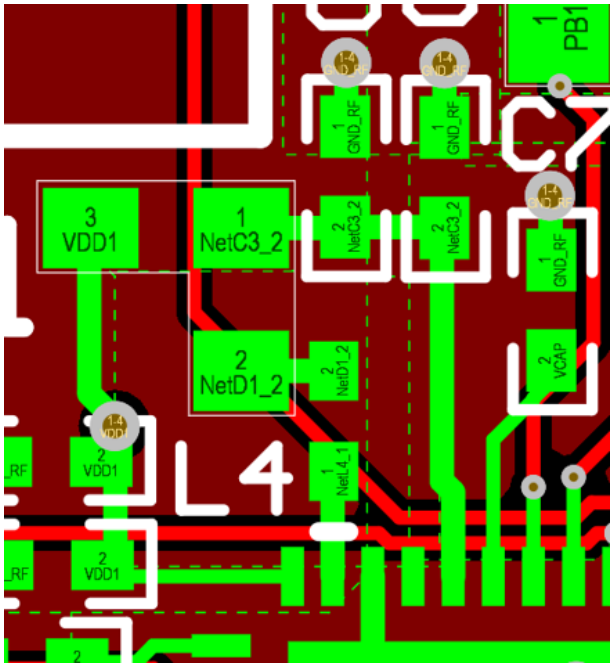
The DC-DC converter area is very sensitive and it is necessary to pay attention on the layout of this part. This is because the DC-DC converter generates ground noise that can get coupled on surrounding ground reducing the sensitivity and high frequency components that can be coupled onto the RF part.

So to ensure a correct layout it is necessary:

1. To provide efficient filtering by placing capacitors as close as possible from the BlueNRG-LP
2. To reduce parasitic ensuring wide and short connections to BlueNRG-LP

In Figure 10. QFN48 DC-DC converter layout zone the suggested layout is shown:

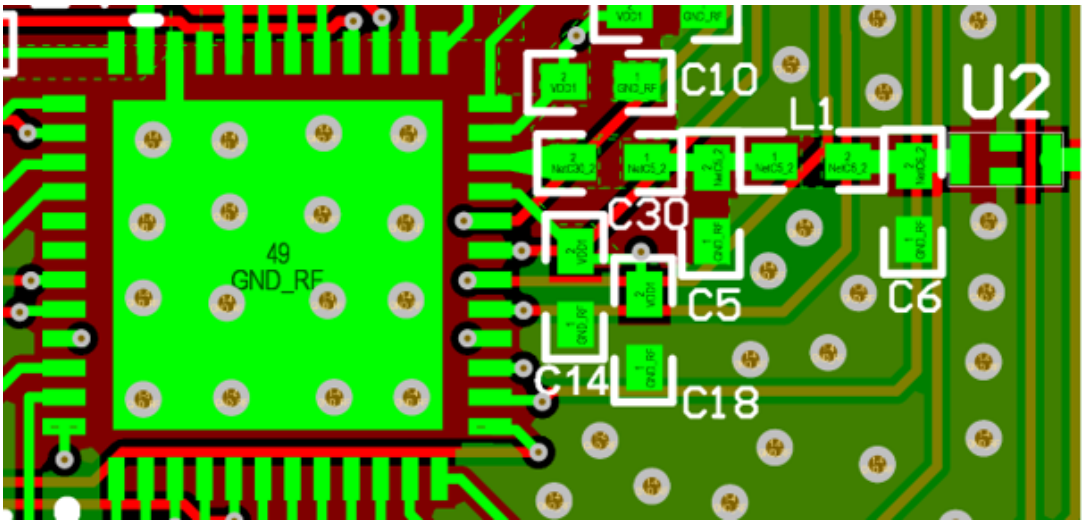
Figure 10. QFN48 DC-DC converter layout zone



Special care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering placing these capacitors as close as possible from their dedicated pins on the BlueNRG-LP.

The TX/RX part of the BlueNRG-LP is very sensitive. A differential to single ended device is integrated into the BlueNRG-LP so no external balun resulting in a BOM reduction. A Π matching network is foreseen on the application board if a 50 ohm matching activity is necessary. After the Π matching network an LPF is used to cut the harmonics of the PA in TX mode.

Figure 11. **QFN48 RF layout zone**

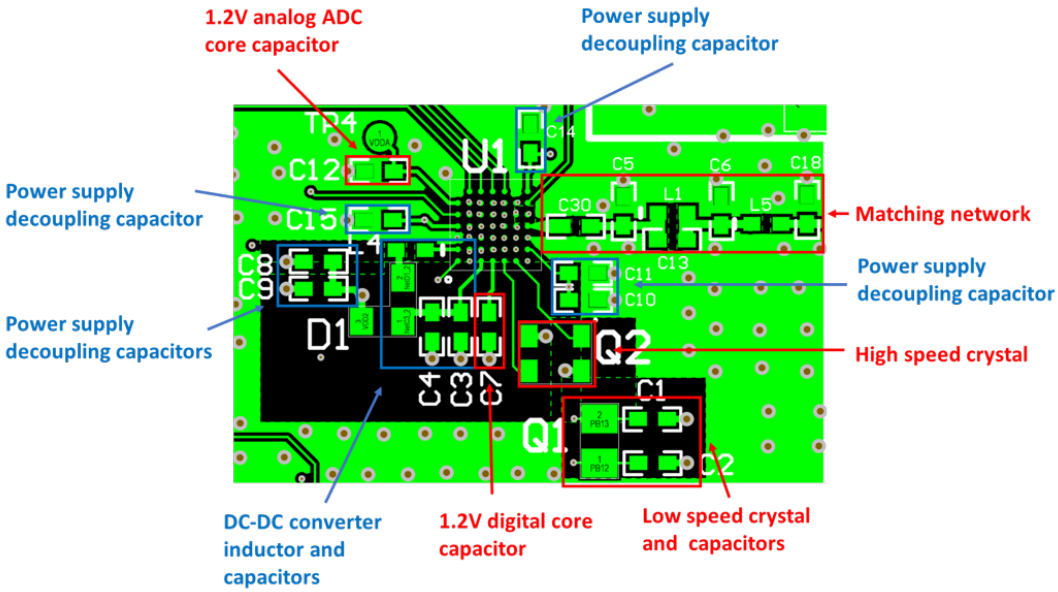


4 CSP package layout recommendations

The layout of CSP package is more complex than that of a QFN. A technology that uses laser via is typically used to access the internal pads of the device. Laser technology is more expensive than the one that does not use blind as well, so a solution that uses a copper capped via has been used to access the internal pads of the CSP package.

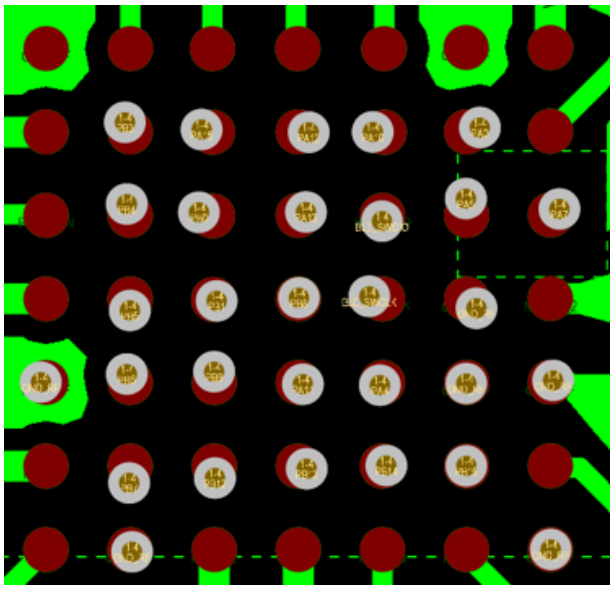
The application board top layer layout using the BlueNRG-LP is shown in Figure 12. BlueNRG-LP CSP49 application board top layer .

Figure 12. BlueNRG-LP CSP49 application board top layer



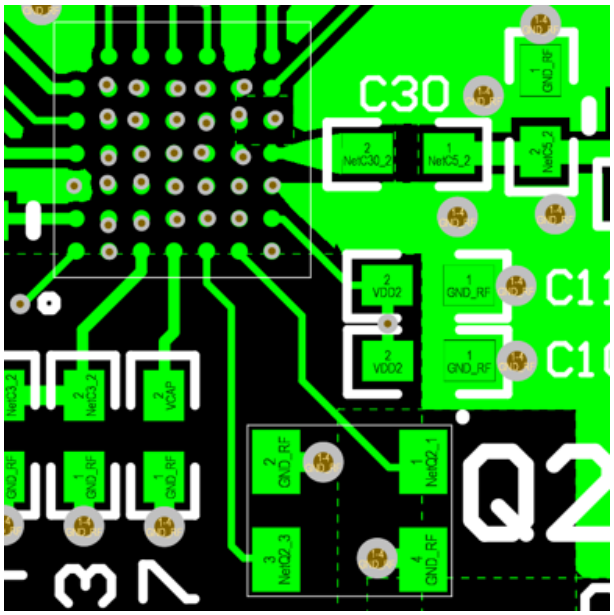
As for the QFN package, it is very important to connect very well the ground of the CSP49 to the ground of the application board. The ground pads are connected to ground with a via directly on the pad itself. Where possible the connection to the ground of the TOP layer has been made.

Figure 13. CSP49 package footprint



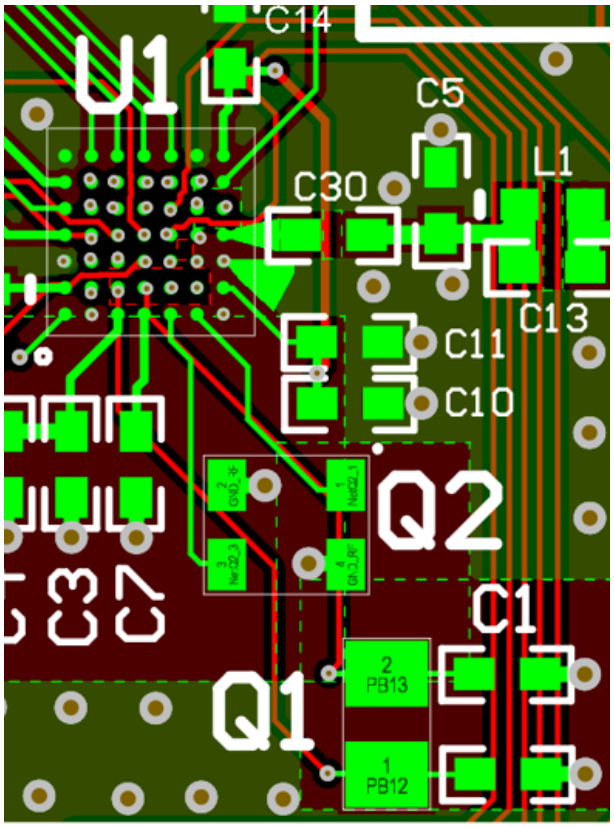
The QFN package high speed crystal (Q2) is connected directly to the BlueNRG-LP without external load capacitors. Two loading capacitors are tunable through a 6-bit word. This is mainly in order to enable fine XTAL frequency tuning. This tuning network is made by a fixed capacitor + 6 binary weighted switchable ones. The effective range of loading capacitors are programmable through an internal register. The programmable register and the capacitor range are reported in the BlueNRG-LP datasheet.

Figure 14. CSP49 high speed crystal zone



The low speed crystal is connected directly to the BlueNRG-LP with external load capacitors. The tracks that connect the low speed crystal to the BlueNRG-LP are put in a lower layer, the bottom layer, to reduce the coupling with the RF part.

Figure 15. **CSP49 low speed crystal zone**



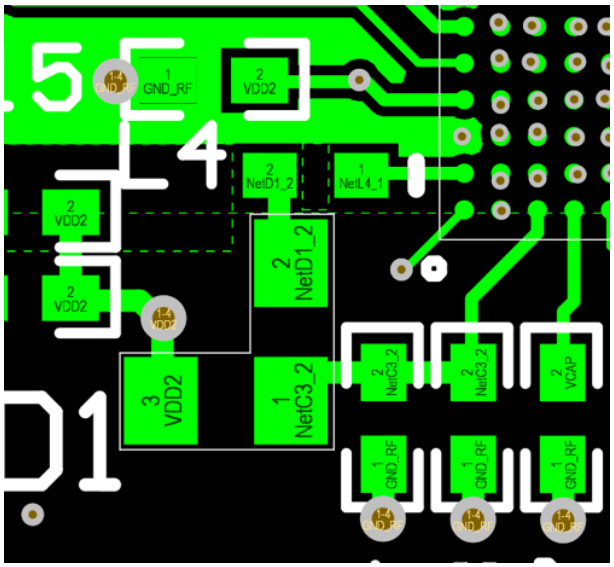
The DC-DC converter area is very sensitive and it is necessary to pay attention to the layout of this part. This is because the DC-DC converter generates ground noise that can get coupled on a surrounding ground reducing the sensitivity and high frequency components that can be coupled onto RF part.

So to ensure a correct layout it is necessary:

1. To provide efficient filtering by placing capacitors as close as possible to the BlueNRG-LP
2. To reduce parasitic ensuring wide and short connections to the BlueNRG-LP

In Figure 16. CSP49 DC-DC converter zone the suggested layout is shown.

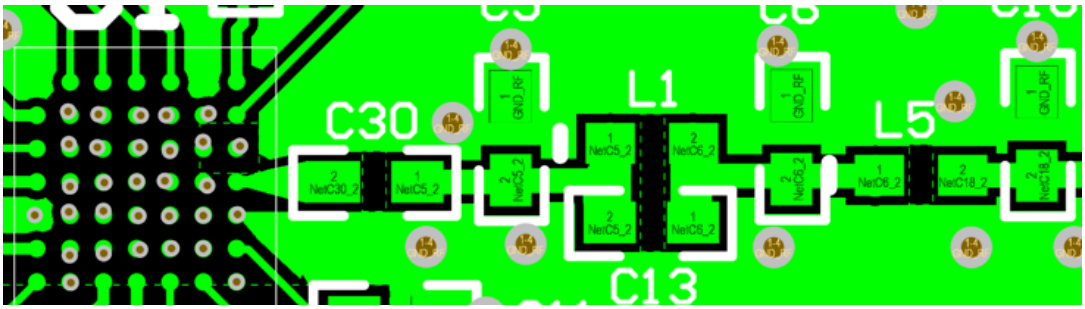
Figure 16. **CSP49 DC-DC converter zone**



Special care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering placing these capacitors as close as possible to their dedicated pins on the BlueNRG-LP.

The TX/RX part of the BlueNRG-LP is very sensitive. A differential to single-ended device is integrated into the BlueNRG-LP so no external balun resulting in a BOM reduction. A complex discrete filtering network is foreseen on the application board to filter the harmonics when the PA is on.

Figure 17. **CSP49 discrete filtering network**



5 Reference

[1] BlueNRG-LP Datasheet

Revision history

Table 2. **Document revision history**

Date	Version	Changes
24-Jul-2020	1	Initial release.
15-Sep-2020	2	Updated Section Introduction.

Contents

List of figures