# PIC64HX Series PIC64HX1000 Family



## Summary

The PIC64HX1000 family represents a new class of high-performance multicore 64-bit microprocessors (MPUs) for aerospace and defense, industrial, automotive, medical and communications applications. The unique architecture provides comprehensive Ethernet networking, advanced Artificial Intelligence and Machine Learning (AI/ML) processing, and connectivity support while delivering unprecedented flexibility, fault tolerance, scalability and power efficiency. The PIC64HX family includes specific devices targeted at industrial, aviation and military applications.

PIC64HX is designed for mission-critical applications that demand:

- High-performance edge computing with AI/ML
- Spatial and temporal partitioning
- Time-Sensitive Networking (TSN) Ethernet connectivity and switching
- Defense-grade security including post-quantum cryptography
- Superb fault tolerance and reliability for mission-critical and autonomous systems

A complete package of tools, libraries, drivers and boot firmware is available to unlock the full capabilities of PIC64HX while accelerating your time to market. Multiple open source, commercial and real-time operating systems are supported including Linux<sup>®</sup> and RTEMS, as well as hypervisors such as Xen. PIC64HX leverages and builds upon Microchip's Mi-V ecosystem for RISC-V<sup>®</sup>.

## Application Compute Complex With Real-Time Support

The PIC64HX1000 family provides multicore 64-bit RISC-V processing. Highlights of the Application Compute Complex include:

- Eight 64-bit RISC-V CPU cores (SiFive Intelligence<sup>™</sup> X280) with vector extensions
- Up to 1 GHz operation
- Optional Dual-Core Lockstep (DCLS)
- Multiple operating modes: Unified, Split and Cache-Isolated
- Enhanced support for real-time applications
- Decoupled vector pipeline supporting 512-bit vector lengths that enable AI/ML
- Support for virtualization and both Type 1 and Type 2 hypervisor usage (MMU and IOMMU with two-stage translation)
- 26K DMIPS or (a CoreMark<sup>®</sup> score of 46K) for scalar performance and up to 2 TOPS (int8) or 1 TFLOPS (bfloat16) for vector matrix multiplication (all eight cores)

## WorldGuard End-to-End Partitioning Architecture

WorldGuard provides hardware-based spatial partitioning of the entire device including core, cache, interconnect, peripherals and memory with support for up to 32 domains. WorldGuard facilitates integration and isolation of mixedcriticality workloads.

### Integrated System Controller

The onboard system controller is an additional 64-bit RISC-V CPU core (SiFive S7) operating at 500 MHz. The system controller enables mission-critical and autonomous systems with runtime monitoring and fault management. Attached to the system controller are the following dedicated and shared peripherals:

- One SPI/QSPI
- One I<sup>2</sup>C, one UART and 32 GPIO (shared)





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## **TSN Ethernet Switch**

The PIC64HX1000 family integrates 240 Gbps of Ethernet switching with full TSN support aligned to P802.1DP (aerospace profile) and IEEE / IEC 60802 (industrial profile):

- Up to 160 Gbps of switching from up to 16 external facing ports
- Up to 80 Gbps of Direct Memory Access (DMA) for packet insertion and extraction from internal subsystems, including the Application Compute Complex
- 16 external-facing ports for Ethernet rates from 10M to 10G
- Remote Direct Memory Access (RDMA) with RDMA over Converged Ethernet (RoCEv2) for low-latency transfers from remote sensors and extensibility

#### **Memory Interfaces**

- Two DDR interfaces supporting up to DDR4-3200
- 72-bit interface with ECC for single-bit error correction
- Up to 32 GB per DDR interface
- Optional support for encrypted DDR transfers of instructions to maximize platform and IP security

#### Nonvolatile Memory and SRAM

- e-MMC<sup>™</sup> and SD<sup>™</sup>
- Parallel NAND Flash, NOR Flash and SRAM
- NAND and NOR SPI Flash
- MRAM with SPI or parallel interface

## **Co-Processor/Accelerator Interfaces**

- Up to two PCle<sup>®</sup> Gen 3 ×8 ports or four PCle Gen 3 ×4 ports through bifurcation
- Support Compute Express Link<sup>®</sup> (CXL<sup>®</sup>) 2.0 (at eight GT/s) host operation for cache-coherent interconnect to CXL Type 2 devices such as FPGAs, GPUs or coprocessors

## Peripheral Interfaces

- Up to four TSN Ethernet endpoint ports supporting rates from 10M to 10G
- Up to two USB 2.0/3.0
- Two SPI, four UART, four I<sup>2</sup>C, 64 GPIO, two MDIO, JTAG host, timers and watchdogs

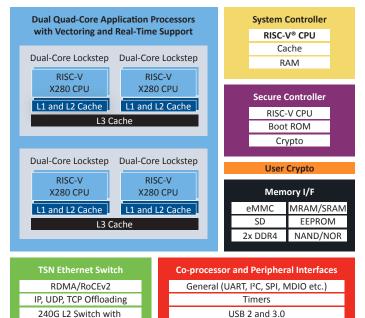
## Defense-in-Depth Security

L3 Forwarding

16-ports (10M up to 10 GbE)

- Cryptographically controlled supply chain and device manufacturing flow that ensures authenticity
- Dedicated secure enclave to support secure boot and platform root of trust
- Post-quantum cryptography: ML-KEM and ML-DSA
- User/application-level security acceleration
- Extensive anti-tamper detection and response capabilities

# PIC64HX1000 Family Block Diagram



## **Product Table**

	PIC64HX1000 - IN	PIC64HX1000 - AV	PIC64HX1000 - MI
Application	Industrial	Aviation	Military
Package	45 mm × 45 mm Plastic, 1932 balls		
Qualification	JEDEC	AEC-Q100	AEC-Q100
Neutron Report	Not Applicable	Planned, on demand	Planned, on demand
Operating Temperature	–40°C (T <sub>A</sub> ) to +105°C (T <sub>I</sub> )	–40°C (T <sub>A</sub> ) to +125°C (T <sub>I</sub> )	–55°C (T <sub>A</sub> ) to +125°C (T <sub>I</sub> )

Contact Microchip for the fully qualified part number.

**Міскоснір** 

4x TSN Ethernet (10M up to 10 GbE)

PCIe<sup>®</sup> Gen 3; Optional CXL<sup>®</sup> 2.0