White Paper
10-2018

Reliability and qualification of CoolGaN™

Technology and devices

Abstract

Infineon's CoolGaN™ gallium nitride on silicon (GaN-on-Si) HEMTs (high electron mobility transistors) represent a dramatic improvement in power conversion switching device figure of merit (FOM) with outstanding system performance enabling higher efficiency, power density and reduced system cost.

But, as with any new technology, it is of critical importance that a thorough technology development and product qualification procedure is followed in order to assure reliable operation that meets design lifetime and quality requirements in power conversion systems. GaN device materials and device designs are very different from their silicon counterparts. These differences are substantial enough as to warrant analyzing how they will be used in application and determining what new changes must be introduced to the development and reliability qualification processes.

This paper describes the comprehensive four-part process that Infineon has used to successfully qualify CoolGaN™ 600 V technology and products. Key failure mechanisms are described, and the means to ensure safe and reliable operation in a wide variety of applications are provided.

Through this approach, many risks our customer would otherwise encounter are avoided and a safe path to use CoolGaN™ technology is provided. This publication also holds tutorial value to engineers with an interest to better understand semiconductor reliability concepts generally.

By
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1 Background: why can't we use silicon qualification processes on GaN technology?

1.1 50 years of silicon experience

Silicon semiconductor device failure modes and reliability have been active topics of research and development for over 50 years. Iteration after iteration, generation after silicon generation, relevant failure modes such as time dependent dielectric breakdown (TDDB) and humidity driven corrosion have been discovered, solved, and sometimes revisited and solved again as materials and device development pushed towards physical limits in service of Moore's law.

1.2 Silicon failure mechanisms

The models/equations shown in Table 1 have proven to be useful in predicting failure of silicon devices under targeted application conditions. They include time dependent dielectric breakdown (TDDB) such as occurs in silicon device gate oxide, fatigue behavior, electromigration due to high current density in conductors, and corrosion such as occurs due to humidity and bias. Though many or most of these also apply to GaN devices, this cannot be considered as a sufficient list for consideration to qualify GaN devices.

Table 1 List of silicon material/device failure mechanisms [1] and models developed over 50 years to describe its behavior

Failure mechanism		TF model
Electromigration		$TF = A_o J^{-N} Exp(Q/K_BT)$
Stress migration		$TF = A_o (T_O-T)^{-N} Exp(Q/K_BT)$
Corrosion		$TF = A_o (\%RH)^{-N} Exp(Q/K_BT)$
Time dependent dielectric breakdown (TDDB)	E model	$TF = A_o Exp(-\gamma E_{ox}) Exp(Q/K_BT)$
	1/E model	$TF = A_o Exp(G/E_{ox}) Exp(Q/K_BT)$
Fatigue		$TF = A_o (\Delta T-T_o)^{-N}$
Surface inversion/mobile ions		$TF = A_o J_{ion}^{-1} Exp(Q/K_BT)$
Hot carrier injection		$TF = A_o (I_{sub} / W)^{-N} Exp(Q/K_BT)$

1.3 Silicon qualification standards

Based on knowledge of silicon device failure mechanisms, qualification procedures such as the one shown in Table 2 have been published by JEDEC (Joint Electron Device Engineering Council) and other institutes (e.g., automotive qualification standard Q101 from the Automotive Electronics Council). These procedures define tests, stresses, durations and sample sizes used to qualify silicon power semiconductor products. The choice of qualification test stresses and conditions is often based on the underlying knowledge and models of silicon device failure mechanisms. Although JEDEC qualification is

the industry standard still there are more sufficient ways to qualify GaN power semiconductor devices to assure reliable operation in real applications. In the next sections we will discuss these in detail.

Table 2 A typical list of test used in JEDEC [2] qualification for silicon technology and devices

Stress	Conditions	Duration	Sample size
Temperature cycling JESD22 A104	With PC -55 °C / +150 °C	1000x	3 lots x 77 pieces
High temperature reverse bias JESD22 A-108	With PC 150 °C / 600 V	1000 h	3 lots x 77 pieces
High temperature storage live JESD22 A-103	With PC 150 °C	1000 h	3 lots x 45 pieces
Positive high temperature gate stress JESD22 A-108	With PC 150 °C / 50 mA	1000 h	3 lots x 77 pieces
Negative high temperature gate stress JESD22 A-108	With PC 150 °C / -10 V	1000 h	3 lots x 77 pieces
High humidity temperature reverse bias JESD22 A-101	With PC 85 °C / 85 % r.h. / 100 V	1000 h	3 lots x 77 pieces
Intermittent operational life test MIL-STD 750/Meth. 1037	With PC ΔT = 100 K	15,000x	3 lots x 77 pieces
ESD-HBM JS-001	Without PC	-	1 lot x 3 pieces per voltage level
ESD-CDM JS-002	Without PC	-	1 lot x 3 pieces per voltage level

1.4 The need for new qualification concept for GaN devices

The need of a different qualification approach is rooted in differences in structures between silicon and GaN devices. A cross section of a typical CoolMOS™ Superjunction (SJ) silicon power transistor is shown in Figure 1. The source, gate and drain contacts are identified. In normal operation, during “on” condition a sufficiently high voltage is applied across the gate dielectric (2) which causes inversion of the channel conductivity from p to n type and the electrons flow from source to drain in the vertical direction (as shown by the red line and arrow).

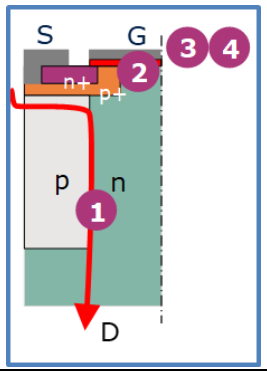

Figure 1 Cross section of unit cell of typical Superjunction power transistor such as CoolMOS™

The numbers identify key device features and correspond to the stress tests typically applied during device qualification.

(1) The p-n body diode (and the not shown edge of die termination structure) is stressed during high temperature reverse bias (HTRB) testing.
(2) Gate oxide dielectric ruggedness is tested during high temperature gate bias (HTGB) testing.
(3) Device passivation, and mold compound are stressed during temperature, humidity and bias testing (THB).
(4) Top aluminum and wire bonds are stressed during temperature cycling.

Compared to their vertically built silicon counterparts GaN HEMTs have a lateral device structure (see Figure 2).

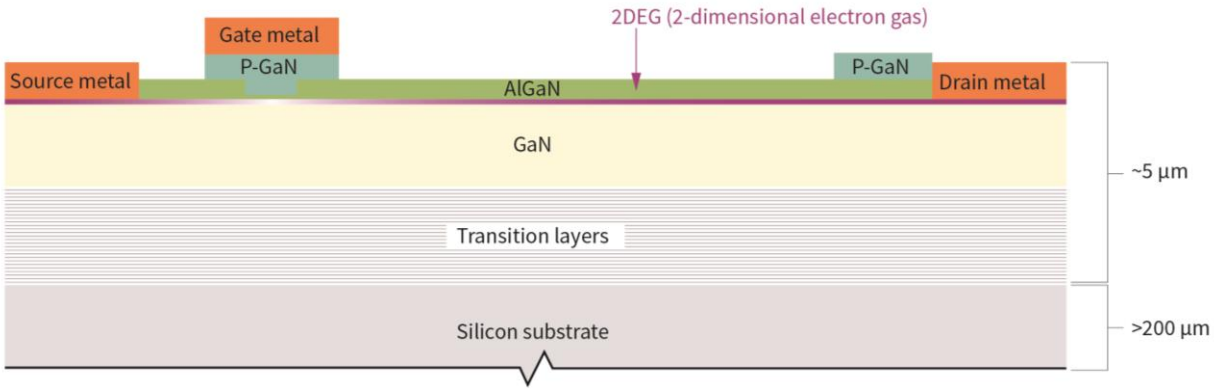

Figure 2 Schematic cross section of a GaN HEMT showing lateral current flow and three surface terminals (silicon substrate is referenced to source)

The source, gate and drain contacts are all on the surface (though the device backside is held at source potential). During “on” condition electrons flow from source to drain but, different from the SJ MOSFET, it flows laterally between the source and drain terminals on the surface. The device operation physics are also very different. In a GaN HEMT the material system creates a thin, high density layer of electrons known as a two-dimensional electron gas (2DEG) between AlGaN and GaN layers (as shown in Figure 2). The 2DEG layer is interrupted by thinning the AlGaN beneath the gate which prevents 2DEG

formation resulting in normally-off operation. Application of a sufficiently high positive gate to source voltage applies a vertical field which causes the 2DEG to reform beneath the gate thus completing a conduction layer of 2DEG for “on” operation. Different from SJ MOSFETs, there is no p-n drain to source junction or an oxide dielectric material in the gate structure of a CoolGaN™ HEMT. The drain to source field terminates laterally and at many places across the surface of the GaN HEMT device which increases the risk of possible occurrence of humidity induced corrosion compared to the SJ MOSFET which only terminates source to drain potential along the device perimeter.

All these differences between silicon and GaN device structures and material systems must be considered when setting the qualification plan for a GaN HEMT.

2 A proposed four-part method for qualifying GaN devices

As already explained above, silicon power device qualification standards are insufficient for qualifying GaN devices. A comprehensive and effective qualification plan includes elements that focus on device specific differences between GaN and silicon parts. The starting point is to understand the stresses applied in the intended application, as well as considering the planned useful life and quality while ensuring device robustness. On this topic Infineon has been the industry leader [3] that developed and follows a four-part path to qualify its GaN devices (see Figure 3).

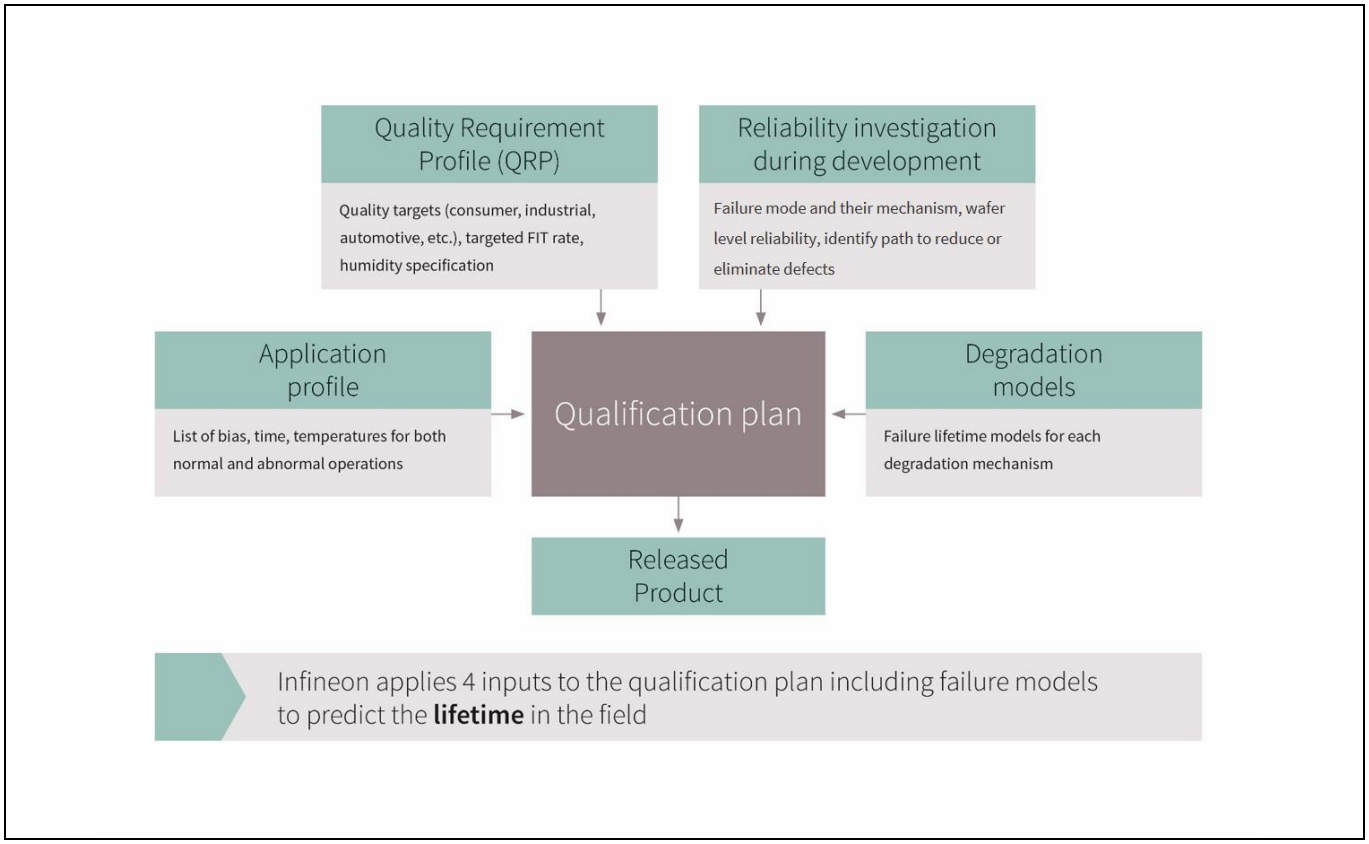

Figure 3 Infineon's comprehensive four-part qualification plan for its CoolGaN™ devices

2.1 Application profile

The first of the four qualification elements is the application profile. Assuring reliable operation of GaN HEMTs to the planned quality level and lifetime requires close cooperation between our customers and Infineon. It all starts with describing the stresses from which a device can suffer during operation in a specific topology. A complete application profile also lists all relevant system level requirements such as output power profile versus time, time at various temperatures and at different relative humidity, and hard or soft switching for a partial list [4]. Resultant stresses on the devices are described in great detail. For instructive purposes in this paper we will describe one typical application profile, a telecom rectifier (AC-DC) power converter.

Table 3 High level summary of an Application profile for a telecom AC-DC power converter

Telecom rectifier AC-DC socket	
Key device parameters, topology	2.5 kW, 230 V line, CCM hard-switching
Expected lifetime	15 years
Operating lifetime	100 %
Environmental conditions	
Relative humidity	85 %
Profile of ambient temperature (in the box) -% of operating time at each temperature	15 % @ -27.5 ˚C 60 % @ 15 ˚C 25 % @ 72.5 ˚C
Profile of Load conditions % of operating time at each load condition	5 % standby, no load 40 % @ 10-30 % load 50 % @ 30-80 % load 5 % @ 80-100 % load
Device electrical conditions	
Drain source voltage (V_{ds})	Average during off = 400 V Peak depends on I_{LOAD} (max = 460 V)
I_{GS+}	Average = 15 mA Peak = 625 mA for 50 ns
V_{GS}	Average = -3 V Peak = -10 V for 10ns
I_D	Load current average 50% duty-cycle
PWM frequency	65 kHz

Telecom rectifier (AC-DC) sockets have fairly stressful operating conditions. Such systems are required to operate for long duration in the field with ambient temperatures varying on a large scale and humidity that can reach quite high levels. This application represents a good use case for GaN device qualification as operating conditions can reach extreme levels. This qualification approach can apply to similar applications (e.g., server, TV power supply) with the same power conversion topologies and less restrictive conditions. Table 3 provides a high level summary of a 2.5 kW telecom rectifier system and the related stresses seen by the power transistors in the PFC section. Three temperature regimes are required to simulate a four-season operation. Four load conditions are described from standby to 80-100% load to cover all possible output conditions of the system. As some device reliability factors are temperature and/or load dependent, it is important to include these in the application profile.

The next table from the application profile (Figure 4) provides another level of detail to the operating conditions including startup conditions, frequency of switching, and single switch cycle timing of turn on and turn off (including duration of the L x di/dt induced voltage spike). For completeness, the temperature and load profile information is repeated. The heart of the application profile is a table wherein the device stress modes (in particular voltage and current) are detailed as a function of temperature and humidity.

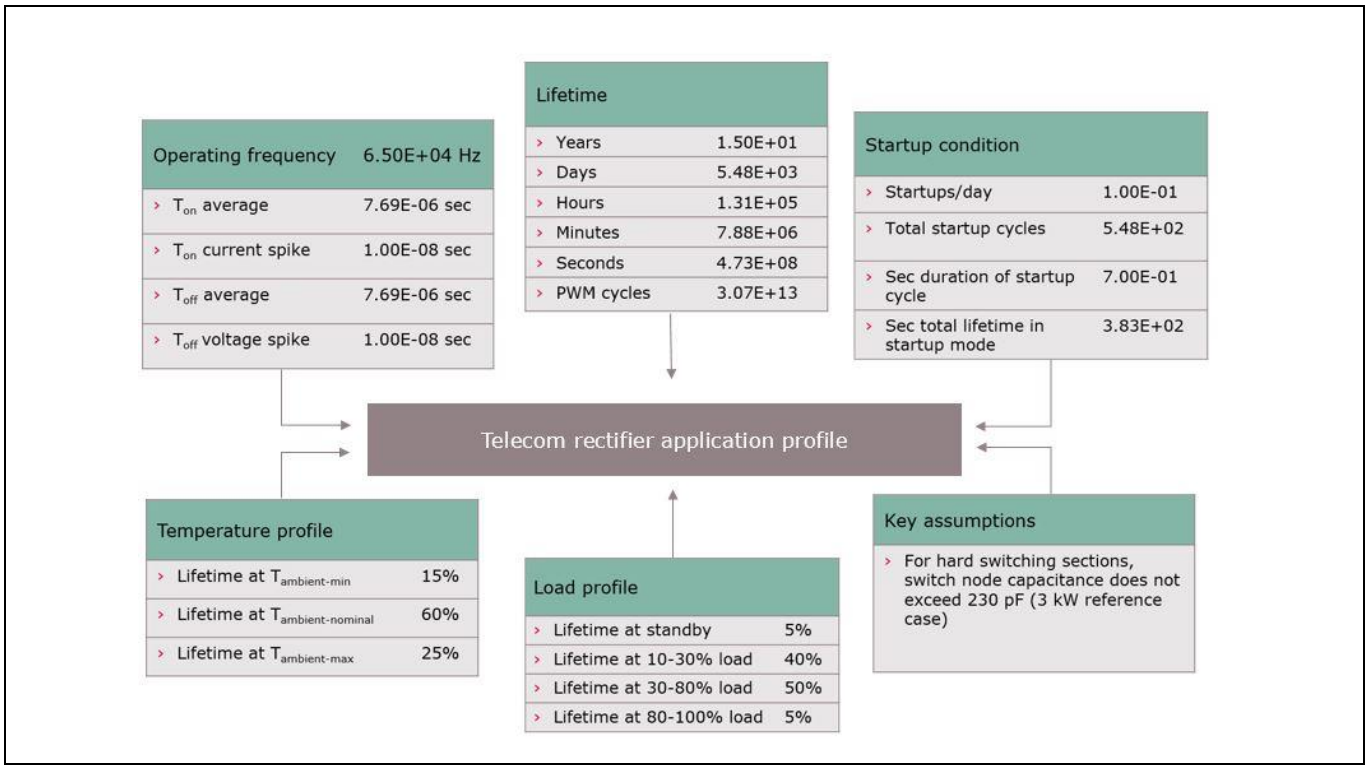

Figure 4 Telecom rectifier application profile, first table of operating conditions

An example is shown in Table 4. In this table only the lowest temperature condition is shown (the information for the other ambient temperature operating conditions such as 25 ˚C and 72 ˚C are not included for clarity of this exposition however are also required for a complete reliability analysis). The corresponding time at each load condition is provided, as well as for each load condition the average and peak voltage (during off state) and current (during on state) are described[1].

[1] *This information will be used for later reliability modeling of the effects of time under DC bias and for switching safe operating area (SOA) lifetime.*

Table 4 Application profile of a telecom AC-DC power converter

Ambient temperature	$R_{DS(on)}$	Load condition	On/off state [average/peak]	Total time duration in this condition [h]	Off: V_{DS} [V]	Off: V_{GS} [V]	On: V_{DS} [V]	On: I_G [mA]	On: I_{load}	P_{tot} [W]
-27.5	0.05	Standby	On state average	4.93E+02			0.05	15	1	0.0
			On state peak	6.41E-01			0.075	625	1.5	0.1
			Off state average	4.93E+02	400	-3.0				0.0
			Off state peak	6.41E-01	410	-10.0				0.0
		10-30%	On state average	3.94E+03			0.2	15	4	0.4
			On state peak	5.12E+00			0.3	625	6	0.9
			Off state average	3.94E+03	400	-3.0				0.0
			Off state peak	5.12E+00	420	-10.0				0.0
		30-80%	On state average	4.93E+03			0.5	15	10	2.5
			On state peak	6.41E+00			0.7	625	14	4.9
			Off state average	4.93E+03	400	-3.0				0.0
			Off state peak	6.41E+00	440	-10.0				0.0
		80-100%	On state average	4.93E+02			0.6	15	12	3.6
			On state peak	6.41E-01			0.9	625	18	8.1
			Off state average	4.93E+02	400	-3.0				0.0
			Off state peak	6.41E-01	460	-10.0				0.0

The peak turn off voltage increases for the higher load conditions as is observed in application. As we will see later, the DC bias failure model depends quite strongly on voltage. If, under application conditions, there are substantial differences in the spike or average voltage (V_{DS}) applied to the device then it is important to capture this as well in the application profile.

2.2 Quality requirements profile

In the second element of qualification we create the quality requirements profile. We collect a general description of the application, customer target lifetime (that can vary on a large scale depending on the application), maximum allowed cumulative failure rate, definition of parametric drift limits to the required electrostatic discharge (ESD) rating, operating humidity requirements, and moisture sensitivity level (MSL) rating.
For the subject telecom rectifier market we have required a 15 year lifetime with a failure rate of 1 FIT (that equals to 1 failure per billion device-hours).

2.3 Reliability investigations during development

During the development of Infineon‘s CoolGaN™ devices, we have completed a thorough reliability investigation of GaN specific failure modes. We have segregated these failure modes into two categories: intrinsic failures (those due to inherent wear out of device structure and materials) and extrinsic failures (those due to defectivity or very high process variability). During technology

development a path must be found to reduced defectivity and process variation in order to eliminate extrinsic failures.

Early reliability investigations use tools such as a Weibull plot. This takes time to failure data and graphs the fraction of a failed sample (y axis) versus time under stress (x axis). For an illustrative and arbitrary applied stress, the Weibull plot in the left image in Figure 5 shows failure in time data (time is shown on a logarithmic scale) where a fraction of the devices failed early in time (circled group) and another fraction failed much later. Each data point represents the time at which a single device failure occurred (x axis) and the cumulative fraction of the population failing before that device (y axis). The subset of early failing parts indicates a different failure mechanism (or mechanisms), typically due to either defectivity or wide process variation or a combination of both. We refer to these early failures as extrinsic since their source is external to the real capabilities of the design and materials.

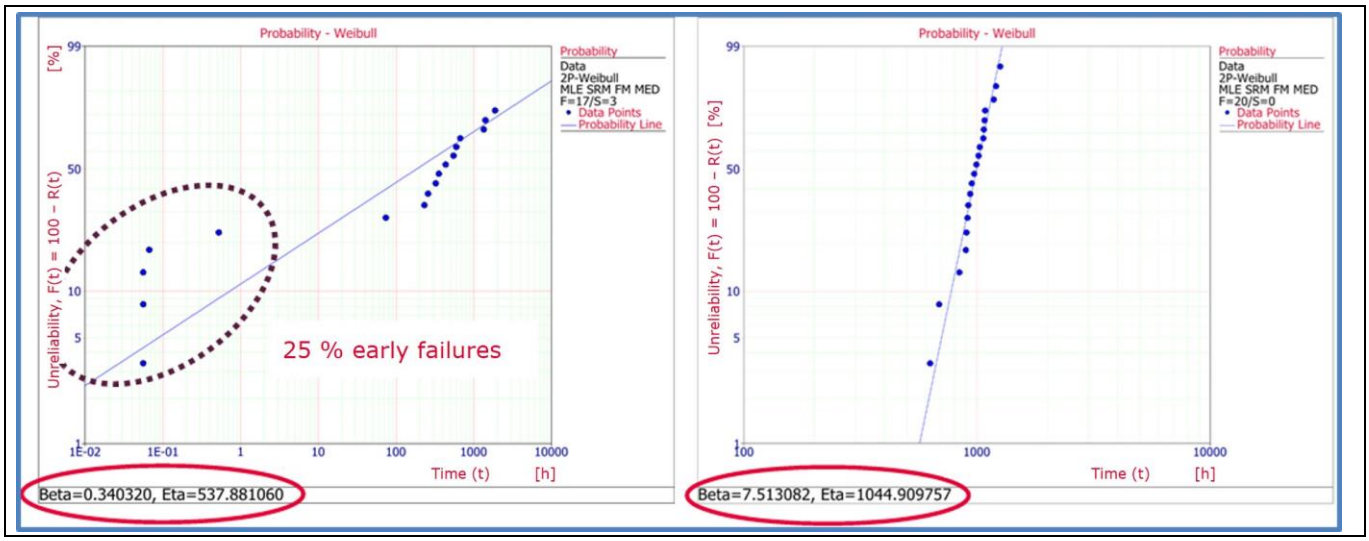

Figure 5 The Weibull plot shows individual failures versus (logarithmic) time, helping to identify and isolate devices which fail early due to defectivity/high process variation

On the left graph in Figure 5, the circled group of parts failed very early in time. These are the so called extrinsic failures. The second part of the population of parts fail after a much longer time under stress. These devices fail at the wear out limits of the material and device design. These failures are referred to as intrinsic since they fail in a predictable manner at the physical limits of the intended device design and materials.
The right graph of Figure 5 shows data from a population which appears to include only intrinsic failures. These devices fail very uniformly and later in time compared to the extrinsic failures identified on the left graph. These devices live longer, behave and fail more uniformly (this is indicated in a higher slope and the points falling along a well-defined line). The failures in this case are considered to be intrinsic caused typically by material wear out.

The goal of the reliability investigations is to discover the intrinsic and extrinsic failure mechanisms for each relevant stress, and to find a path of process/design/test changes. These changes will greatly reduce the occurrence of extrinsics. Then, with intrinsics now dominating the distribution, a degradation model can be generated to predict lifetime and failure rate.

2.4 Degradation models

The fourth dimension of qualification is composed of degradation models for key failure modes of GaN devices. These allow predicting failure rates under stated stress conditions and lifetimes. To better understand such models we will review some first principles of reliability statistics and build upon the notion and role of the Weibull plot that was just introduced.

2.4.1 The reliability bathtub curve

A well-accepted notion is the reliability bathtub curve. Such a curve shows the instantaneous failure rate over the lifetime of any system or component, and typically identifies three failure regimes: the early life (or infant mortality), the random (or constant), and the wear out failure rate regions. The blue curve in Figure 6 is the observed failure rate (equals to the sum of all three failure rate regions mentioned previously) which has a bath tub shape. Referring back to the Weibull plot in section 2.3 (see Figure 5), the initially high early life (or infant mortality) failure rate is due to extrinsic failure mechanisms such as defectivity and process variation which cause premature failure. The constant failure rate is due to random destructive events such as cosmic rays. For the use of GaN devices in terrestrial applications we note that this failure rate is low enough to not to consider it. The wear out failure rate occurs when the inherent limits of the design and material system reach destructive limits. In silicon power FETs this can include gate oxide failure due to well-understood time dependent dielectric breakdown. Other relevant wear out mechanisms (common in silicon and GaN devices) include die attach solder and wire bond fatigue, and moisture/humidity induced corrosion. Later in this document, we will examine important failure modes that are specific to GaN devices.

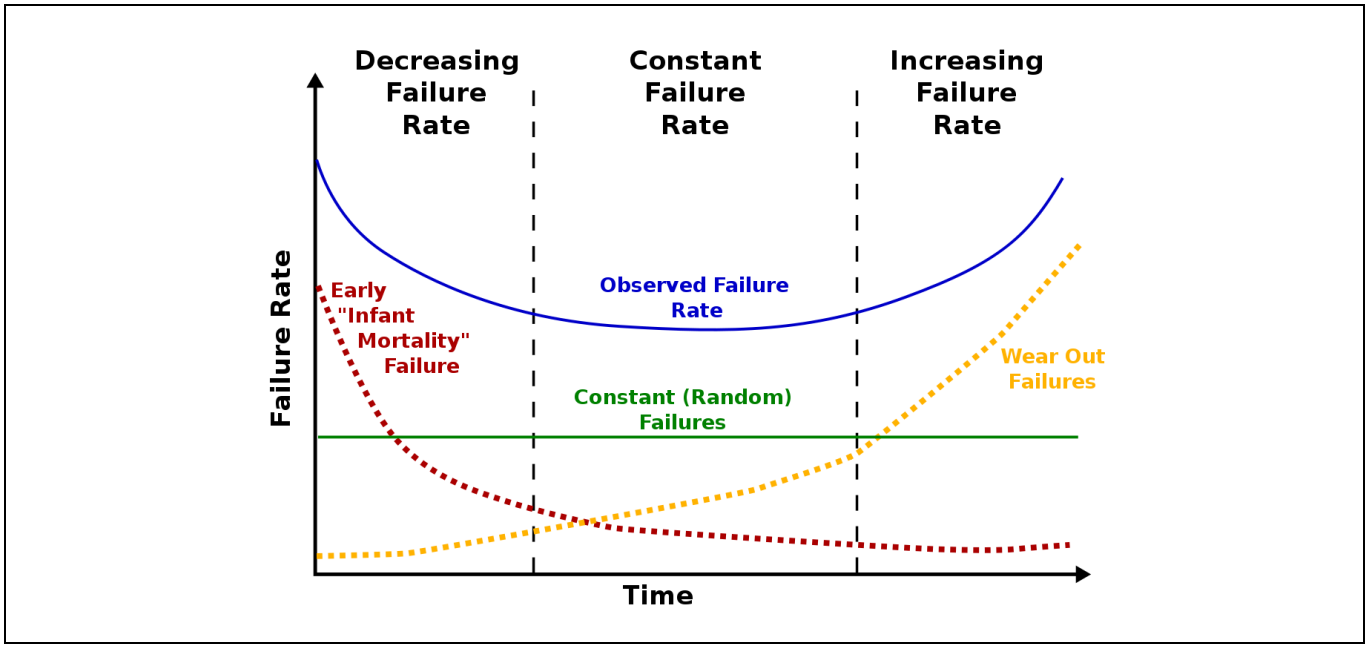

Figure 6 The reliability bathtub curve shows early (purple), constant (green) and wear out (yellow) failure regimes, and the net failure rate that is sum of the three (blue)

2.4.2 The Weibull function and plot

We return now and expand upon the discussion of the Weibull plot from section 2.3. The plot assumes failure data can be fit to a very flexible and useful fitting function known as the Weibull cumulative density function which describes the cumulative failure rate:

$$F(t) = 1 - e^{-(\frac{(t-\gamma)}{(\eta)})^{\beta}}$$ Equation 1

This expression for cumulative failure rate can be used to model all three regions of the bath tub curve (separate constants β and η and γ apply for each case). For early failure regime, β will have a value less than 1, while for the wear out regime β >1 (as stated previously, we ignore the constant failure rate regime). On the Weibull plot (left graph in Figure 5) the slope (β) is 0.34, indicating presence of extrinsic/early life failures. The slope (β) in the right side graph in Figure 5 is 7.5, consistent with wear out /intrinsic failures. To restate: during development, devices are stressed to failure and failure modes are studied and parsed into extrinsic (early life) and intrinsic (wear out) and a path is defined to reduce the occurrence and /or influence of extrinsic failures. This path can be a combination of changes in design, process, material or screening stress tests. When the primary failures are due to intrinsics then a wear out model can be developed.

2.4.3 Wear out model example

Once the extrinsic failures are reduced, a formula /model can be chosen to describe the failure of the intrinsics.

For an illustrative example, see the plot in Figure 7.

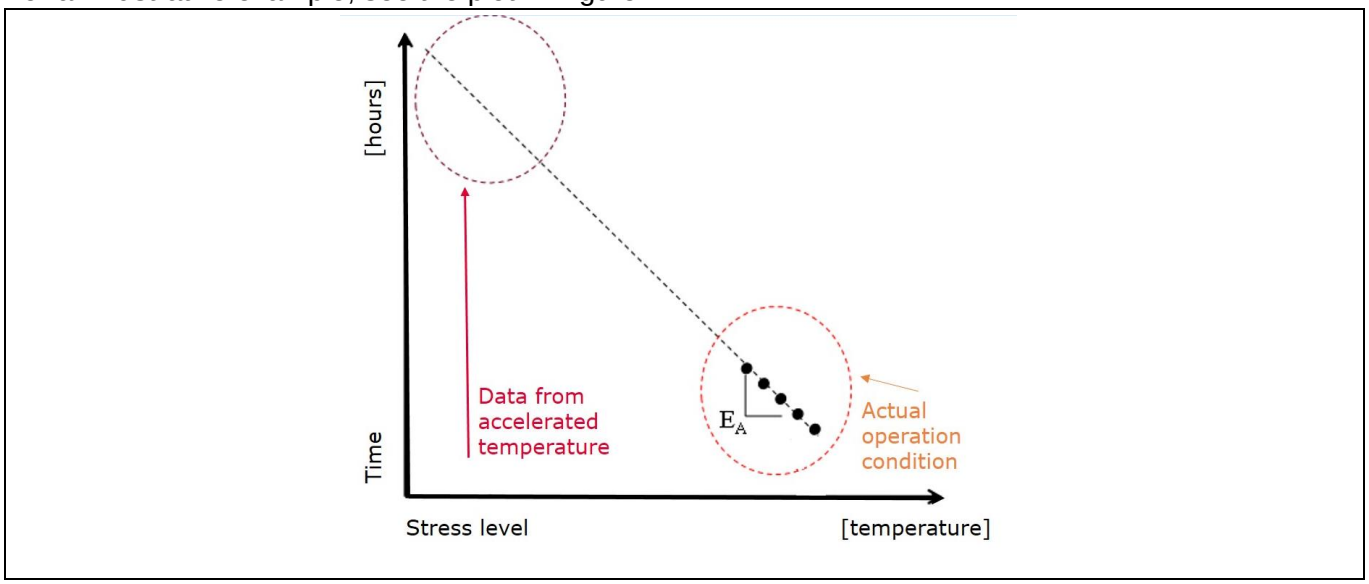

Figure 7 Plot of accelerated test to failure data consistent with the Arrhenius equation

Each data point shown in this figure is the average of a population tested to failure under accelerated temperature conditions (so there are five different temperatures in this example). In this case, with axes

in a logarithmic scale, as temperature is increased the time to failure is reduced. This behavior is seen in many physical systems. In fact, silicon device gate oxides fail in this manner which can be described by the Arrhenius equation as follows:

$$AF(T) = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)} \qquad \text{Equation 2}$$

The characteristic activation energy (E_a) can be extracted from the slope of the plot as shown. The constant k is the familiar Boltzmann's constant. Taking one of the data points in the plot as a reference (with related temperature T_{stress} and its reference time to failure value)and a different specified use temperature (T_{use}), we can calculate an acceleration factor (AF) which can be multiplied with the reference time to failure value to calculate the average time to failure at the use temperature.
The Arrhenius equation is often used to describe the failure behavior of silicon device gate oxides under temperature and bias stress. In some instances, it is also applicable to GaN failure modes. Different failure mechanisms call for different solutions and hence equations, as discussed later in this paper.

3 Key failure mechanisms and degradation models for GaN devices (different from silicon)

During the development process of our CoolGaN™ HEMTs, we learned a lot about different failure mechanisms for GaN devices. In this section we will discuss several of the most important ones that stand out, especially because they do not occur in silicon power FETs.

3.1 DC bias failure mode

The first one to examine is DC bias lifetime. That might seem surprising since silicon devices are also prone to DC bias failure; for that reason high temperature reverse bias (HTRB) testing is performed.

With respect to failure modes under DC bias the difference between silicon and GaN HEMT devices is that GaN HEMT's - when tested at accelerated voltage and temperature conditions - exhibit a failure rate that depends strongly on voltage. Let's start first with typical response of a GaN HEMT to drain to source voltage (V_{DS}) stress. In Figure 8 a cross section of a test device rated at 200 V is shown on the left, while on the right the related I, V_{DS} trace for the off state is shown. The measurements were stopped at breakdown. There are two relevant conduction regimes: an early conduction period (labeled as 1st conduction mechanism) which is generally nondestructive, and a regime which occurs at higher voltage (labeled as 2nd conduction mechanism). This 2nd conduction mechanism regime has a much steeper slope than the first one and will lead to device destruction at sufficiently high voltage. As will further be explained, this behavior is similar to what is observed for metal oxide semiconductor (MOS) material stacks that are commonly used in silicon power MOSFET gate structures.

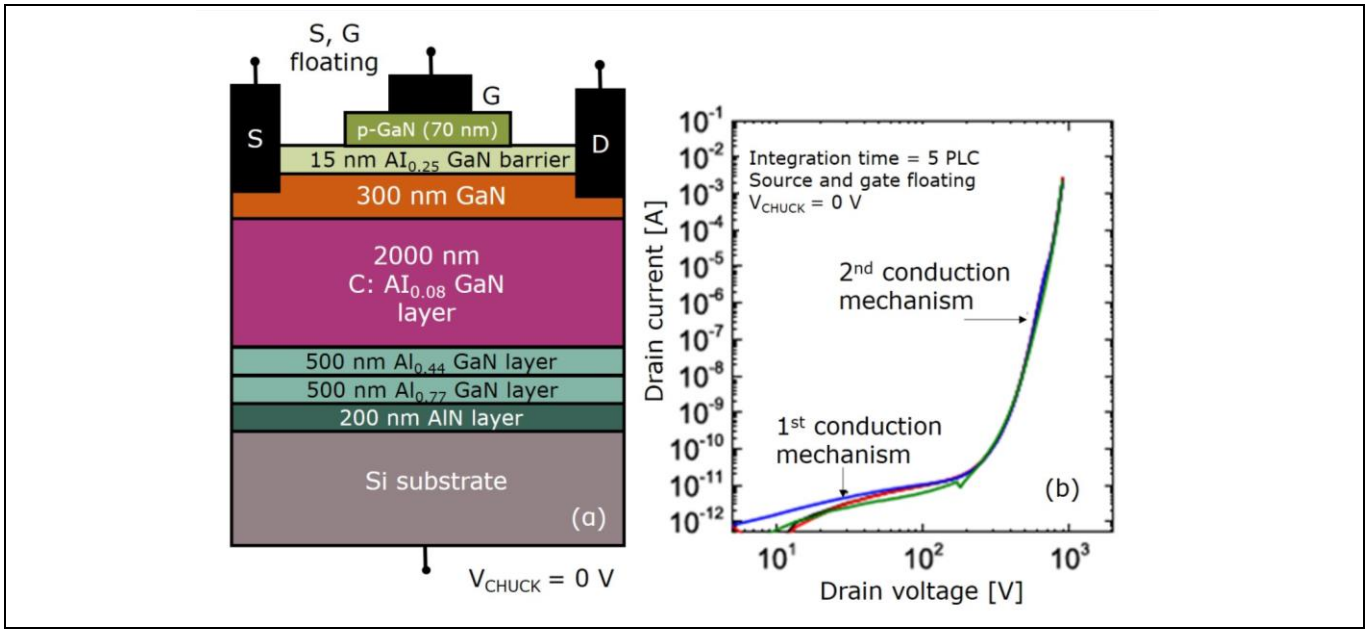

Figure 8 Schematic representation of the device under test and drain controlled vertical leakage current measurement [5]

Figure 9 shows the drain current response as drain voltage is ramped in 20 V steps and held for 120 seconds at each step.

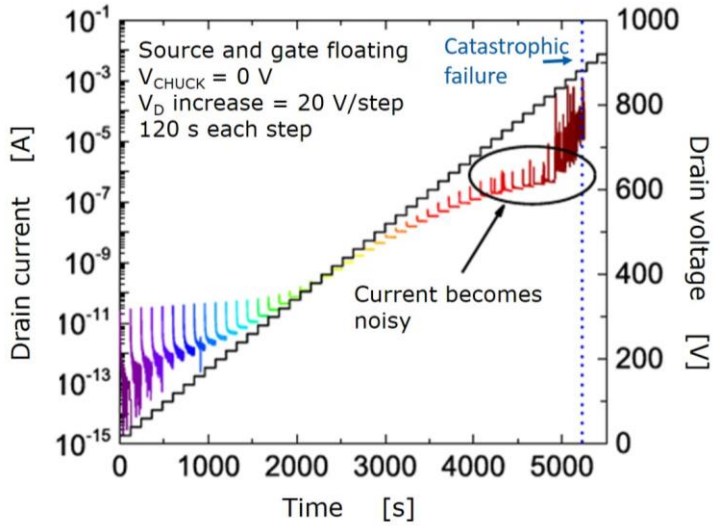

Figure 9 Drain current monitored using the step stress (V_{CHUCK} = 0 V, V_D increases in 20 V steps) [5]

As drain voltage is ramped, the drain current increases in mini step bursts. These bursts become more and more frequent and larger in magnitude (so called noisy) just before the devices fails. This behavior is similar to what is observed in silicon dioxide based MOS structures as gate materials degrade due to time dependent dielectric breakdown (TDDB). This is not surprising as the chemical bonds for both silicon oxides and gallium nitride are covalent but highly polar in nature (see Figure 10). When subjected to an electric field, the polar molecules lead to asymmetrical lattice distortion straining their chemical bonds which will break over time. The electronegativity of the Si-Si bond is zero so although SiO_2 structures (including MOS device gates) are subject to TDDB failure, Si-Si structures such as p-n junctions are not. So although TDDB occurs during reverse bias on GaN devices and not for silicon FETs, silicon devices do show TDDB with respect to their gate structure when SiO_2 or other polar molecules are used as insulating material.

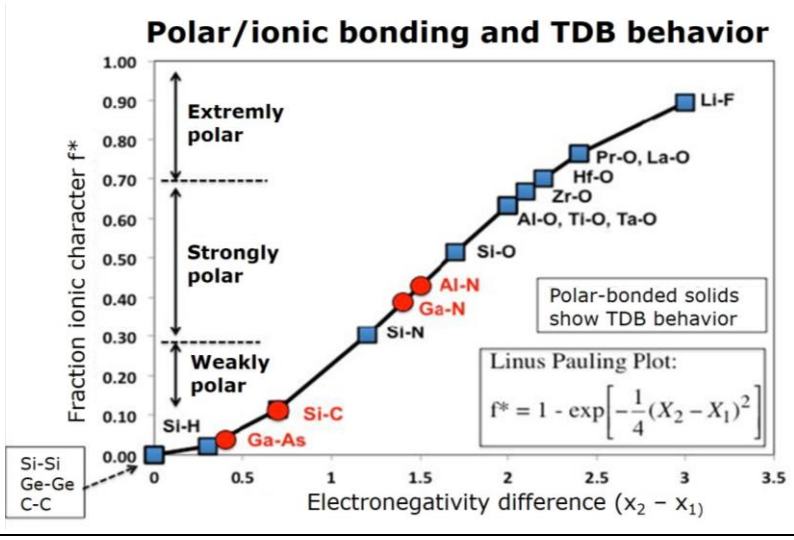

Figure 10 Electronegativity of bonds between element pairs [1]

3.2 DC bias degradation model: Weibull plots for matrix of voltage and temperature

Returning now to the Weibull plot concept introduced in section 2.3, Figure 11 displays accelerated stress time to failure data with DC bias and temperature stress applied to samples of Infineon's 190 mΩ CoolGaN™ 600 V e-mode HEMTs. A simulated application condition of 480 V and 125 ˚C is considered with target of 15 year lifetime and failure rate of 1 FIT.

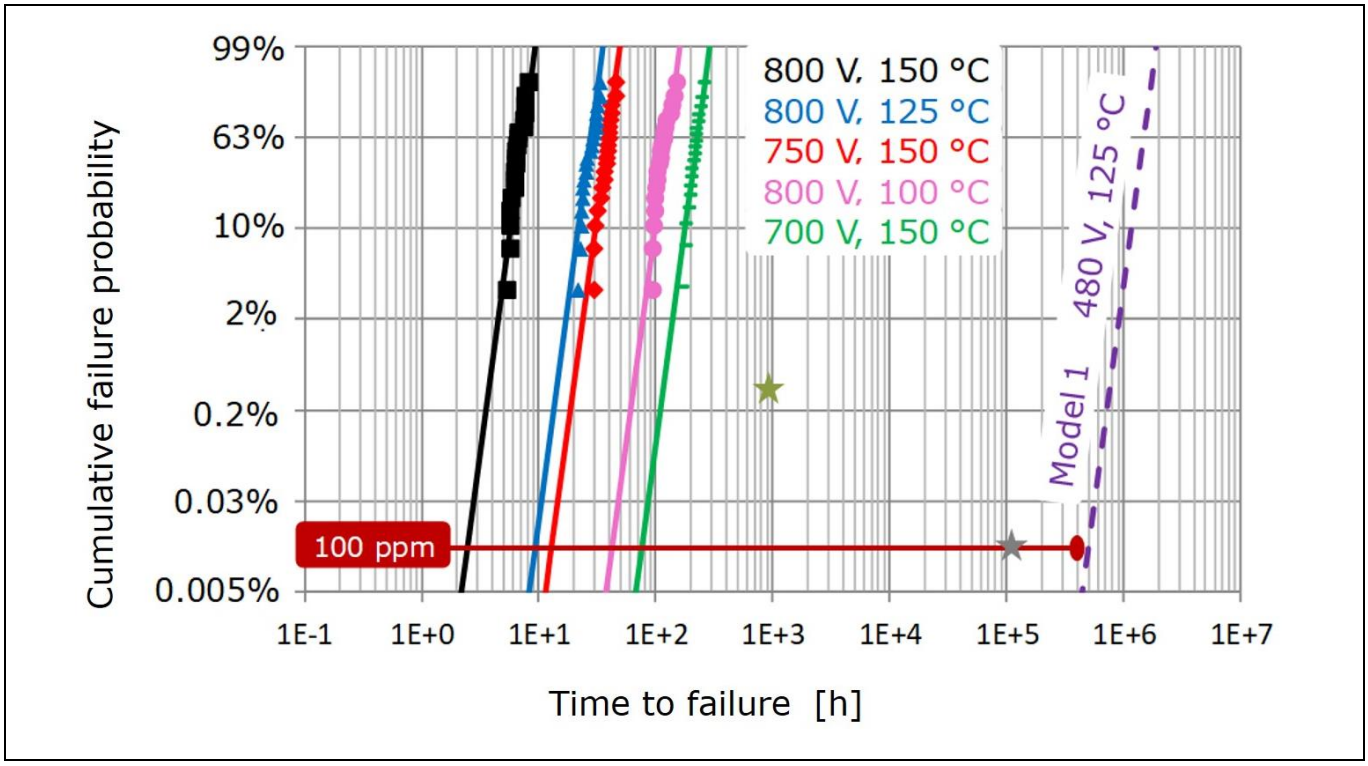

Figure 11 Infineon's Weibull plot for DC bias time to failure for a matrix of voltage and temperature [6]

One can see that five different stress conditions were chosen with voltage spanning 700 V, 750 V and 800 V (far exceeding the device rating of 600 V), and temperature covering the range of 100 ˚C to 150 ˚C (see Figure 11 for details). It is characteristic of GaN HEMTs that they can withstand much higher voltages than their silicon counterparts which go into avalanche breakdown abruptly at a voltage slightly higher than the rated value. The time to failure data is displayed on a Weibull plot with the time axis in logarithmic scale and y axis chosen as a measure of the cumulative fraction of failed devices from a linearized version of the Weibull equation (Equation 1). It is evident that all groups have slope, $\beta > 1$ and so reflect intrinsic failure. The data fit well a model which shows temperature and voltage behavior in the forms shown in Figure 12. The temperature acceleration behaves according to the previously introduced Arrhenius equation while the stress voltage dependence is best modeled by the Eyring (exponential) model. As shown, the combined acceleration can be taken from the product of the individual voltage and temperature acceleration factors. From these factors the failure curve can be estimated for user specified combinations of voltage and temperature. For example, applying the acceleration factor conditions of 480 V and 125 ˚C results in a projection of the dashed line shown. Note the strong dependence of failure time on bias; devices at 800 V and 125 ˚C all fail in less than approximately

30 hours while devices at 480 V and 125 ˚C are projected to fail at approximately 2 million hours. So although the GaN devices can non-destructively withstand voltage stress much higher than their silicon counterparts, their lifetime at such high voltages is limited. The model shows a lifetime greater than three times the target. The green star indicates the typical qualification time and failure fraction detectable with existing silicon qualification methods - they are insufficient to predict useful life. The grey start indicate the target lifetime that is 15 years at 100 parts per million (ppm).

Bias Under Temperature:
(Arrhenius Model)

$$AF(T) = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)}$$

Voltage bias:
(Eyring Model)

$$AF(V) = e^{\beta(V_{stress} - V_{use})}$$

Temperature and bias:

$$AF(V,T) = AF(V) * AF(T)$$

Figure 12 Model equations for temperature (Arrhenius) and voltage (Eyring) acceleration factors, and combined acceleration

3.2.1 What is the avalanche capability of GaN devices and how does it compare to silicon?

GaN devices can withstand higher reverse voltage stress than their equivalently rated silicon MOSFET counterparts. A visual comparison of the drain current versus drain voltage curve for each of the devices is shown in Figure 13.

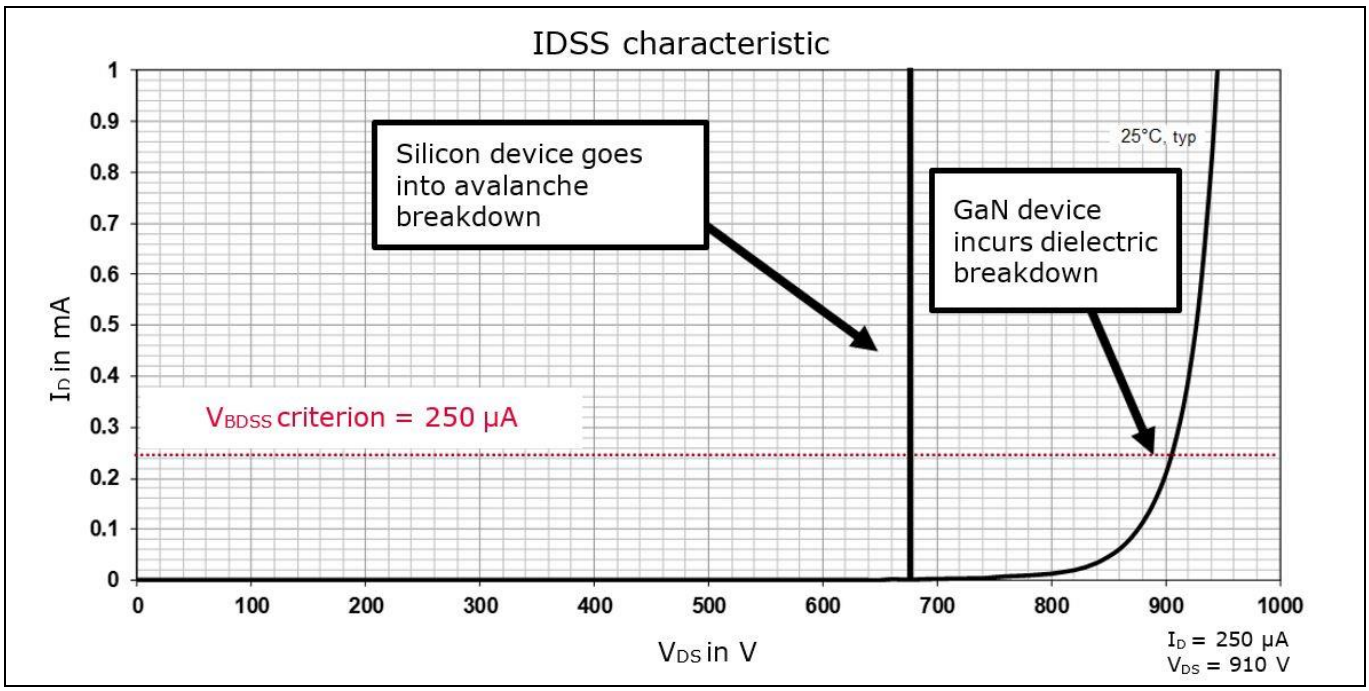

Figure 13 Overlay of drain current versus drain voltage traces for a 600 V-rated GaN HEMT and a 650V-rated silicon SJ MOSFET

The graph shows an overlay of the off-state I-V curve for both devices. The 650V-rated silicon device reaches avalanche between 650 V and 700 V, and can no longer block voltage. If it is kept at this condition for too long, it will go beyond its thermal limits and fail destructively, thus it can tolerate the avalanche condition only as long as it does not exceed its thermal rating. Avalanche ratings are provided as a measure of that thermal limit. By comparison the GaN device does not go into such abrupt avalanche condition. The 600V-rated GaN HEMT can tolerate a higher reverse voltage; it reaches 910Vat the same drain current value as the 650 V silicon MOSFET. Nevertheless, similar to the silicon device, it can tolerate this condition only for a period of time, but in this case not only due to a thermal but also a time limit because of the TDDB failure mechanism.

3.3 Switching SOA failure mode and model

A second key new degradation mechanism for GaN devices is switching SOA (also known as dynamic high temperature operating life or DHTOL). Along with other semiconductor manufacturers, Infineon has published long-term application switching data, showing stable device operation (measured as steady case temperature) in hard switching (boost) application over time periods from 1,000 to 3,000 hours (Figure 14).

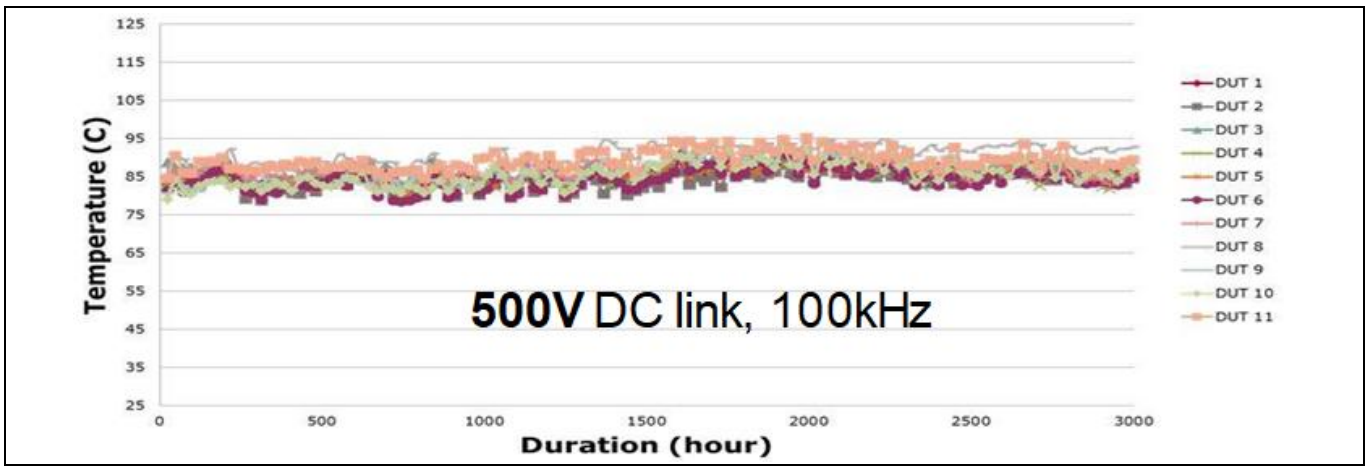

Figure 14 Eleven devices tested in hard switched boost application to 3,000 hours with no failure and steady power dissipation

3,000 or even 10,000 hours (corresponding to 18 - 60 weeks) of typical application is obviously not enough to make conclusions for the entire intended design lifetime which typically spans years. Therefore, Infineon set up a test platform that allows accelerated testing at higher than designed voltage and current to investigate if the reliability of long-term switching operation can be better predicted. Figure 15 shows a schematic of this test circuit. The device damage in the test circuit was limited in order to allow failure analysis of devices which destruct under test. This circuit operates devices in a hard switching boost configuration such as might be experienced in a PFC or other application circuits.

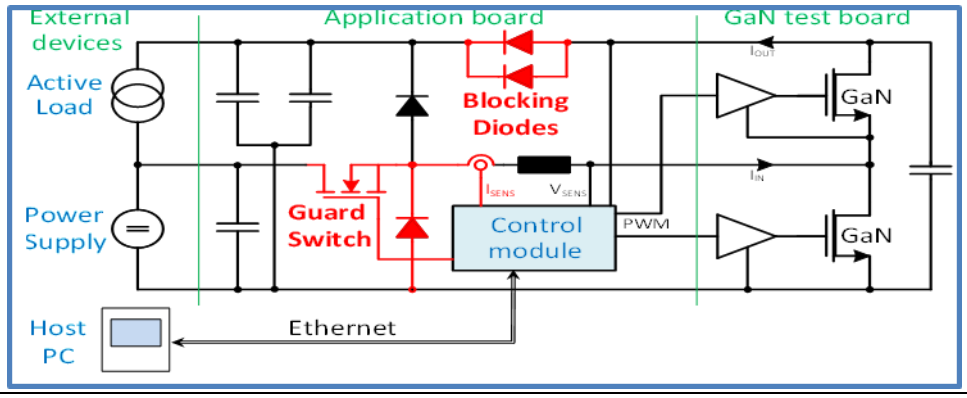

Figure 15 Schematic application circuit for accelerated hard switching boost stress. Devices under test are held on a separate GaN test board.

The Infineon test platform allows testing at accelerated bus voltage up to 700 V (versus typical use condition of 420 V), and at higher than rated device current. Above a certain threshold of peak I-V conditions in testing of samples under accelerated hard switching, device failure did occur over time. A model was extracted that allows failure rate prediction as a function of current, voltage, and frequency. Additional accelerated testing was performed with CoolGaN™ HEMTs also in a soft switching operating condition such as routinely occurs in DC-DC converters with an LLC architecture as well as with other topologies. In this case no failures were observed at and beyond those operating conditions at which failures had occurred during testing under accelerated hard switching. It shows that the switching trajectory or locus is very important with respect to possible failure during device dynamic operation (see Figure 16).

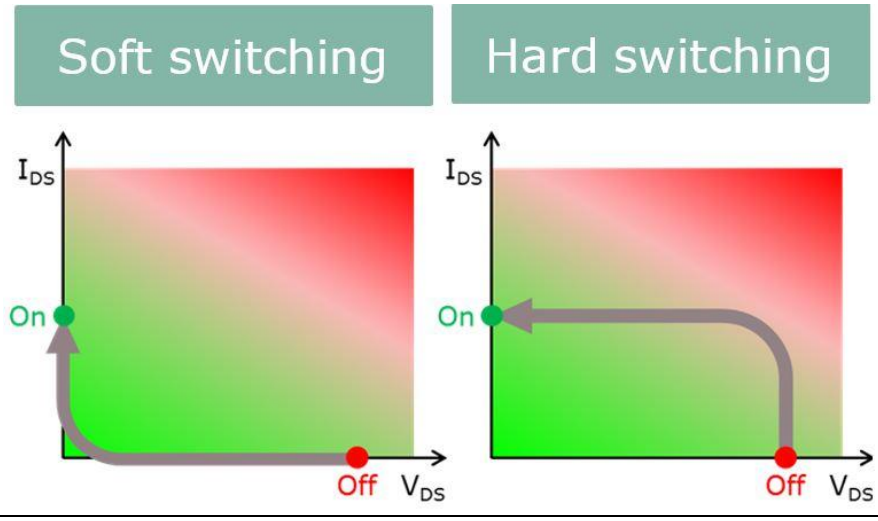

Figure 16 Device I-V trajectory under soft switching (left) and hard switching (right)

Rossetto et al [7] made a study that shines a light on the difference between hard and soft switching behavior. In this study a special evaluation test rig was introduced which allowed for adjusting the current and voltage overlap, that occurs during hard switching, while also allowing dynamic $R_{DS(on)}$ measurement. On the same test stand both soft and hard switching could be performed. Additionally, special test device structures (e.g., HEMTs) were used which allowed taking electroluminescence (EL) measurements simultaneously with the switching event. Electroluminescence has been established as a

means to detect hot electrons in GaN HEMT devices [8]. The degree of overlap of the I and V during switching was controlled by varying the drain and the gate overlap. The drain gate delay (DGD) is a measure of the overlap where more negative values correspond to “harder” switching while zero overlap corresponds to soft switching. All measurements were taken during turn-off. The results show a strong correlation between hard switching (thus more negative DGD) and both hot electrons (indicated by higher EL count) and dynamic $R_{DS(on)}$ (depicted in Figure 17). Thus, hot electrons may be associated with both dynamic $R_{DS(on)}$ and device failure during hard switching.

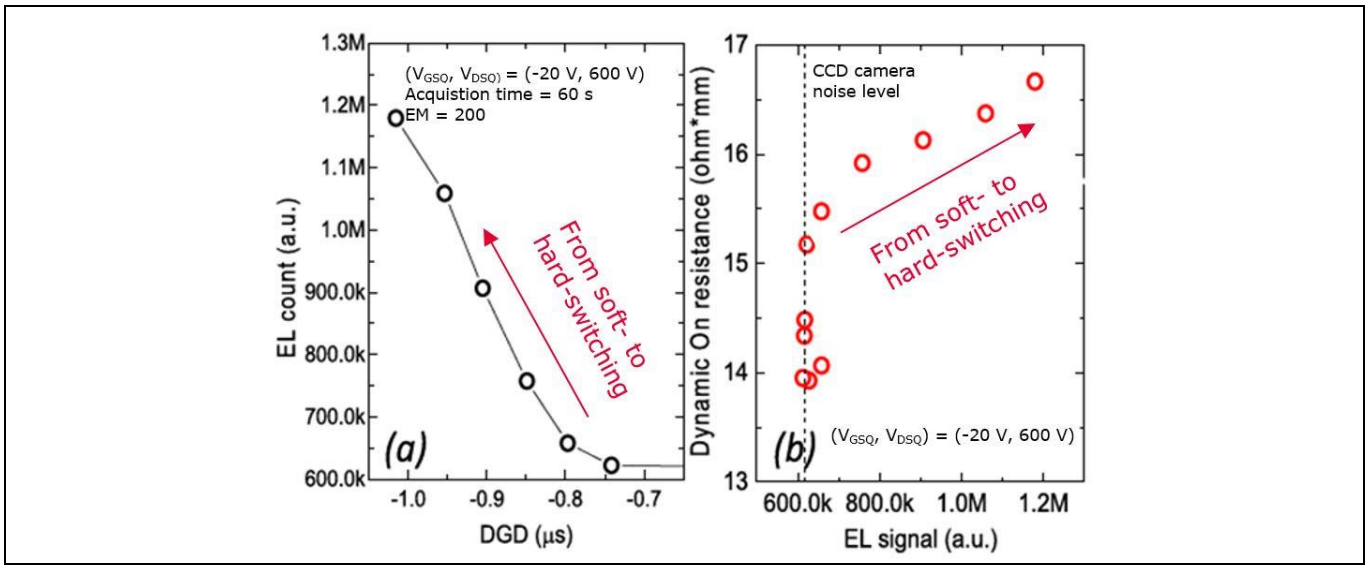

Figure 17 Experimental switching set up that allows operating in hard switching (D_{GD} < 0) to soft switching (D_{GD} tends to zero) shows correlation between EL, dynamic $R_{DS(on)}$ and degree of hard switching [7]

As stated earlier, silicon devices do not have such a dynamic switching behavior related failure mechanism while GaN switches have. This points out the benefit and importance of following Infineon‘s proposed qualification method and model that to be discussed later in this paper.

3.4 Dynamic on-state resistance

Another failure mechanism that applies to GaN devices but not for silicon is dynamic on-state resistance, $R_{DS(on)}$ (Figure 18). During off state, the device has high voltage applied between drain and source. In this plot the output characteristic (I –V) for initial (pre-stress) condition is shown in solid blue. The tangent or slope of this curve that is shown in dashed blue line corresponds to the initial $R_{DS(on)}$ value. Also the post-stress value of the same is shown (in pink). The stress applied between initial and post measurements is DC bias. Post stress, the output curve changes slope (corresponding to increased $R_{DS(on)}$) and the peak output current reduces. This is because there are lateral (between surface drain and gate) and vertical (between surface drain connections and the silicon substrate at source potential) electric field components. The 2DEG on the drain side sits at high potential, its electrons can be attracted to and (transiently) trapped by positive charges either in the GaN bulk (substrate side) or in the surface layers above the AlGaN. During post stress measurement, when the device first turns on and the high drain to source voltage collapses, these charges remain briefly trapped and are unavailable to carry

current. The result is a temporary (dynamic) increase in $R_{DS(on)}$. As the traps release the charges (as there is no longer a high field to hold them), the 2DEG is fully repopulated and the $R_{DS(on)}$ recovers to its pre stress value.

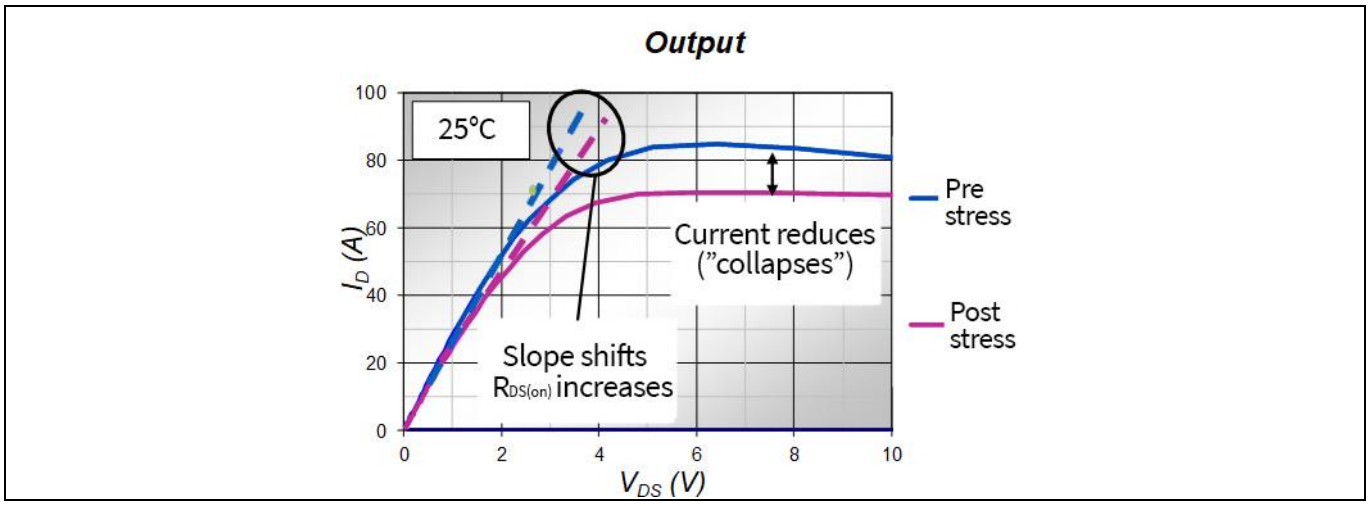

Figure 18 $R_{DS(on)}$ shifts between measured pre (blue dashed line) value and post (pink dashed line) application of DC bias

Through careful attention paid to the design of the device as well as the heteroepitaxial layer structure and materials, Infineon CoolGaN™ devices have very low dynamic $R_{DS(on)}$. Dynamic $R_{DS(on)}$ can be a strong function of voltage (V_{DS}) applied. The plot in Figure 19 shows variation in dynamic $R_{DS(on)}$ (as measured at 20 A under hard switching) with voltage. Infineon CoolGaN™ product varies very little even out to the rated voltage of 600 V while the competitor devices show a strong increase in dynamic $R_{DS(on)}$ even above 400 V. As dynamic $R_{DS(on)}$ is a transient phenomenon, a lower delay offers a more sensitive measurement; in this case the delay time between voltage application and measured $R_{DS(on)}$ was set at 700 nanoseconds.[2]

[2] *However some competitors have published values as high as 2.5 microseconds, the test measurement complexity poses challenges here [9]. Infineon continues to further develop the measurement capability and will publish updates over time.*

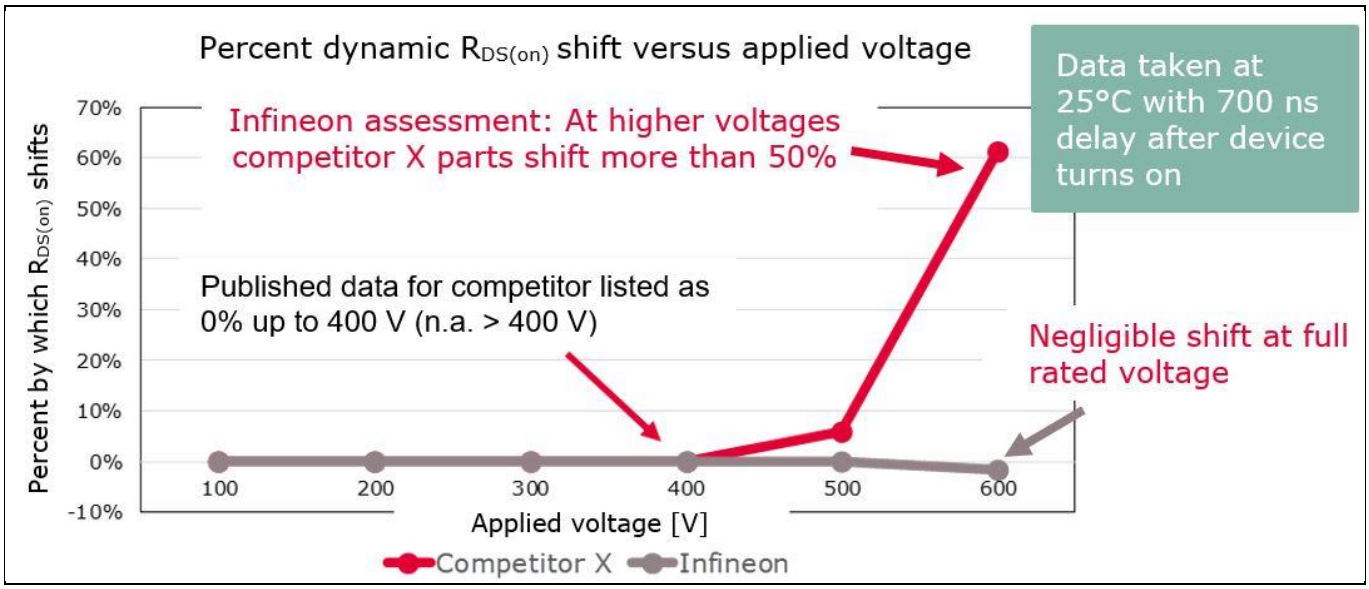

Figure 19 Dynamic $R_{DS(on)}$ as a function of drain voltage for Infineon and competitor "X" device. Testing was done under hard switching conditions at 20 A. Note that some suppliers publish data taken at soft switching conditions which is not as stressful on devices.

Stable dynamic $R_{DS(on)}$ is an important criterion for reliable operation in application circuits. As previously discussed, there appears to be a correlation between high dynamic $R_{DS(on)}$ and the repetitive switching SOA related failure mechanism we have just studied. Some suppliers may point out that their device is good for operation since it may have low or modest dynamic $R_{DS(on)}$ at or below application stress voltage (e.g., as for competitor „x“ in our example), but the occurrence of dynamic $R_{DS(on)}$ as measured at voltages above the applied voltage (in application) may be a sign of repetitive switching SOA failure mechanism that results in higher failure rate and lower lifetime than expected.

4 How to ensure reliable operation of GaN devices in an application - predicting failure rate

In this section we will discuss how to apply previously described models to real applications. Although Infineon has developed a total of four GaN degradation models, we focus here on the two that are considered as the most important: DC bias and switching SOA.[3] By returning to the application profile, we use these two models as tools to answer the question: how can we be sure that GaN devices will operate to the desired lifetime and quality level?

4.1 Example of telecom AC-DC system application profile

Here we refer back to Tables 3, and 4 and Figure 4 which are taken from the application profile for a 2.5 kW, AC-DC power converter for use in telecom systems.
The PFC uses a CCM totem pole, hard switching configuration at 65 kHz. The DC-DC section uses an LLC (soft switching) topology. Since the telecom system can be installed in extreme environments, a wide temperature range is required (ambient temperature varies between -27.5 ˚C to 72.5 ˚C in the box/cabinet of the system) with the fraction of operating time at each temperature as given. The average voltage output of the PFC is 400 V with a turn off spike/peak between 410 V at standby and 460 V at the 80 -100 % output power condition. Duty cycle is given. The system has 100% operating time with 15 year lifetime, but operates between standby and 80-100% load with given load profile. The load current varies between 1.5 A at standby and 18 A at 80-100% load condition. Not given in Table 3, 4 or Figure 4 is a customer input from the quality requirements profile that the target cumulative failure rate is 1 FIT at 15 years.

4.2 Running the DC bias degradation model for telecom AC-DC

The telecom rectifier is composed of a PFC section and a DC to DC section. We look first to apply the DC bias lifetime to the CCM totem pole PFC.
From the application we know that target lifetime is 15 years and duty cycle of the switch in the PFC is 50%. This corresponds to total bias time of 7.5 years or approximately 65,000 hours. But this must be broken out to total time at each voltage (average of 400 V or peak V at other conditions) and temperature. Accordingly, Infineon's model includes a simple worksheet that allows such inputs as seen in Figure 20. Then, for a representative reference condition, the acceleration factors and equivalent hours for each line item are calculated based on the Arrhenius (temperature) and Eyring (voltage) models described in Figure 12, for a target lifetime the cumulative failure rate is estimated. From the telecom rectifier application profile inputs a value of less than 1 FIT is calculated (1 FIT is equivalent to 1 failure per billion device-hours of operation). Note that this degradation model assumes intrinsic failures only. Process variation and defectivity may enable extrinsic failures to occur with a higher failure rate than calculated using the intrinsic model.

[3] *Infineon has also developed gate degradation and temperature/humidity/bias models, but these are considered to demonstrate robust operation across a wide range of operation.*

Mission profile for: IGxx60R070D1 (High voltage GaN, 70 mΩ)					
#	Operation mode	Duration [h]	Amb. Temp. [°C]	Off: V_{DS} [V]	Junct. Temp. [°C]
1	Total OFF time at average V_{OFF}	6.57E+02	-40	420	15
2	Total OFF time at peak V_{OFF}	1.05E+00	-40	450	15
3	Total OFF time at average V_{OFF}	5.10E+04	25	420	80
4	Total OFF time at peak V_{OFF}	8.30E+01	25	450	80
5	Total OFF time at average V_{OFF}	1.31E+04	55	420	110
6	Total OFF time at peak V_{OFF}	2.10E+01	55	450	110
TOTAL		64955.4 = 7.5 years			

Failure rate predictions	
FR	<1 FIT (dpm / 1000 h)
MTTF:	2.31E + 11 h 26325878 a

Figure 20 Bias/time data from the application profile reused as inputs to the DC Bias degradation lifetime model to estimate a cumulative failure rate of less than 1 FIT in the telecom rectifier application

4.3 Checking the telecom AC-DC application against the switching SOA (DHTOL) model and rating

Based on Infineon's DHTOL / dynamic switching degradation model, repetitive SOA (switching) curves are provided in Infineon`s CoolGaN™ datasheets. Shown in Figure 21 are the curves for the case of part number IGT60R070D1, a 70 mΩ, 600V-rated GaN device.

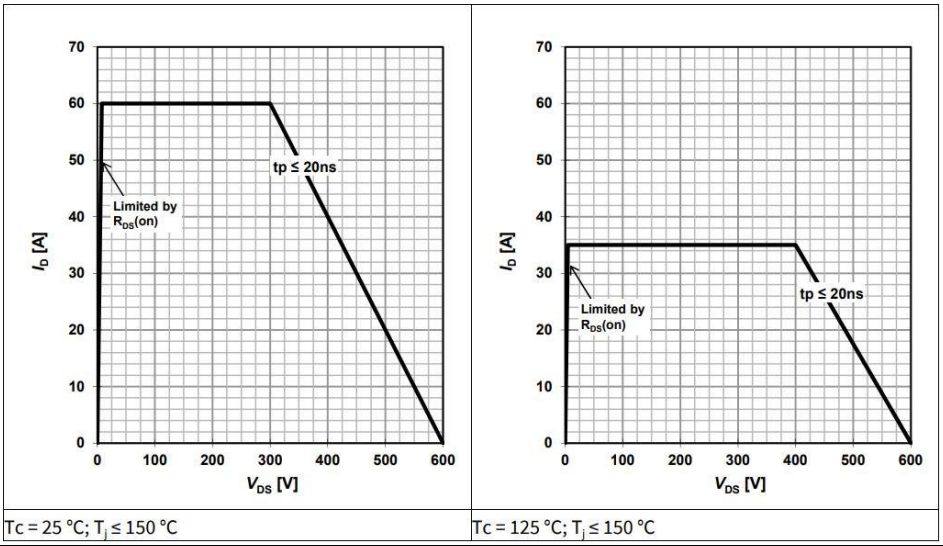

Figure 21 Repetitive safe operation area curves depict the allowable I-V operating regime of CoolGaN™ to avoid failure due to dynamic switching

The flat portion of each curve is limited by the pulsed current rating of the device. Each curve changes slope at a specific I-V point where peak current is allowable, and then decreases as voltage increases. This region of decreasing current is based on Infineon's DHTOL / dynamic switching model and ensures that the device does not operate in a region where it is sensitive to that dynamic switching failure mechanism. The value of current provided in the curves includes dynamic capacitive current associated with charging the printed circuit board parasitic switch node (midpoint between the two transistors).This value is not measurable external to the device but can be modeled. For ease of use, a simplified but conservative estimate of 18 A is used to represent this charging current. This value is generated from Infineon models, based on an assumed worst case value of 230 pF for the switch node parasitic capacitance which should be easily achieved following sound layout practices. Following this estimation method, the current values provided in the curves in Figure 21 can be interpreted to represent peak application current together with 18 A for parasitic charging. For example, a hard-switched application peak current value of 17 A is allowable at 400 V and T_{case} = 125 ˚C. For a boost stage like in a PFC, the turn-on of the low side generates the most stressful hard switching conditions for the switch. Figure 22 shows an example waveform during turn-on of the low side as measured through the inductor- I_L but also through a shunt resistor (solid blue trace). Though the inductor current (I_L) varies little, the current through the shunt clearly shows the effect of device and switch node charging with an application current of 17 A, and a peak charging current spike of 18 A.

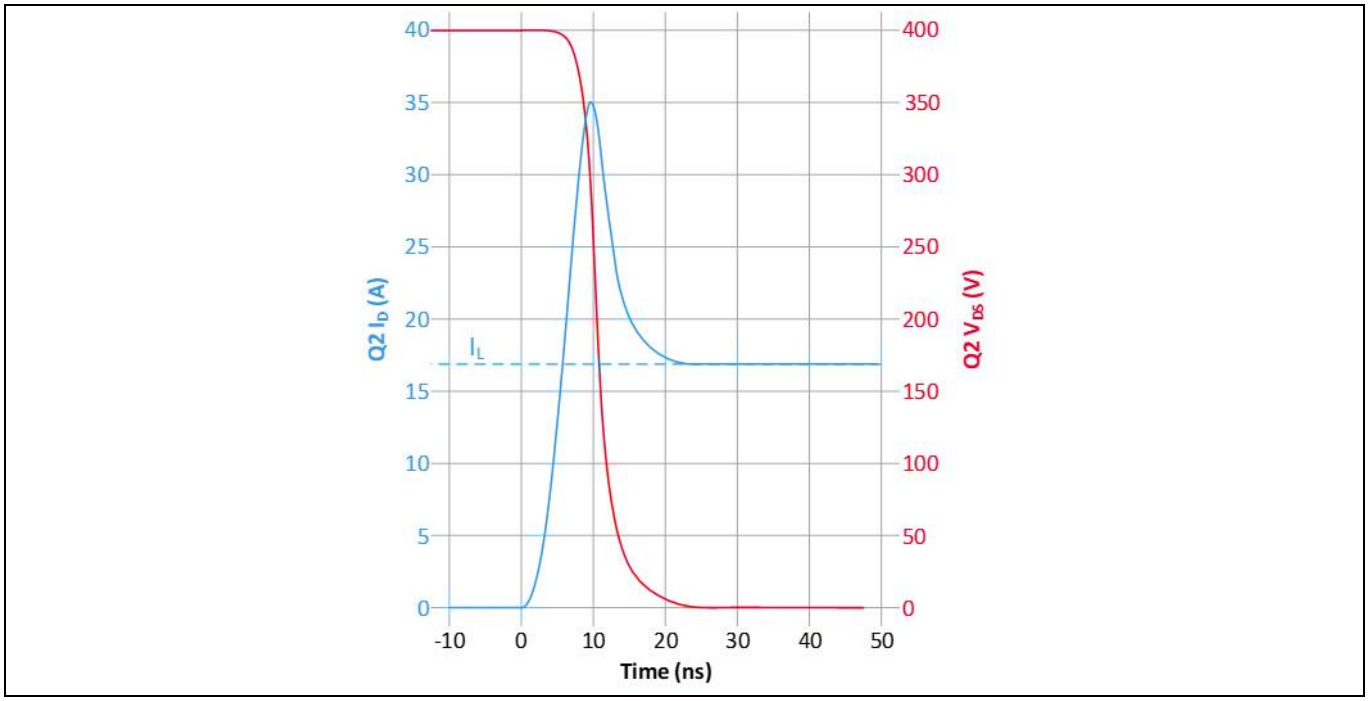

Figure 22 Turn-on current (blue) and voltage (red) waveforms for low-side device in a totem pole boost converter. The dashed line is current measured through the inductor.

Details for this test case were the following:

- DC_{link} = 400 V
- f = 65 kHz
- I_{input} = 20A *(e.g., peak sine wave inductor current for a 2.5 kW PFC stage at low line 180 V_{rms})*
- I_{ripple} = 6A (= 30%)
- $I_{turn\text{-}on}$ = 20A – (6A/2) = 17A *(half ripple subtracted for the low-side switch turn-on)*

- C_{par} = 230 pF
- 2 x $C_{OSS(tr)}$ @ 400 V = 205 pF *(for the subject 70mΩ 600 V GaN device)*
- dV/dt(turn-on) = 42 V/ns
- $I_{overshoot}$ = (C_{par}+2 x $C_{OSS(tr)}$)* dV/dt(turn-on) = 18 A *(for this case shown)*

Calculated peak current is 35 A (17 A inductor current at turn-on with 18 A overshoot added) which is just within the curve of the recommended limits. For these conditions and assuming a 1 FIT allowed failure rate, the predicted lifetime is 15 years at continuous full load operation.

To check switching SOA for any (hard switching) application, the repetitive switching SOA curves and $C_{OSS(tr)}$ for the considered device should be used along with the values of duty cycle, load current variation from the application profile and design specific C_{par} (switch node parasitic capacitance) value.

Conditions for other applications may vary, and also the failure rate lifetime depends on both voltage and current (as the curve describes). Please note, this failure mode applies to hard switching topologies and has not been observed to occur in soft switching conditions. If your application requires conditions far from those outlined above, it is recommended to contact local Infineon applications support to run a more detailed check based on the time and load profile of your application (e.g., short times of over current operation can be compensated by longer phases with partial load).

5 Industry standards for GaN device reliability and qualification

As detailed in this white paper, Infineon follows a comprehensive qualification regime for its CoolGaN™ devices to assure reliable operation in applications. Nevertheless, the importance for the industry to develop comprehensive standards for device qualification is unquestionable. Industry standards are set to ensure that any quality related concerns can be addressed simply and quickly without reference to the details of failure mechanisms for each supplier. Accordingly, Infineon has initiated and contributed to the establishment of a GaN focused subcommittee (JC-70.1) within JEDEC [10] to introduce qualification guidelines and standards with regards to GaN devices.[4] In this JEDEC effort, Infineon supports the views and approaches described in this publication.

[4] *This initiative is ongoing and will follow a multi-step process over time to publish first guidelines and later standards.*

6 Summary of GaN reliability and qualification

In section 1 we pointed out the limitations and risks of applying existing silicon based JEDEC qualification standards to GaN devices. It was detailed that compared to silicon power transistors there are significant material and device design differences that have implications on device failure. Thus, these must be considered for an appropriate GaN product and technology qualification regime. Key failure modes were described and degradation models developed.
The detailed contents of Infineon's GaN qualification program are summarized in the following subsections.

6.1 Traditional stress tests used for GaN product qualification

At the outset we referenced existing silicon device qualification requirements, and listed the nine basic JEDEC tests used for silicon part reliability testing. Although Infineon complies with all nine, one test in particular deserves a mention for its demanding test conditions, namely the HTRB that is performed at 150 ˚C with 600 V reverse bias applied. Given the high sensitivity to voltage acceleration behavior demonstrated in section 3.1, testing at 600 V corresponds to much higher stress than any test at 480 V of bias used by some competitors in their qualification processes.

6.2 Additional stress tests

In addition to the nine JEDEC tests, as part of technology qualification activities, Infineon has performed ten additional investigatory tests. These were performed to accelerated conditions to stress gate passivation and gate dynamic behavior. Accelerated humidity test was also performed, and behavior over wide temperature range was examined.

As an additional risk reduction measure, Infineon also performed eleven different tests at up to 2-5 times the JEDEC specified duration to ensure that unexpected failure or drift behavior would not occur at longer test times.

6.3 Technology qualification: four models

As previously described in detail in sections 3.2 and 3.3, Infineon has established degradation models for DC bias and switching SOA. It is to ensure that the related key failure mechanisms are managed and customer design lifetime and failure rate requirements are met. In addition, Infineon also has two other models which are not detailed in this publication since their use in case of the subject example application is not necessary. These models are gate degradation and temperature, humidity and bias (THB) degradation.

6.4 Other applications

We have demonstrated how Infineon CoolGaN™ devices are expected to meet typical industry lifetime and quality (cumulative failure rate) targets when operated in totem pole, hard switching PFC topology according to the telecom rectifier application profile given in section 2.2. Nevertheless, CoolGaN™ HEMTs fit many other applications and can also be used as a general switch.
Conditions and recommended steps for some other applications/topologies is listed in Table 5. The list provided here is not complete, thus should you have any further applications/topology related questions, please visit www.infineon.com/gan or contact Infineon's local application support.

Table 5 Application suitability highlights table for CoolGaN™

Recommended application	Topology	Conditions / recommended steps
Telecom AC-DC uncontrolled	PFC: CCM totem pole, DC-DC: LLC	Assumes operating conditions as stated in the application profile included in this whitepaper. If operating in extreme environment it is recommended to request local Infineon applications support to run humidity/bias model.
Telecom AC-DC controlled	PFC: CCM totem pole, DC-DC: LLC	Assumes operating conditions are no more stringent than those described in this white paper.
Datacenter, server	PFC: CCM totem pole, DC-DC: LLC	Assumes operating conditions are no more stringent than those described in the application profile discussed in this white paper.
Charger/adapter (< 70 W)	Half-bridge based flyback (with clamp to reduce voltage spike)	Voltage spikes must be limited to 480 V or below.
Low power charger Adapter	Single-ended flyback	Reflected voltage and leakage inductance lead to high nominal voltage and high spikes. DC model must be run with specific voltage inputs from customer specific application profile. Possibility of high FIT rate. CoolMOS™ devices are generally recommended for this topology. Contact local Infineon applications support.
Photovoltaic inverter	Various	Must fit within switching SOA curve and also DC bias model must be run with inputs from customer specific application profile. Recommend to run temperature, humidity and bias model if operating in extreme environment. Possibility of higher FIT rate. Request local Infineon applications support.
Motor control	Hard switched inverter	Must fit within switching SOA curve and also DC bias model must be run with inputs from customer specific application profile. Possibility of higher FIT rate. Request local Infineon applications support if needed.
Wireless power	Class E	High frequency but not hard switched. Must respect peak voltage limits and DC bias life model.
Audio	Class D	Assumes hard switching within the switching SOA curve boundaries.
DC-DC	Phase shifted full-bridge	Assumes switching SOA is within datasheet limits and peak voltage is less than 480 V.

Not recommended application	Topology	Conditions/recommended steps
Linear switch	Conduction occurs at high voltage	GaN is not recommended for linear loads. However CoolGaN™ can survive SMPS pulses within the switching SOA limit the switching SOA curve in single or regular basis.

7 Conclusions

GaN devices can enable new levels of system efficiency, density and reduced overall system cost. This paper has outlined the comprehensive and application specific qualification process that Infineon followed to ensure that CoolGaN™ devices meet the target lifetime and quality requirements, operate reliably in real applications. Figure 23 associates the described qualification process of CoolGaN™ with the new GaN device materials and structures that were outlined at the outset of this document. Based on our test/qualification results, CoolGaN™ is ready for reliable use to increase efficiency and density in a broad range of applications.

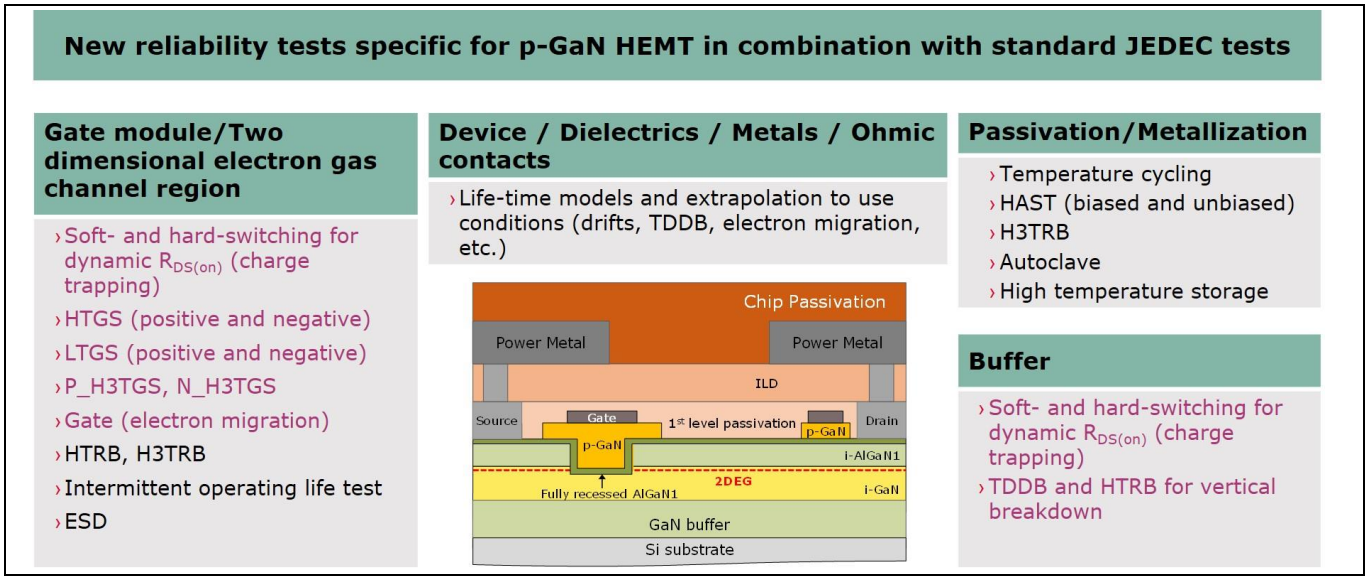

Figure 23 Schematic drawing describing key GaN HEMT features. Surrounding this are the tests that are used to stress these key features. Items in black font type are "traditional" tests used with silicon devices. Tests in purple were developed for use with GaN devices.

For Infineon's CoolGaN™ portfolio of switches and dedicated GaN EiceDRIVER™, please visit www.infineon.com/gan and www.infineon.com/gan-eicedriver.

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